TM52F0200

DATA SHEET

Rev 1.0

AMENDMENT HISTORY

Version	Date	Description
V1.0	Jul, 2017	New release.

CONTENTS

$TM52_{Series}$ F52xx FAMILY

Common Features

CPU	MTP/Flash Program Memory	RAM Bytes	Dual Clock	Operation Mode	Timer0 Timer1 Timer2	UART	Real-time Timer3	LVD	LVR
Fast 8051 (2T)	4K~16K With IAP, ISP, ICP	256 ~ 512	SXT SRC FXT FRC	Fast Slow Idle Stop	8051 Standard		15-bit	2.3V	1.8V 2.3V 2.9V

Note: IAP, ISP only for Flash type program memory

Family Members Features

P/N	Program Memory	RAM Bytes	IO Pin	PWM	SAR ADC	Touch Key	LCD	LED	SPI	Others
TM52F0200	Flash 8K Bytes	512	30	(8+2)-bit x2	12-bit 12-ch	– 14-ch	4x18	4x18	Yes	–

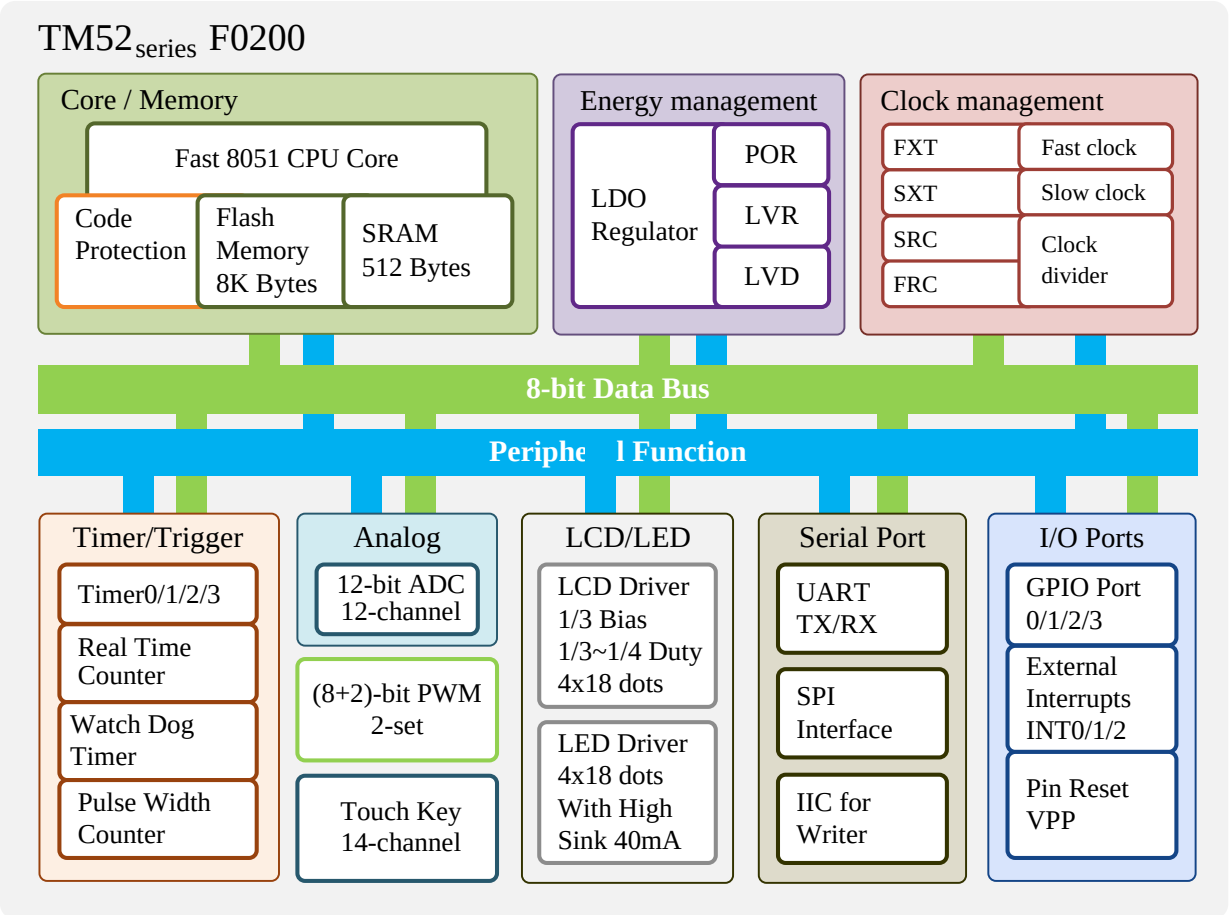
P/N	Operation Voltage	Operation Current (V_{CC}=3V) MODE3V=1, PWRSAV=1, LVR Disable				Max. System Clock (Hz)			
		Fast FRC	Slow SRC	Idle SRC	Stop	SXT	SRC	FXT	FRC
TM52F0200	1.8~5.5V	2.5mA	9μA	3μA	< 0.1μA	32K	24K	8M	7.37M

GENERAL DESCRPTION

TM52 Series **TM52F0200** are versions of a new, fast 8051 architecture for an 8-bit microcontroller single chip with an instruction set fully compatible with industry standard 8051, and retains most 8051 peripheral's function block. Typically, the **TM52** executes instructions six times faster than the standard 8051 architecture.

The TM52F0200 provides improved performance, lower cost and fast time-to-market by integrating features on the chip, including 8K Bytes Flash program memory, 512 Bytes SRAM, Low Voltage Reset (LVR), Low Voltage Detector (LVD), dual clock power saving operation mode, SPI Interface, 8051 standard UART and Timer0/1/2, real time clock Timer3, LCD/LED driver, 2 set (8+2)-bit PWMs, 12 channels 12-bit A/D Convertor, 14 channels Touch Key and Watchdog Timer. Its high reliability and low power consumption feature can be widely applied in consumer and home appliance products.

BLOCK DIAGRAM



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051
2. **8K Bytes Flash Program Memory**
   - Support “In Circuit Programming” (ICP) or “In System Programming” (ISP) for the Flash code
   - Byte Write “In Application Programming” (IAP) mode is convenient as Data EEPROM access
   - Code Protection Capability
3. **Total 512 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 256 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
4. **Four System Clock type Selections**
   - Fast clock from 1~8 MHz Crystal (FXT)
   - Fast clock from Internal RC (FRC 7.3728 MHz)
   - Slow clock from 32768 Hz Crystal (SXT)
   - Slow clock from Internal RC (SRC 24 KHz)
   - System clock can be divided by 1/2/4/16 option
5. **8051 Standard Timer – Timer0/1/2**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1
   - 16-bit Timer2, also supports T2O clock output for Buzzer application
6. **15-bit Time3**
   - Clock source is Slow clock
   - Interrupt period can be clock divided by 32768/16384/8192/128 option
7. **8051 Standard UART**
   - One Wire UART option can be used for ISP or other application
8. **Two independent "8+2" bits PWMs with prescaler/period-adjustment**
9. **SPI Interface**
   - Master or Slave mode selectable
   - Programmable transmit bit rate
   - Serial clock phase and polarity options
   - MSB-first or LSB-first selectable
10. **14-Channel Touch Key**
11. **12-bit ADC with 10 Channels External Pin Input and 2 Channels Internal Reference Voltage**

12. LCD Controller/Driver

- 1/3~1/4 Duty
- Max. 4 COM x 18 SEG
- 1/3 LCD Bias
- 8 Brightness Level selection

13. LED Controller/Driver

- 1/3~1/4 Duty
- Max. 4 COM x 18 SEG
- 40mA High Sink COM
- Active High or Active Low Common Output
- COM Dead Time option

14. 11 Sources, 4-level Priority Interrupt

- Timer0/Timer1/Timer2/Timer3 Interrupt
- INT0/INT1 Falling-Edge/Low-Level Interrupt
- Port1 Pin Change Interrupt
- UART TX/RX Interrupt
- P3.7 (INT2) Interrupt
- ADC/Touch Key Interrupt
- SPI Interrupt

15. Pin Interrupt can Wake up CPU from Power-Down (Stop) mode

- P3.2/P3.3 (INT0/INT1) Interrupt & Wake-up
- P3.7 (INT2) Interrupt & Wake-up
- Each Port1 pin can be defined as Interrupt & Wake-up pin (by pin change)

16. Max. 30 Programmable I/O pins

- CMOS Output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up can be Enable or Disable

17. Independent RC Oscillating Watchdog Timer

- 360ms/180ms/90ms/45ms Selectable WDT Timeout options

18. Five types Reset

- Power on Reset
- Selectable External Pin Reset
- Software Command Reset
- Selectable Watchdog Timer Reset
- Selectable Low Voltage Reset

19. 3-level Low Voltage Reset

- TM52F0200: 1.8V/2.3V/2.9V (can be disabled)

20. 1-level Low Voltage Detect

- 2.3V (can be disabled)

21. Four Power Saving Operation Modes

- Fast/Slow/Idle/Stop Mode

22. On-chip Debug/ICE interface

- Use P3.0/P3.1 pin or P2.4/P2.5 pin
- Share with ICP programming pin

23. Operating Voltage and Current

- VCC=2.3V~5.5V @FSYSCLK=7.3728 MHz
- VCC=2.0V~5.5V @FSYSCLK=3.6864 MHz
- ICC=3μA @Stop mode, MODE3V=0, PWRSAV=1, VCC=3V
- ICC=3μA @Stop mode, MODE3V=1, PWRSAV=1, VCC=3V

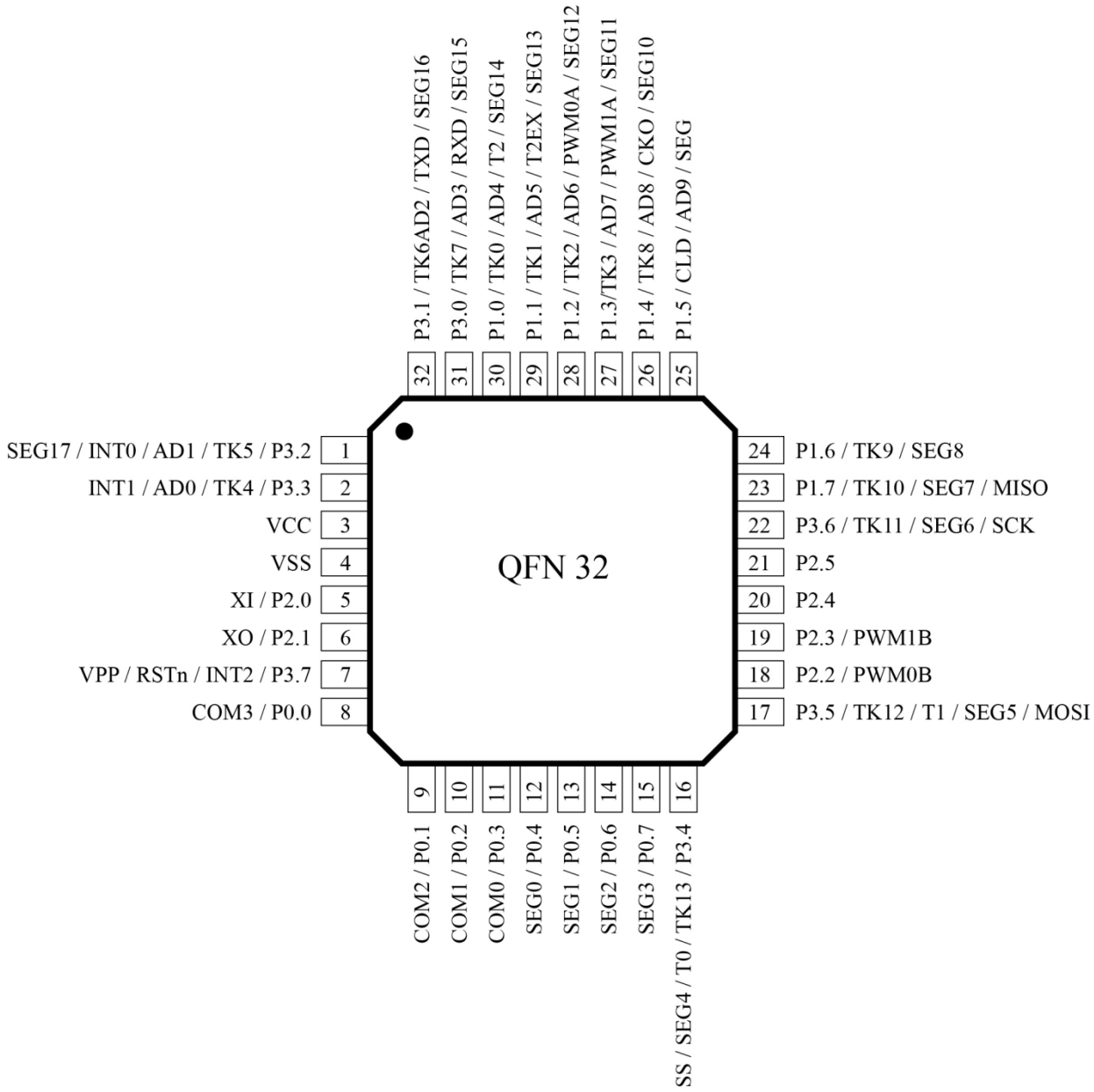
24. Operating Temperature Range

- TM52F0200: –20°C ~ +70°C

25. Package Types

- QFN32 pin (5*5*0.75 – 0.5mm)

PIN ASSIGNMENT



PIN DESCRIPTION

Name	In/Out	Pin Description
P0.0~P0.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or CMOS push-pull output. Pull-up resistors are assignable by software.
P1.0~P1.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software. These pin's level change can wake up CPU from Idle/Stop mode.
P2.0~P2.1	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P2.2~P2.5	I/O	Bit-programmable I/O port for Schmitt-trigger input or CMOS push-pull output. Pull-up resistors are assignable by software.
P3.0~P3.2	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "pseudo open drain" output. Pull-up resistors are assignable by software.
P3.3~P3.6	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up resistors are assignable by software.
P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or "open-drain" output. Pull-up resistor is fix enable.
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Stop mode wake up input.
INT2	I	External falling edge Interrupt input, Idle/Stop mode wake up input.
RXD	I/O	UART Mode0 transmit & receive data, Mode1/2/3 receive data
TXD	I/O	UART Mode0 transmit clock, Mode1/2/3 transmit data. In One Wire UART mode, this pin transmits and receives serial data.
T0, T1, T2	I	Timer0, Timer1, Timer2 event count pin input
T0O	O	Timer0 overflow divided by 64 output
T2O	O	Timer2 overflow divided by 2 output
CKO	O	System Clock divided by 2 output
T2EX	I	Timer2 external trigger input
PWM0A PWM0B PWM1A PWM1B	O	8+2 bit PWM output
AD0~AD9	I	ADC input
TK0~TK13	I	Touch Key input
CLD	I/O	Touch Key charge collection capacitor connection pin
SEG0~SEG17	O	LCD/LED segment output
COM0~COM3	O	LCD/LED common output
MISO	I/O	SPI data input for master mode, data output for slave mode
MOSI	I/O	SPI data output for master mode, data input for slave mode
SS	I	SPI active low slave select input for slave mode
SCK	I/O	SPI clock output for master or clock input for slave mode
RSTn	I	External active low reset input, Pull-up resistor is fixed enable
XI, XO	–	Crystal/Resonator oscillator connection for system clock
VPP	I	Flash programming high voltage input
VCC, VSS	P	Power input pin and ground

PIN SUMMARY

TM52F0200

Pin Number		Pin Name	Type	Input			Output			Alternate Function						Misc
QFN-32				Pull-up Control	Wake up	Ext. Interrupt	P.P.	P.O.D.	O.D.	LCD/LED	ADC	SPI	UART	PWM	Timer	
1		INT0/AD1/SEG17/P3.2	I/O	O	●	●	●	●		●	●					
2		INT1/AD0/P3.3	I/O	O	●	●	●		●		●					
3		VCC	P													
4		VSS	P													
5		XI/P2.0	I/O	O			●		●							Crystal
6		XO/P2.1	I/O	O			●		●							Crystal
7		VPP/RSTn/INT2/P3.7	I/O	⊙	●	●			●							Reset
8		COM3/P0.0	I/O	◉			●			●						
9		COM2/P0.1	I/O	◉			●			●						
10		COM1/P0.2	I/O	◉			●			●						
11		COM0/P0.3	I/O	◉			●			●						
12		SEG0/P0.4	I/O	◉			●			●						
13		SEG1/P0.5	I/O	◉			●			●						
14		SEG2/P0.6	I/O	◉			●			●						
15		SEG3/P0.7	I/O	◉			●			●						
16		T0/T0O/SS/SEG4/P3.4	I/O	O			●		●	●		●			●	
17		T1/MOSI/SEG5/P3.5	I/O	O			●		●	●		●			●	
18		PWM0B/P2.2	I/O	◉			●							●		
19		PWM1B/P2.3	I/O	◉			●							●		
20		P2.4	I/O	◉			●									
21		P2.5	I/O	◉			●									
22		SCK/SEG6/P3.6	I/O	O			●		●	●		●				
23		MISO/SEG7/P1.7	I/O	O	●		●		●	●		●				
24		SEG8/P1.6	I/O	O	●		●		●	●						
25		AD9/SEG9/P1.5	I/O	O	●		●		●	●	●					
26		CKO/AD8/SEG10/P1.4	I/O	O	●		●		●	●	●					
27		PWM1A/AD7/SEG11/P1.3	I/O	O	●		●		●	●	●			●		
28		PWM0A/AD6/SEG12/P1.2	I/O	O	●		●		●	●	●			●		

Pin Number		Pin Name	Type	Input			Output			Alternate Function						Misc
QFN-32				Pull-up Control	Wake up	Ext. Interrupt	P.P.	P.O.D.	O.D.	LCD/LED	ADC	SPI	UART	PWM	Timer	
29		T2EX/AD5/SEG13/P1.1	I/O	⊙	●		●		●	●	●				●	
30		T2/T2O/AD4/SEG14/P1.0	I/O	⊙	●		●		●	●	●				●	
31		RXD/AD3/SEG15/P3.0	I/O	⊙			●	●		●	●		●			
32		TXD/AD2/SEG16/P3.1	I/O	⊙			●	●		●	●		●			

Symbol:

P.P. = Push-Pull Output
O.D. = Open Drain
P.O.D. = Pseudo Open Drain

PS:

1. ⊙ 3.7 Pull up resistor is fix enable
2. ⊙ Port1, P2.0, P2.1, Port3 these pins control Pull up resistor by operation modes
3. ⊙ Port0, P2.2~P2.5 these pins control Pull up resistor while PxOE.n=0 and Px.n=1

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as “A” or “ACC” including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The “B” register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B.

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A.

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** B register

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer. The Stack Pointer points to the top location of the stack.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer (DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs.

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below.

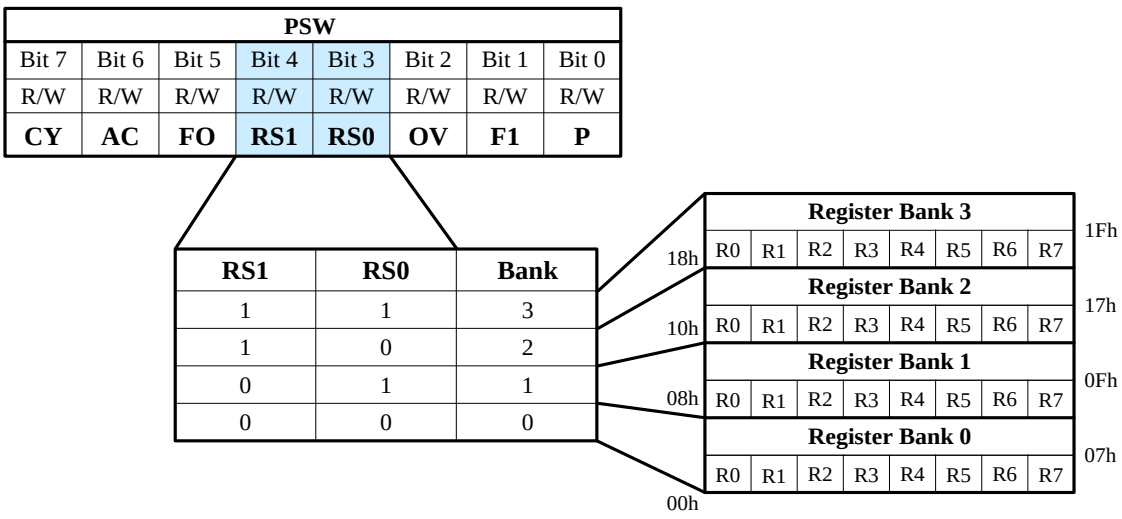
Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag
D0h.6 **AC:** ALU auxiliary carry flag
D0h.5 **F0:** General purpose user-definable flag
D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
00: Bank 0 (00h~07h)
01: Bank 1 (08h~0Fh)
10: Bank 2 (10h~17h)
11: Bank 3 (18h~1Fh)
D0h.2 **OV:** ALU overflow flag
D0h.1 **F1:** General purpose user-definable flag
D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.



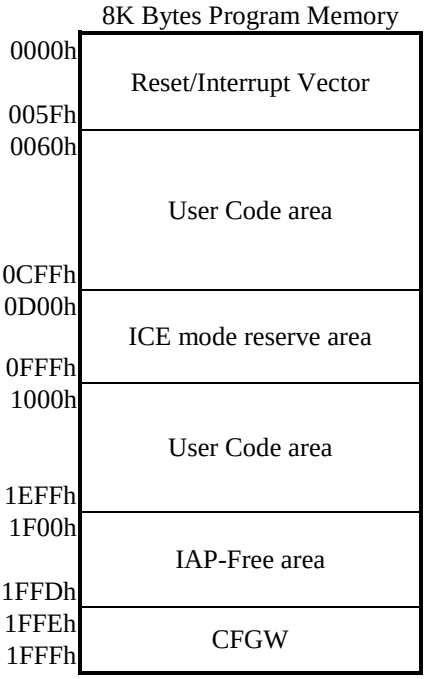
2. Memory

2.1 Program Memory

The Chip has an 8K Bytes Flash program memory, which can support In Circuit Programming (ICP), In Application Programming (IAP) and In System Programming (ISP) function modes. The Flash write endurance is at least 50K cycles. The Flash program memory address continuous space (0000h~1FFFh) is partitioned to several sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 2 bytes (1FFEh~1FFFh) of program memory is defined as chip Configuration Word (CFGW), which is loaded into the device control registers upon power on reset (POR). The address space 1F00h~1FFDh is the IAP free area, while the 0000h~005Fh is occupied by Reset/Interrupt vectors as standard 8051 definition. In the in-circuit emulation (ICE) mode, user also needs to reserve the address space 0D00h~0FFFh for ICE System communication.



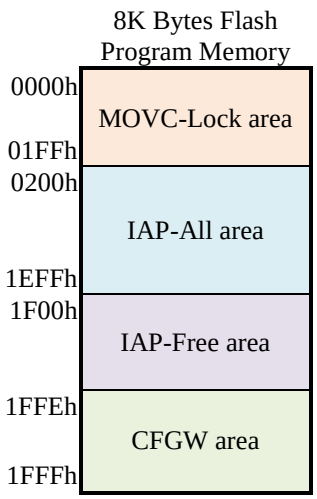
2.1.2 Flash ICP Mode

The Flash memory can be programmed by the tenx proprietary writer **(TWR98/TWR99)**, which needs at least four wires (VCC, VSS, P3.0 and P3.1 pins) to connect to this chip. To shorten the programming time, it is recommended to connect Writer with an additional fifth wire, which is the VPP (P3.7) pin. If the user wants to program the Flash memory on the target circuit board (In Circuit Programming, ICP), these pins must be reserved sufficient freedom to be connected to the Writer. More pins connected to Writer ensure more writing efficiency and speed. The P3.0 and P3.1 pin's can be replaced by P2.4 and P2.5.

Writer wire number	Pin connection
4-Wire	VCC, VSS, P3.0, P3.1
5-Wire	VCC, VSS, P3.0, P3.1, VPP
7-Wire	VCC, VSS, P3.0, P3.1, VPP, P3.3, P1.2 ***Note:*** P3.2 output FRC/2 and P3.5 always output Low in this mode

2.1.3 Flash IAP Mode

The Chip has “In Application Programming” (IAP) capability, which allows software to read/write data from/to the Flash memory during CPU run time as conveniently as data EEPROM access. The IAP function is byte writable, meaning that the Chip does not need to erase one Flash page before write. The available IAP data space is 254 Bytes after chip reset, and can be re-defined by the “MVCLOCK” and “IAPALL” control register as shown below.



Flash Memory	MVCLOCK	IAPALL	MOVC Accessible	MOVX (IAP) Accessible
0000h~01FFh	1	X	No	No
	0	0	Yes	No
	0	1	Yes	Yes
0200h~1EFFh	X	0	Yes	No
	X	1	Yes	Yes
1F00h~1FFDh	X	X	Yes	Yes
1FFEh	X	0	Yes	No
	X	1	Yes	Yes
1FFFh	X	X	Yes	No

In IAP mode, the program Flash memory is separated into four sectors: MOVC-Lock area, IAP-All area, IAP-Free area, and CFGW area. These four sectors are regulated differently.

In the **MOVC-Lock area,** IAP read/write is limited by MVCLOCK bit, which can be set to control the accessibility of the MOVC and MOVX instructions to this area. The size of this area is 512 Bytes. The lock function is made to protect the main program code against unconsciously writing Flash memory in IAP mode. Locking or unlocking the function should be performed by the tenx TWR98/99 writing to the CFGW in Flash memory.

The **IAP-All area** is protected by the IAPALL register to prevent IAP mode from writing application data to the program area, resulting in a program code error that cannot be repaired. The size of this area is 7424 Bytes. Enabling IAPALL requires writing 65h to SFR SWCMD 97h to set the IAPALL control flag. Then, software can use MOVX instructions to write application data to flash memory from 0200h to 1EFFh. If user wants to disable IAPALL function, user can write other values to SFR SWCMD 97h to clear the IAPALL control flag. User must be careful not to overwrite program code which is already resided on the same Flash memory area.

The **IAP-Free area** has no control bit to protect. It can be used to reliably store system application data that needs to be programmed once or periodically during system operation. Other areas of Flash memory can be used to store data, but this area is usually the best. The size of this area is 254 Bytes, equivalent to an EEPROM, and Flash memory can provide byte access to read and write commands. In the past, storage of configuration data required an additional EEPROM or the other storage device. However, this functionality can now be provided by on-chip Flash, reducing the chip count of embedded applications. An external EEPROM or SRAM may not be needed.

The **CFGW area** has 2 data bytes (CFGWH and CFGWL), which is located at the last 2 addresses of Flash memory. The CFGWH is not accessible to IAP, while the CFGWL can be read or written by IAP in case the IAPALL flag is set. CFGWL is copied to the SFR F7h after power on reset, software then take over CFGWL’s control capability by modifying the SFR F7h.

2.1.4 IAP Mode Access Routines

Flash IAP write is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target Flash address (0000h~1FFEh), and the ACC contains the data being written. The Chip accepts IAP Write command only when the IAPWE SFR is enabled. Flash IAP writing requires approximately 500μs. Meanwhile, the CPU stays in a waiting state, but all peripheral modules (Timers, LCD, and others) continue running during the writing time. The software must handle the pending interrupts after an IAP write. Flash IAP writing needs higher V_{CC} voltage, V_{CC}>2.8V.

Because the Program memory and the IAP data space share the same entity, a Flash IAP read can be performed by the "MOVX A, @DPTR" or "MOVC" instruction as long as the target address points to the 0000h~1FFFh area. A Flash IAP read does not require extra CPU wait time.

```
; IAP example code ; need VCC>2.8V
MOV     DPTR, #1F00h        ; DPTR=1F00h=target IAP address
MOV     A, #5Ah             ; A=5Ah=target IAP write data
MOV     INTE1, #A0h         ; IAPWE=1
MOVX    @DPTR, A            ; Flash [1F00h] =5Ah, after IAP write
                            ; 200μs~500μs H/W writing time, CPU wait
MOV     INTE1, #00h         ; IAPWE=0 immediately after IAP write
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=5Ah
CLR     A                   ; A=0
MOVC    A, @A+DPTR          ; A=5Ah
```

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

1FFFh.1 **MVCLOCK:** If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **IAPALL (W) :** Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.

97h.0 **IAPALL (R) :** Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	IAPWE			SPIE	TKIE	EX2	P1IE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

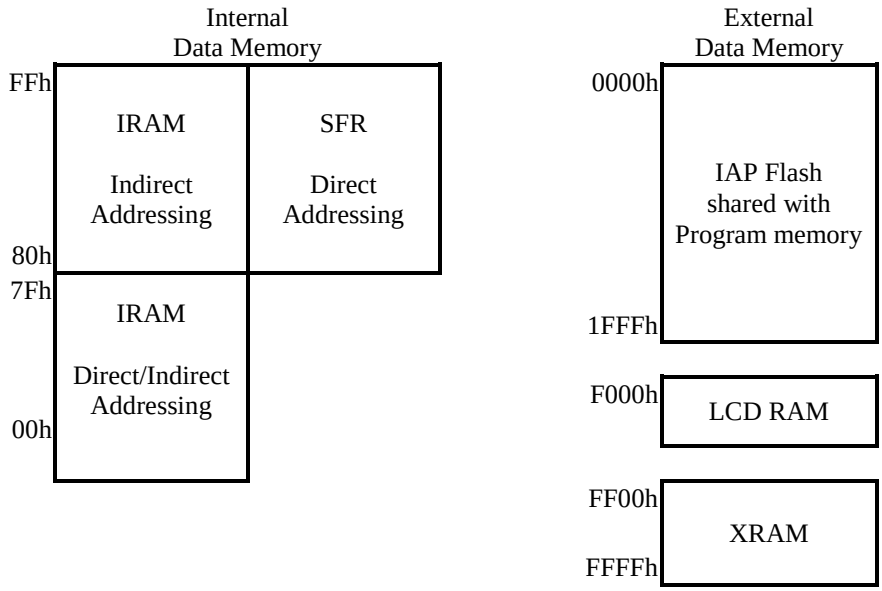
A9h.7~5 **IAPWE:** IAP write enable control
101: Enable IAP write. It is recommended to clear it immediately after IAP write.
Others value: Disable IAP write.

2.1.5 Flash ISP Mode

The "In System Programming" (ISP) usage is similar to IAP, except the purpose is to refresh the Program code. User can use UART/SPI or other method to get new Program code from external host, then writes code as the same way as IAP. ISP operation is complicated; basically it needs to assign a Boot code area to the Flash which does not change during the ISP process.

2.2 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and 67 SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 256 Bytes XRAM, LCDRAM and IAP Flash, which can be only accessed by MOVX instruction.



2.2.1 IRAM

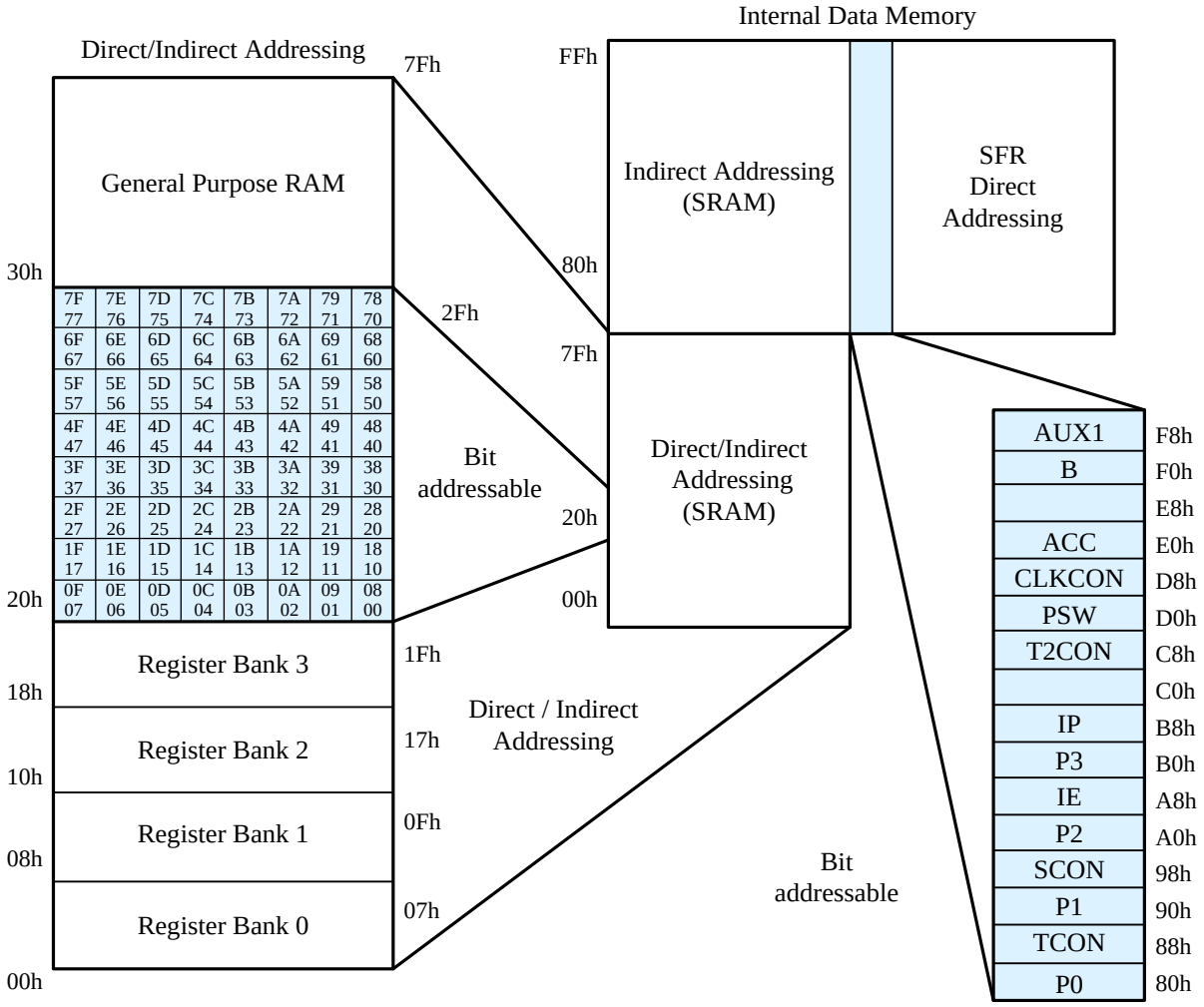
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.2.2 XRAM

XRAM is located in the 8051 external data memory space (address from FF00h to FFFFh). The 256 Bytes XRAM can be only accessed by “MOVX” instruction.

2.2.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the SPI/LCD, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B							CFGWL
E8h								
E0h	ACC							
D8h	CLKCON							
D0h	PSW							
C8h	T2CON		RCP2L	RCP2H	TL2	TH2		
C0h			ATKC10H	ATKC32H	ATKC0L	ATKC1L	ATKC2L	ATKC3L
B8h	IP	IPH	IP1	IP1H	SPCON	SPSTA	SPDAT	
B0h	P3	LCDCON	LCDCON2	LCDPIN				
A8h	IE	INTE1	ADTKDT	ADCDH	TKDL	TKCON	CHSEL	TKCON2
A0h	P2	PWMCON	P1MODL	P1MODH	P3MODL	P3MODH	PINMOD	
98h	SCON	SBUF	PWM0PRD	PWM0DH	PWM1PRD	PWM1DH		
90h	P1	P0OE		P2MOD	OPTION	INTFLG	P1WKUP	SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH				PCON

3. Power

The Chip has a built-in internal low dropout regulator. When MODE3V=0, the voltage regulator outputs 3.3V power to the internal chip circuit. When MODE3V=1, the LDO is turned off, and the internal circuit receives a power supply directly from the VCC pin. Because the LDO consumes 150μA for operation, turning off LDO by setting MODE3V=1 can reduce the Chip current consumption. However, setting MODE3V=1 is only valid for an operating condition of V_{CC}<3.6V. The PWRSAV also control the LDO. When MODE3V=0 and PWRSAV=1, the LDO is turned off in Stop mode for saving power consumption. In addition, set PWRSAV will affect the LVR/LVD setting.

MODE3V=0

Operation Mode	CFGW		LDO	LVR	LVD	Function
	PWRSAV	LVRE				
Fast Slow Idle	X	00	ON	ON	–	LV Reset 2.9V
	X	01	ON	ON	–	LV Reset 2.3V
	X	10	ON	ON	ON	LV Reset Disable/2.0V
	X	11	ON	ON	ON	LV Reset 1.8V/2.0V
Stop	0	00	ON	ON	–	LV Reset 2.9V
	0	01	ON	ON	–	LV Reset 2.3V
	0	10	ON	ON	–	LV Reset Disable/2.0V
	0	11	ON	ON	–	LV Reset 1.8V/2.0V
	1	00	OFF	ON	–	LV Reset 1.8V/2.0V
	1	01	OFF	ON	–	LV Reset 1.8V/2.0V
	1	10	OFF	ON	–	LV Reset Disable/2.0V
	1	11	OFF	ON	–	LV Reset 1.8V/2.0V

MODE3V=1

Operation Mode	CFGW		LDO	LVR	LVD	Function
	PWRSAV	LVRE				
Fast Slow Idle	0	00	OFF	ON	–	LV Reset 2.9V
	0	01	OFF	ON	–	LV Reset 2.3V
	0	10	OFF	ON	ON	LV Reset Disable/2.0V
	0	11	OFF	ON	ON	LV Reset 1.8V/2.0V
	1	00	OFF	ON	–	LV Reset 1.8V/2.0V
	1	01	OFF	ON	–	LV Reset 1.8V/2.0V
	1	10	OFF	ON	–	LV Reset Disable/2.0V
	1	11	OFF	ON	–	LV Reset 1.8V/2.0V
Stop	0	00	OFF	ON	–	LV Reset 2.9V
	0	01	OFF	ON	–	LV Reset 2.3V
	0	10	OFF	ON	–	LV Reset Disable/2.0V
	0	11	OFF	ON	–	LV Reset 1.8V/2.0V
	1	00	OFF	ON	–	LV Reset 1.8V/2.0V
	1	01	OFF	ON	–	LV Reset 1.8V/2.0V
	1	10	OFF	ON	–	LV Reset Disable/2.0V
	1	11	OFF	ON	–	LV Reset 1.8V/2.0V

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

1FFFh.3 **VCCFLT:** Set 1 to enhance the Chip's power noise immunity

1FFFh.2 **PWRSAV:** Power saving function control bit

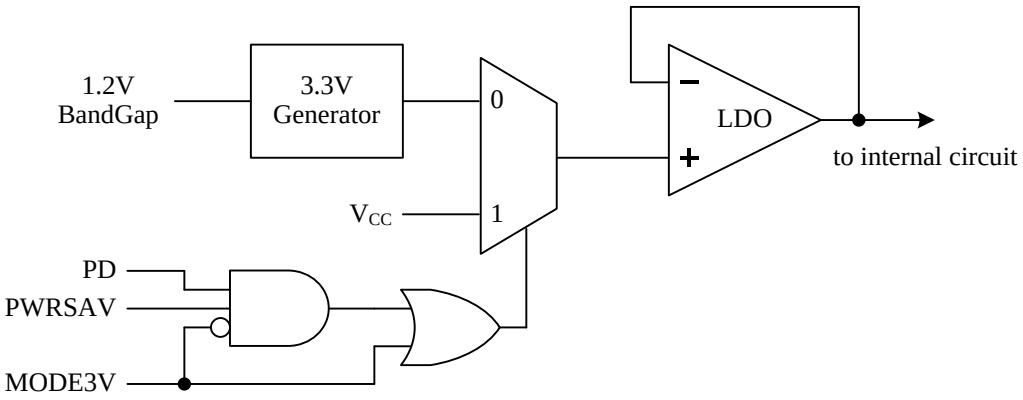
0: Disable Power saving function

1: Enable Power saving function

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.6 **MODE3V:** 3V mode selection control bit

If this bit is set, the Chip can be only operated in the condition of V_{CC}<3.6V, and LDO is turned off to save current



4. Reset

The Chip has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGW controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 40 ms as chip warm up time, then downloads the CFGW register from Flash‘s last two bytes (Other Reset will not reload the CFGW). The Power on Reset needs VCC pin’s voltage first discharge to near VSS level, then rise beyond 2.0V.

4.2 External Pin Reset

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the Chip. External Pin Reset can be disabled or enabled by CFGW.

4.3 Software Command Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watchdog Timer Reset

WDT overflow Reset is disabled or enabled by SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

The Chip offers three options for LVR and Low Voltage Detection (LVD) functions. The user can make a selection by CFGW, let LVR voltages of 2.9V, 2.3V, and 1.8V/2.0V be selected separately, and let LVD be 2.3V only. If the LVR is selected as 1.8V/2.0V, the 2.3V LVD flag is available for LVD. If LVR is selected as 2.3V or 2.9V, the LVD flag cannot be used.

System Clock frequency	8 MHz	6 MHz	4 MHz	2 MHz
Minimum LVR level	LVR=2.9V	LVR=2.9V	LVR=2.3V	LVR=1.8V/2.0V

LVR setting table

Note: LVR must be enable, also refer to AP-TM52XXXXX_02S for LVR setting information

Flash **1FFEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL	WDTE		–	FRCF				

1FFEh.7~6 **WDTE:** Watchdog Timer Reset control
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode
11: Watchdog Timer Reset always enable

Flash **1FFFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWH	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

1FFFh.6 **XRSTE:** External Pin Reset control
0: Disable External Pin Reset
1: Enable External Pin Reset

1FFFh.5~4 **LVRE:** Low Voltage Reset function select
00: Set LVR at 2.9V
01: Set LVR at 2.3V
10: LVR disable and set LVD at 2.3V
11: Set LVR at 1.8V and LVD at 2.3V

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 360ms WDT overflow rate
01: 180ms WDT overflow rate
10: 90ms WDT overflow rate
11: 45ms WDT overflow rate

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.7 **LVD:** Low Voltage Detect flag
Set by H/W when a low voltage occurs. The flag is valid when LVR is 2.0V. This flag is disabled in Stop mode or if MODE3V=1 and PWRSAV=1.

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	IAPALL/SWRST							
R/W	W							R/W
Reset	–							0

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle

5. Clock Circuitry and Operation Mode

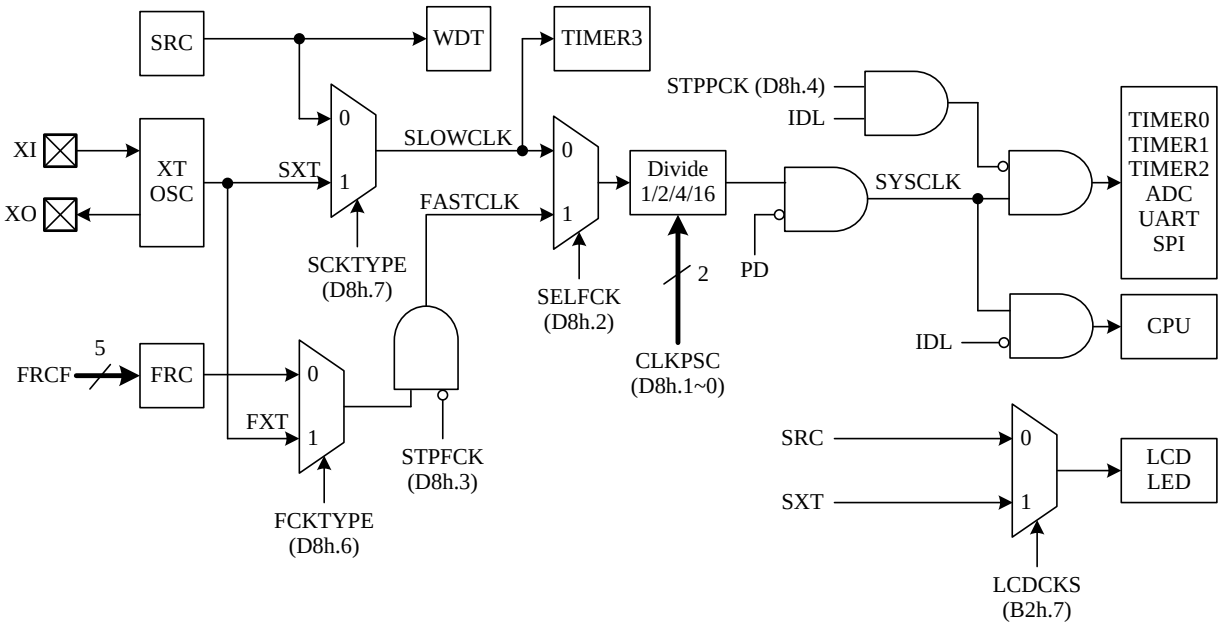
5.1 System Clock

The Chip is designed with dual-clock system. During runtime, user can directly switch the System clock from fast to slow or from slow to fast. It also can directly select a clock divider of 1, 2, 4 or 16. The Fast clock can be selected as FXT (Fast Crystal, 1~8 MHz) or FRC (Fast Internal RC, 7.3728 MHz). The Slow clock can be selected as SXT (Slow Crystal, 32 KHz) or SRC (Slow Internal RC, 24 KHz). Fast mode and Slow mode are defined as the CPU running at Fast and Slow clock speeds.

After Reset, the device is running at Slow mode with 24 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency. In a typical condition, an 8 MHz System clock rate requires V_{CC}>2.5V.

The Chip has an external oscillators connected to the XI/XO pins. It relies on external circuitry for the clock signal and frequency stabilization, such as a stand-alone oscillator, quartz crystal, or ceramic resonator. In Fast mode, the fast oscillator can be used in the range from 1~8 MHz. In Slow mode, the slow oscillator can only use a clock frequency of 32.768 KHz.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.



Note: also refer to AP-TM52XXXXX_01S and AP-TM52XXXXX_02S about System Clock Application Note.

5.2 Operation Mode

There are four operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK=1, Timer0/1/2, ADC and UART are stopped in Idle mode. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT is alive if it is enabled. Stop mode can be terminated by Reset or pin wake up.

Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0, 1, 2)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Stop bit. If 1 Stop mode is entered.
87h.0 **IDL:** Idle bit. If 1, Idle mode is entered.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	
Reset	0	0	–	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC
1: SXT
D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC
1: FXT
D8h.4 **STPPCK:** Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode
D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode.
This bit can be changed only in Slow mode.
D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock
D8h.1~0 **CLKPSC:** System clock prescaler.
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

6. Interrupt and Wake-up

This Chip has an 11-source four-level priority interrupt structure. All enabled Interrupts can wake up CPU from Idle mode, but only the Pin Interrupts can wake up CPU from Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	Flag	Description
0003	IE0	INT0 external pin Interrupt (can wake up Stop mode)
000B	TF0	Timer0 Interrupt
0013	IE1	INT1 external pin Interrupt (can wake up Stop mode)
001B	TF1	Timer1 Interrupt
0023	RI+TI	Serial Port (UART) Interrupt
002B	TF2+EXF2	Timer2 Interrupt
0033	–	Reserved for ICE mode use
003B	TF3	Timer3 Interrupt
0043	P1IF	Port1 external pin change Interrupt (can wake up Stop mode)
004B	IE2	INT2 external pin Interrupt (can wake up Stop mode)
0053	ADIF+TKIF	ADC/Touch Key Interrupt
005B	SPIF+WCOL+MODF	SPI Interrupt

Interrupt Vector & Flag

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

SFR **96h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1WKUP	P1WKUP							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

96h.7~0 **P1WKUP:** P1.7~P1.0 pin individual Wake up/Interrupt enable control
0: Disable
1: Enable

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	ET2	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	–	0	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable
0: Disable all interrupts
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.5 **ET2:** Timer2 interrupt enable
0: Disable Timer2 interrupt
1: Enable Timer2 interrupt

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** INT1 pin Interrupt enable and Stop mode wake up enable
0: Disable INT1 pin Interrupt and Stop mode wake up
1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** INT0 pin Interrupt enable and Stop mode wake up enable
0: Disable INT0 pin Interrupt and Stop mode wake up
1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	IAPWE			SPIE	ADTKIE	EX2	P1IE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A9h.4 **SPIE:** SPI interrupt enable
0: Disable SPI interrupt
1: Enable SPI interrupt

A9h.3 **ADTKIE:** ADC/Touch Key interrupt enable
0: Disable ADC/Touch Key interrupt
1: Enable ADC/Touch Key interrupt

A9h.2 **EX2:** INT2 pin Interrupt enable and Stop mode wake up enable
0: Disable INT2 pin Interrupt and Stop mode wake up
1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.

A9h.1 **P1IE:** Port1 pin change interrupt enable
0: Disable Port1 pin change interrupt
1: Enable Port1 pin change interrupt

A9h.0 **TM3IE:** Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–	PT2	PS	PT1	PX1	PT0	PX0
R/W	–	–	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	0	0	0	0	0	0

B9h.5, B8h.5 **PT2H, PT2:** Timer2 interrupt priority control. (PT2H, PT2) =
00: Level 0 (lowest priority)
01: Level 1
10: Level 2
11: Level 3 (highest priority)

B9h.4, B8h.4 **PSH, PS:** Serial Port (UART) interrupt priority control. Definition as above.
B9h.3, B8h.3 **PT1H, PT1:** Timer1 interrupt priority control. Definition as above.
B9h.2, B8h.2 **PX1H, PX1:** INT1 pin interrupt priority control. Definition as above.
B9h.1, B8h.1 **PT0H, PT0:** Timer0 interrupt priority control. Definition as above.
B9h.0, B8h.0 **PX0H, PX0:** INT0 pin interrupt priority control. Definition as above.

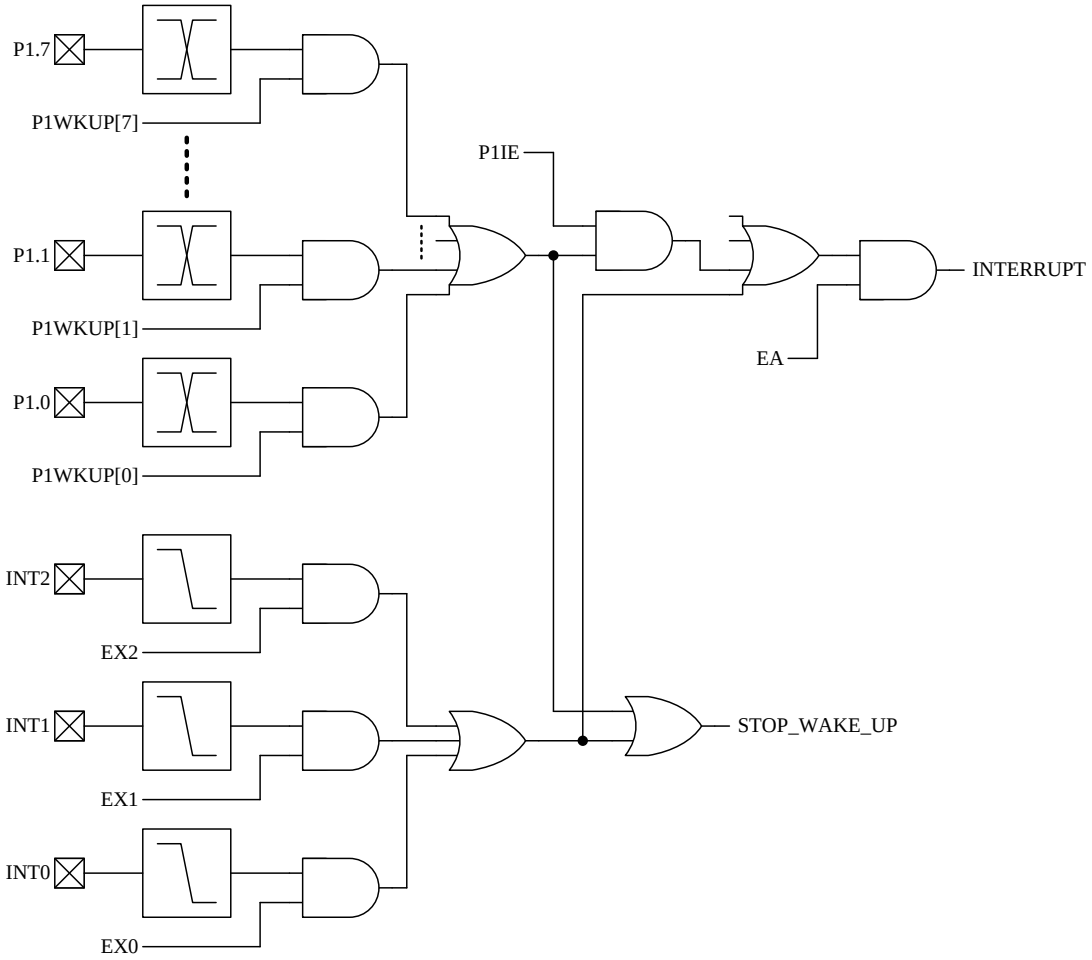
SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	–	–	–	PSPIH	PADTKIH	PX2H	PP1H	PT3H
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	–	–	–	PSPI	PADTKI	PX2	PP1	PT3
R/W	–	–	–	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	0	0	0	0	0

BBh.4, BAh.4 **PSPIH, PSPI:** SPI interrupt priority control. Definition as above.
BBh.3, BAh.3 **PADTKIH, PADTKI:** ADC/Touch Key interrupt priority control. Definition as above.
BBh.2, BAh.2 **PX2H, PX2:** INT2 pin interrupt priority control. Definition as above.
BBh.1, BAh.1 **PP1H, PP1:** Port1 pin change interrupt priority control. Definition as above.
BBh.0, BAh.0 **PT3, PT3:** Timer3 interrupt priority control. Definition as above.

6.2 Pin Interrupt

Pin Interrupts include INT0 (P3.2), INT1 (P3.3), INT2 (P3.7) and Port1 Change Interrupt. These pins also have the Stop mode wake up capability. INT0 and INT1 are falling edge or low level triggered as the 8051 standard. INT2 is falling edge triggered and Port1 Change Interrupt is triggered by any Port1 pin state change.



Pin Interrupt & Wake up

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

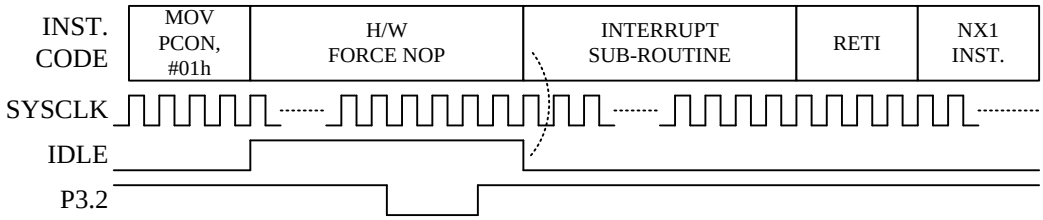
95h.2 **IE2:** External Interrupt 2 (INT2 pin) edge flag
Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FBh to INTFLG to clear this bit. (Note2)

95h.1 **P1IF:** Port1 pin change interrupt flag
Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP).
P1IE does not affect this flag's setting.
It is cleared automatically when the program performs the interrupt service routine.
S/W can write FDh to INTFLG to clear this bit. (Note2)

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

6.3 Idle Mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts (Pins, Timers, ADC, TK, SPI and UART) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. "The first instruction behind IDL (PCON.0) setting" is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

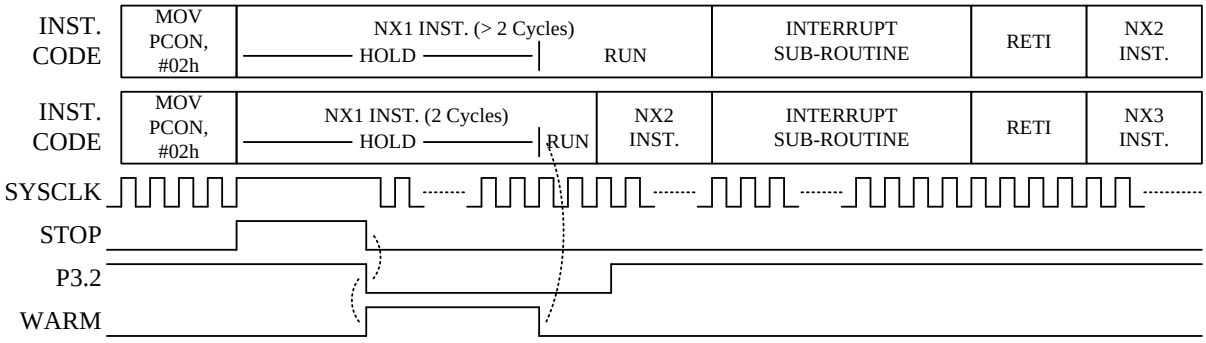
SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Stop bit. If 1, Stop mode is entered.
87h.0 **IDL:** Idle bit. If 1, Idle mode is entered.

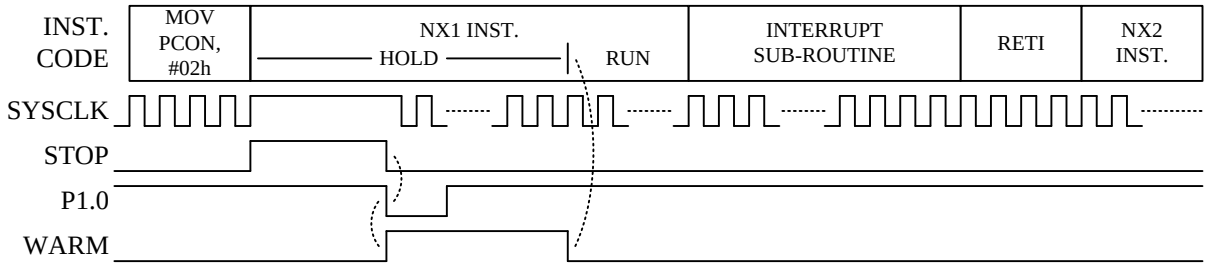
6.4 Stop Mode Wake up and Interrupt

Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1/EX2 can enable INT0/INT1/INT2 pins' Stop mode wake up capability. Set P1WKUP bit 7~0 can enable P1.7~P1.0's Stop mode wake up capability. Upon Stop wake up, "the first instruction behind PD (PCON.1) setting" is executed immediately before Interrupt service. Interrupt entry needs EA=1 (P1WKUP also needs P1IE=1) and the trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Stop mode wake up.

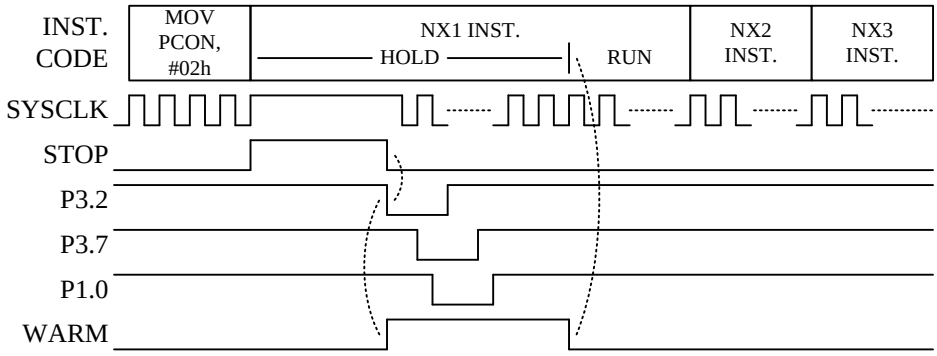
Note: Chip cannot enter Stop Mode if INTn pin is low and wakeup is enable. (INTn=0 and EXn=1, n=0,1,2)



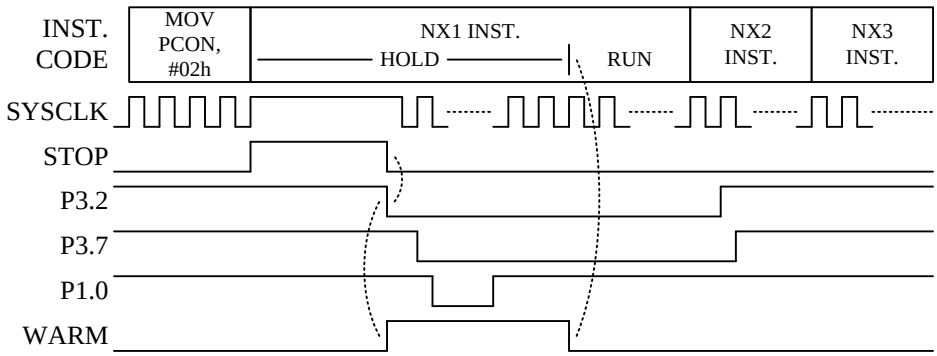
EA=EX0=1
P3.2 (INT0) is sampled after warm-up, Stop mode wake-up and Interrupt.



EA=P1IE=P1WKUP=1
P1.0 change (not need clock sample) , Stop mode wake-up and Interrupt.



EA = EX0=EX2=P1WKUP=1, P1IE=0
Stop mode wake-up but not Interrupt, P3.2/P3.7 pulse too narrow.



EX0=EX2=P1WKUP=1=P1IE=1, EA=0
Stop mode wake-up but not Interrupt.

7. I/O Ports

The Chip has total 30 multi-function I/O pins. All I/O pins follow the standard 8051 “Read-Modify -Write” feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR. (ex: ANL P1, A; INC P2; CPL P3.0)

7.1 Port1 & P2.1~P2.0 & P3.6~P3.0

These pins can operate in four different modes as below.

Mode	Port1, P2.1~P2.0, P3.6~P3.0 pin function		Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
	P3.2~P3.0	Others				
Mode 0	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Pull-up	Y	Y
Mode 1	Pseudo Open Drain	Open Drain	0	Drive Low	N	N
			1	Hi-Z	N	Y
Mode 2	CMOS Output		0	Drive Low	N	N
			1	Drive High	N	N
Mode 3	Alternative Function, such as LCD/LED, ADC and Touch Key		X (don’t care)	–	N	N

Port1, P2.1~P2.0, P3.6~P3.0 I/O Pin Function Table

If a Port1, P2.1~P2.0 or P3.6~P3.0 pin is used for Schmitt-trigger input, S/W must set the I/O pin to Mode0 or Mode1 and set the corresponding Port Data SFR to 1 to disable the pin’s output driving circuitry.

Beside I/O port function, each Port1, P2.1~P2.0 and P3.6~P3.0 pin has one or more alternative functions, such as LCD/LED, ADC and Touch Key. Most of the functions are activated by setting the individual pin mode control SFR to Mode3. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/1, T0/1/2, or RXD/TXD. These pin functions need to set the pin mode SFR to Mode0 or Mode1 and keep the P1.n/P3.n SFR at 1.

Pin Name	8051	Wake-up	CKO	ADC/TK	LCD/LED	others	Mode3
P1.0	T2	Y	T2O	AD4/TK0	SEG14		AD4/TK0
P1.1	T2EX	Y		AD5/TK1	SEG13		AD5/TK1
P1.2		Y		AD6/TK2	SEG12	PWM0A	AD6/TK2
P1.3		Y		AD7/TK3	SEG11	PWM1A	AD7/TK3
P1.4		Y	CKO	AD8/TK8	SEG10		AD8/TK8
P1.5		Y		AD9/CLD	SEG9		AD9/CLD
P1.6		Y		TK9	SEG8		TK9
P1.7		Y		TK10	SEG7	MISO	TK10
P3.0	RXD			AD3/TK7	SEG15		AD3/TK7
P3.1	TXD			AD2/TK6	SEG16		AD2/TK6
P3.2	INT0	Y		AD1/TK5	SEG17		AD1/TK5
P3.3	INT1	Y		AD0/TK4			AD0/TK4
P3.4	T0		T0O	TK13	SEG4	SS	TK13
P3.5	T1			TK12	SEG5	MOSI	TK12
P3.6				TK11	SEG6	SCK	TK11
P2.0						XI	
P2.1						XO	

Port1, P2.1~P2.0, P3.6~P3.0 multi-function Table

The necessary SFR setting for Port1/P2.1~P2.0/P3.6~P3.0 pin's alternative function is list below.

Alternative Function	Mode	Px.n SFR data	Pin State	Other necessary SFR setting
T0, T1, T2, T2EX, INT0, INT1	**0**	1	Input with Pull-up	
	1	1	Input	
RXD, TXD	**0**	1	Input with Pull-up/Pseudo Open Drain Output	
	1	1	Input/Pseudo Open Drain Output	
T0O, T2O, CKO	**0**	X	Clock Open Drain Output with Pull-up	PINMOD P3MODH
	1	X	Clock Open Drain Output	
	2	X	Clock Output (CMOS Push-Pull)	
SEG4~17 (***Note***)	**X**	X	LCD/LED Waveform Output	LCDPIN
TK0~TK13	**0**	1	Touch Key Idling, Pull-up	
	3	X	Touch Key Scanning	
CLD	**3**	X	Touch Key Capacitor Connection	
AD0~AD9	**3**	X	ADC Channel	
PWM0A, PWM1A	**0**	X	PWM Open Drain Output with Pull-up	PINMOD
	1	X	PWM Open Drain Output	
	2	X	PWM Output (CMOS Push-Pull)	
SPI Master Mode MISO	**1**	1	SPI Data Input	SPCON
SPI Master Mode SCK, MOSI	**2**	X	SPI Clock/Data Output (CMOS Push-Pull)	SPCON
SPI Slave Mode MISO	**2**	X	SPI Data Output (CMOS Push-Pull)	SPCON
SPI Slave Mode SCK, MOSI	**1**	1	SPI Clock/Data Input	SPCON
SS	**1**	1	SPI Chip Selection	SPCON
XI, XO	**0**	1	Crystal oscillation	CLKCON

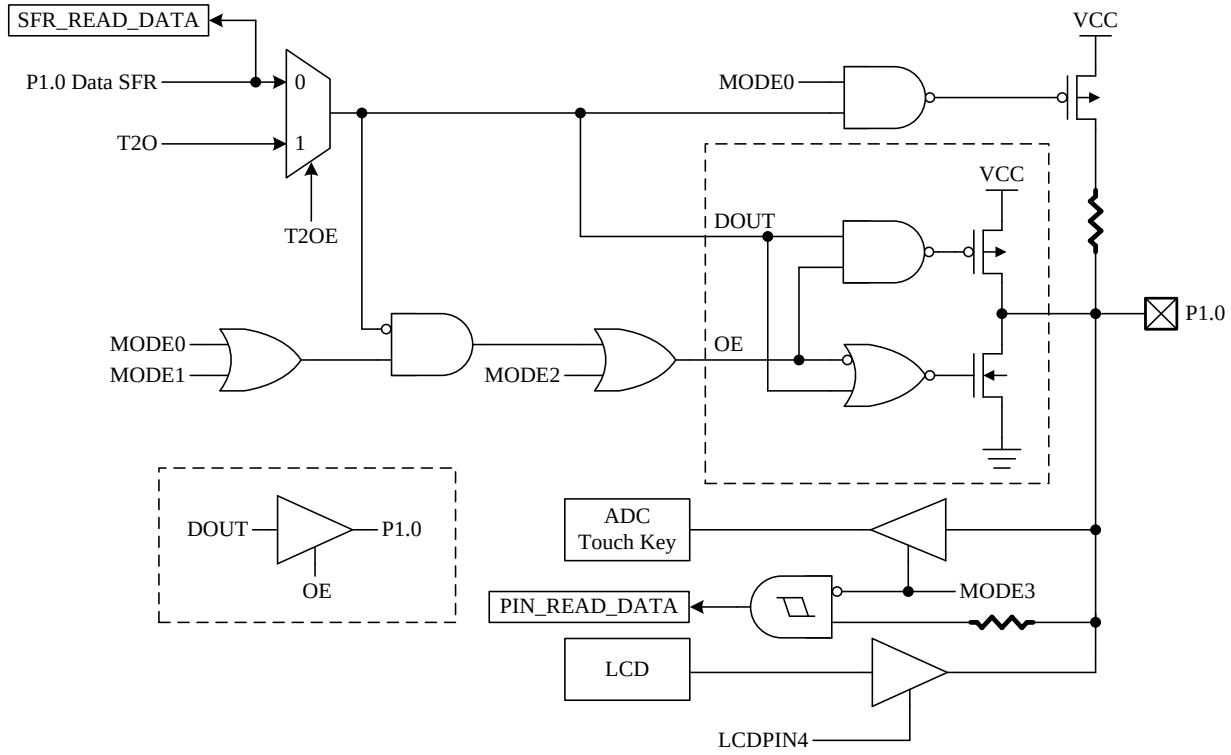
Mode Setting for Port1, P2.1~P2.0, P3.6~P3.0 Alternative Function

For tables above, a **"COMS Output"** pin means it can sink and drive at least 4mA current. It is not recommended to use such pin as input function.

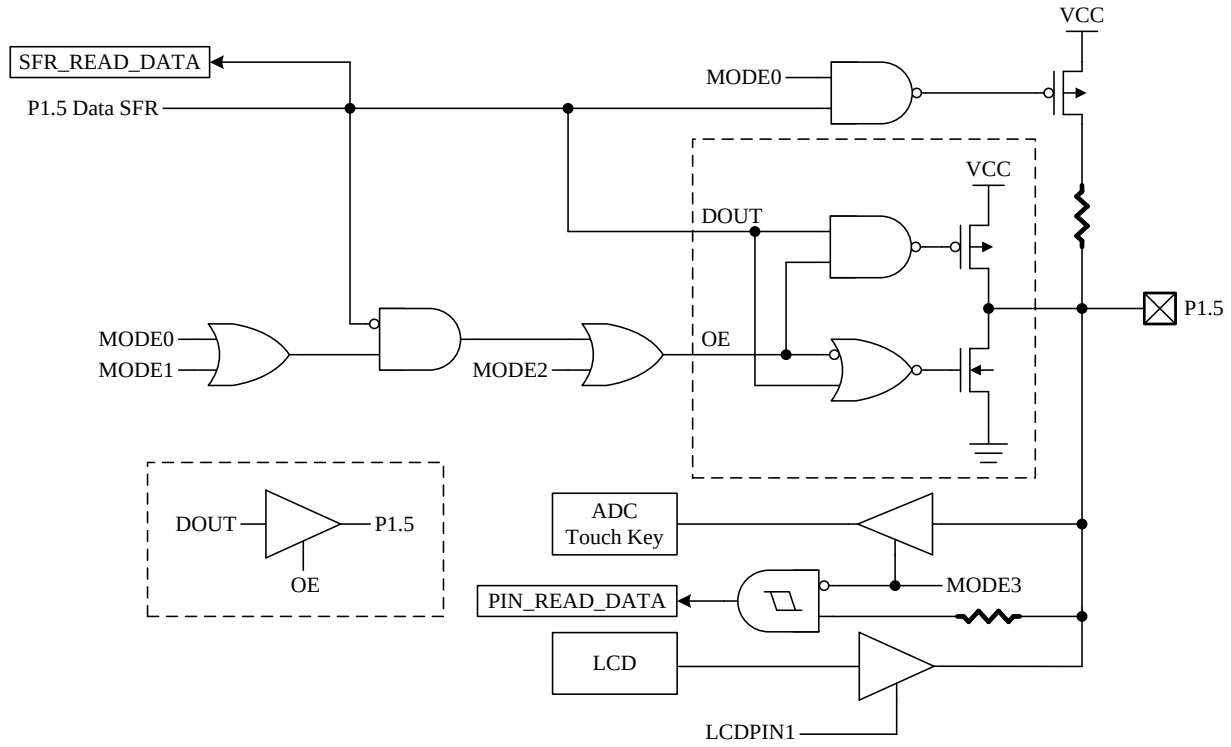
An **"Open Drain"** pin means it can sink at least 4mA current but only drive a small current (<20μA). It can be used as input or output function and typically needs an external pull up resistor.

An 8051 standard pin is a **"Pseudo Open Drain"** pin. It can sink at least 4mA current when output is at low level, and drives at least 4mA current for 1~2 clock cycle when output transits from low to high, then keeps driving a small current (<20μA) to maintain the pin at high level. It can be used as input or output function.

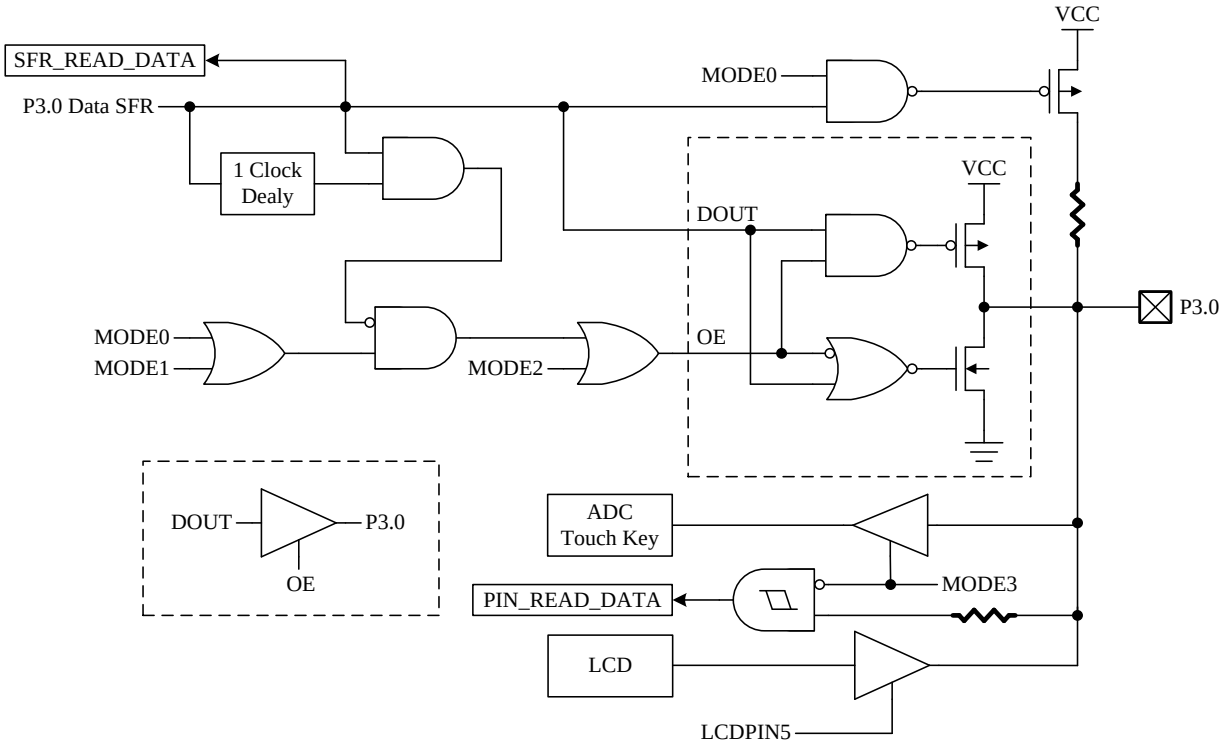
Note: For the necessary SFR setting above, LCDPIN has the highest priority. Therefore, if a pin is not used for Segment (ex: pin is I/O, ADC, TK, SPI…), S/W must disable the pin's LCD/LED Segment function.



P1.0 Pin Structure



P1.5 Pin Structure



P3.0 Pin Structure

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

90h.7~0 **P1:** Port1 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.6~0 **P3.6~P3.0:** P3.6~P3.0 data

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.1~0 **P2.1~P2.0:** P2.1~P2.0 data

SFR **A2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODL	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A2h.7~6 **P1MOD3:** P1.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.3 is ADC or Touch Key input

A2h.5~4 **P1MOD2:** P1.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.2 is ADC or Touch Key input

A2h.3~2 **P1MOD1:** P1.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.1 is ADC or Touch Key input

A2h.1~0 **P1MOD0:** P1.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.0 is ADC or Touch Key input

SFR **A3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MODH	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
R/W	R/W		R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

A3h.7~6 **P1MOD7:** P1.7 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.7 is Touch Key input

A3h.5~4 **P1MOD6:** P1.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.6 is Touch Key input

A3h.3~2 **P1MOD5:** P1.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.5 is ADC input or Touch Key CLD functional pin

A3h.1~0 **P1MOD4:** P1.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P1.4 is ADC or Touch Key input

SFR **A4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODL	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
R/W	R/W		R/W		R/W		R/W	
Reset	0	1	0	1	0	1	0	1

A4h.7~6 **P3MOD3:** P3.3 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.3 is ADC or Touch Key input

A4h.5~4 **P3MOD2:** P3.2 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.2 is ADC or Touch Key input

A4h.3~2 **P3MOD1:** P3.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.1 is ADC or Touch Key input

A4h.1~0 **P3MOD0:** P3.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.0 is ADC or Touch Key input

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
R/W	R/W	–	R/W		R/W		R/W	
Reset	0	–	0	0	0	0	0	0

A5h.7 **T0OE:** Timer0 signal output (T0O) control
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

A5h.5~4 **P3MOD6:** P3.6 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.6 is Touch Key input

A5h.3~2 **P3MOD5:** P3.5 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.5 is Touch Key input

A5h.1~0 **P3MOD4:** P3.4 pin control
00: Mode0
01: Mode1
10: Mode2
11: Mode3, P3.4 is Touch Key input

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2MOD	P2OE				P2MOD1		P2MOD0	
R/W	R/W				R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.3~2 **P2MOD1:** P2.1 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

93h.1~0 **P2MOD0:** P2.0 pin control
00: Mode0
01: Mode1
10: Mode2
11: not defined

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	PWM1BOE	PWM0AOE	PWM0BOE	TCOE	T2OE	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

A6h.7 **PWM1AOE:** PWM1A signal output enable
0: Disable PWM1A signal output to P1.3
1: Enable PWM1A signal output to P1.3

A6h.5 **PWM0AOE:** PWM0A signal output enable
0: Disable PWM0A signal output to P1.2
1: Enable PWM0A signal output to P1.2

A6h.3 **TCOE:** System clock signal output (CKO) control
0: Disable System clock divided by 2 output to P1.4
1: Enable System clock divided by 2 output to P1.4

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDPIN	LCDPIN7	LCDPIN6	LCDPIN5	LCDPIN4	LCDPIN3	LCDPIN2	LCDPIN1	LCDPIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7 **LCDPIN7:** P3.2 (SEG17) LCD/LED mode enable
B3h.6 **LCDPIN6:** P3.1 (SEG16) LCD/LED mode enable
B3h.5 **LCDPIN5:** P3.0 (SEG15) LCD/LED mode enable
B3h.4 **LCDPIN4:** P1.0 (SEG14) LCD/LED mode enable
B3h.3 **LCDPIN3:** P1.1 (SEG13) LCD/LED mode enable
B3h.2 **LCDPIN2:** P1.2 (SEG12) LCD/LED mode enable
B3h.1 **LCDPIN1:** P1.3~P1.6 (SEG11~8) LCD/LED mode enable.
Note: SEG9 and Touch Key CLD share the same pin. If this bit is set, the Touch Key function would be affected.
B3h.0 **LCDPIN0:** P17, P3.6~P3.4 (SEG7~4) LCD/LED mode enable
0: I/O mode
1: LCD/LED mode

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	R/W	R/W	–	R/W	R/W	R/W	R/W	
Reset	0	0	–	0	0	0	1	1

D8h.7 **SCKTYPE:** Slow clock type. This bit can be changed only in Fast mode (SELFCK=1).
0: SRC, P2.1~P2.0 are I/O pins
1: SXT, P2.1~P2.0 are crystal pins

D8h.6 **FCKTYPE:** Fast clock type. This bit can be changed only in Slow mode (SELFCK=0).
0: FRC, P2.1~P2.0 are I/O pins
1: FXT, P2.1~P2.0 are crystal pins

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable, P1.7, P3.5, P3.6 are SPI functional pins.

BCh.3 **SSDIS:** SS pin disable
0: Enable SS pin, P3.4 is SPI chip selection input.
1: Disable SS pin

7.2 P3.7

P3.7 can be only used as Schmitt-trigger input or open-drain output, with pull-up resistor always enable. P3.7 pin is shared with RSTn, INT2 and Flash VPP function.

7.3 Port0 & P2.5~P2.2

These pins are shared with LCD/LED. If a Port0/P2.5~P2.2 pin is defined as I/O pin, it can be used as CMOS push-pull output or Schmitt-trigger input. The pin's pull up function is enable while SFR bit PxOE.n=0 and Px.n=1.

Port0, P2.5~P2.2 pin function	PxOE.n	Px.n SFR data	Pin State	Resistor Pull-up	Digital Input
Input	0	0	Hi-Z	N	Y
	0	1	Pull-up	Y	Y
CMOS Output	1	0	Drive Low	N	N
	1	1	Drive High	N	N

Port0, P2.5~P2.2 I/O Pin Function Table

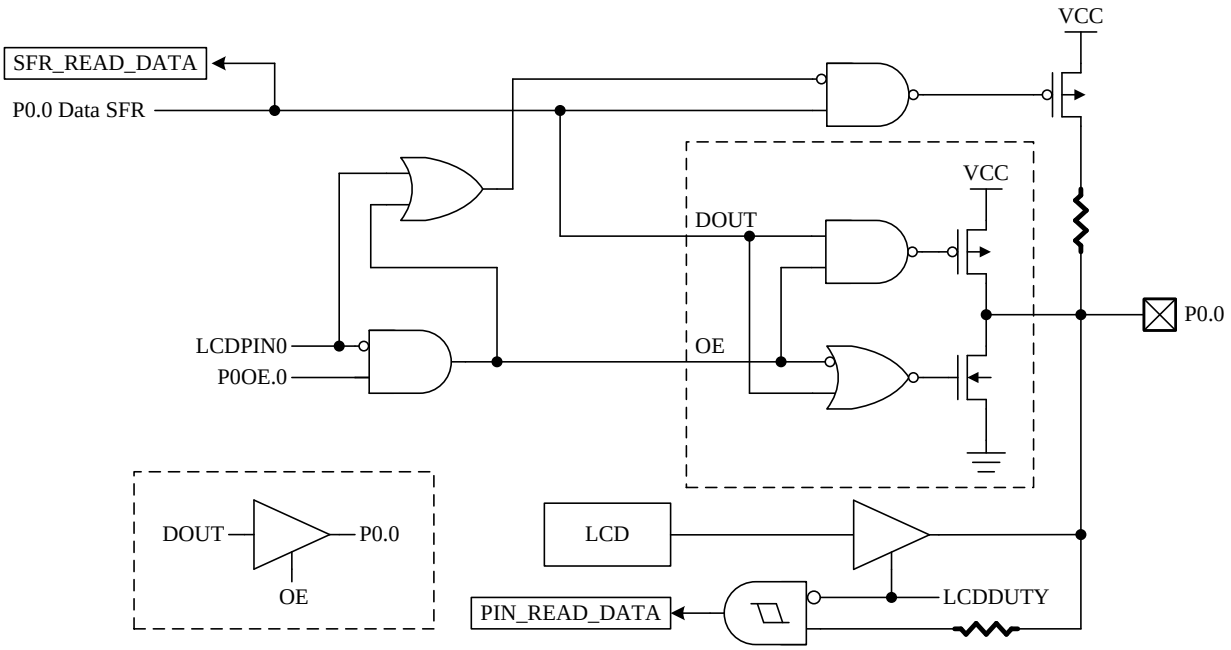
Pin Name	Wake-up	LCD/LED	Others
P0.0		COM3	
P0.1		COM2	
P0.2		COM1	
P0.3		COM0	
P0.4		SEG0	
P0.5		SEG1	
P0.6		SEG2	
P0.7		SEG3	
P2.2			PWM0B
P2.3			PWM1B
P2.4			
P2.5			
P3.7	Y		INT2, RSTn, VPP

Port0, P2.5~P2.2, P3.7 multi-function Table

The necessary SFR setting for Port0/Port2.5~P2.2 pin's alternative function is list below.

Alternative Function	PxOE.n	Px.n SFR data	Pin State	other necessary SFR setting
COM0~COM3	X	X	LCD/LED Waveform Output	LCDCON
SEG0~SEG3	X	X	LCD/LED Waveform Output	LCDCON
PWM0B, PWM1B	1	X	PWM Output (CMOS Push-Pull)	PINMOD

Mode Setting for Port0, P2.5~P2.2 Alternative Function Table



P0.0 Pin Structure

SFR **80h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

80h.7~0 **P0:** Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.

SFR **A0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

A0h.5~2 **P2.5~P2.2:** P2.5~P2.2 data, also controls the P2.n pin's pull-up function. If the P2.n SFR data is "1" and the corresponding P2OE.n=0 (input mode), the pull-up is enabled.

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7 **P3.7:** P3.7 data, also controls the P3.7 pin's I/O mode. If the P3.7 SFR data is "1", the P3.7 is assigned as Schmitt-trigger input mode; otherwise, it is assigned as open-drain output mode.

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P0OE	P0OE							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

91h.7~0 **P0OE:** Port0 CMOS Push-Pull output enable control
0: Disable
1: Enable

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P2MOD	P2OE				P2MOD1		P2MOD0	
R/W	R/W				R/W		R/W	
Reset	0	0	0	0	0	1	0	1

93h.7~4 **P2OE:** P2.5~P2.2 CMOS Push-Pull output enable control
0: Disable
1: Enable

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	PWM1BOE	PWM0AOE	PWM0BOE	TCOE	T2OE	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

A6h.6 **PWM1BOE:** PWM1B signal output enable
0: Disable PWM1B signal output to P2.3
1: Enable PWM1B signal output to P2.3

A6h.4 **PWM0BOE:** PWM0B signal output enable
0: Disable PWM0B signal output to P2.2
1: Enable PWM0B signal output to P2.2

SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON	LCDON	LCDDUTY	–	–	–	LCDBRIT		
R/W	R/W	R/W	–	–	–	R/W		
Reset	0	1	–	–	–	1	0	0

B1h.7 **LCDON:** LCD/LED enable bit
0: LCD/LED disable
1: LCD/LED enable, P0.7~P0.4 are LCD/LED Segment pins

B1h.6 **LCDDUTY:** LCD/LED duty select
0: 1/3 duty, P0.3~P0.1 are LCD/LED Common pins, P0.0 is I/O pin
1: 1/4 duty, P0.3~P0.0 are LCD/LED Common pins

8. Timers

Timer0, Timer1 and Timer2 are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the Chip's Timer0/1/2 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every "2 System clock" rate; in counter mode, T0/T1/T2 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function. The T0O pin can output the "Timer0 overflow divided by 64" signal, and the T2O pin can output the "Timer2 overflow divided by 2" signal. Timer3 is provided for a real-time clock count, when its time base is SXT.

8.1 Timer0/1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

Note: also refer to Section 6 for more information about Timer0/1 Interrupt enable and priority.
Note: also refer to Section 7 for more information about T0O pin output setting.

8.2 Timer2

Timer2 is controlled through the TCON2 register with the low and high bytes of Timer/Counter 2 stored in TL2 and TH2 and the low and high bytes of the Timer2 reload/capture registers stored in RCAP2L and RCAP2H.

SFR **C8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

C8h.7 **TF2:** Timer2 overflow flag
Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.

C8h.6 **EXF2:** T2EX interrupt pin falling edge flag
Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.

C8h.5 **RCLK:** UART receive clock control bit
0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3
1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3

C8h.4 **TCLK:** UART transmit clock control bit
0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3
1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3

C8h.3 **EXEN2:** T2EX pin enable
0: T2EX pin disable
1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK=TCLK=0

C8h.2 **TR2:** Timer2 run control
0: Timer2 stops
1: Timer2 runs

C8h.1 **CT2N:** Timer2 Counter/Timer select bit
0: Timer mode, Timer2 data increases at 2 System clock cycle rate
1: Counter mode, Timer2 data increases at T2 pin's negative edge

C8h.0 **CPRL2N:** Timer2 Capture/Reload control bit
0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1
1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1
If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow

SFR **CAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2L	RCP2L							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CAh.7~0 **RCP2L:** Timer2 reload/capture data low byte

SFR **CBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RCP2H	RCP2H							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CBh.7~0 **RCP2H:** Timer2 reload/capture data high byte

SFR **CCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL2	TL2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CCh.7~0 **TL2:** Timer2 data low byte

SFR **CDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH2	TH2							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

CDh.7~0 **TH2:** Timer2 data high byte

Note: also refer to Section 6 for more information about Timer2 Interrupt enable and priority.
Note: also refer to Section 7 for more information about T2O pin output setting.

8.3 Timer3

Timer3 of the Chip works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 32768, 16384, 8192, or 128 depending on the TM3PSC bits. The Timer3 clock source is Slow clock (SRC or SXT). This is ideal for real-time-clock (RTC) functionality when the clock source is SXT.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.1~0 **TM3PSC:** Timer3 interrupt rate control select
00: Interrupt rate is 32768 Slow clock cycle
01: Interrupt rate is 16384 Slow clock cycle
10: Interrupt rate is 8192 Slow clock cycle
11: Interrupt rate is 128 Slow clock cycle

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.0 **TF3:** Timer 3 interrupt flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit. (***Note2***)

Note2: S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

F8h.6 **CLRTM3:** Set to clear Timer3, H/W auto clear it at next clock cycle

Note: also refer to Section 6 for more information about Timer3 Interrupt enable and priority.

8.4 T0O and T2O Output Control

This device can generate various frequency waveform pin output (in CMOS or Open-Drain format) for Buzzer. The T0O and T2O waveform is divided by Timer0/Timer2 overflow signal. The T0O waveform is Timer0 overflow divided by 64, and T2O waveform is Timer2 overflow divided by 2. User can control their frequency by Timers auto reload speed. Set T0OE and T2OE SFRs can output these waveforms.

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	PWM1BOE	PWM0AOE	PWM0BOE	TCOE	T2OE	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

A6h.2 **T2OE:** Timer2 signal output (T2O) control
0: Disable Timer2 overflow divided by 2 output to P1.0
1: Enable Timer2 overflow divided by 2 output to P1.0

SFR **A5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MODH	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
R/W	R/W	–	R/W		R/W		R/W	
Reset	0	–	0	0	0	0	0	0

A5h.7 **T0OE:** Timer0 signal output (T0O) control
0: Disable Timer0 overflow divided by 64 output to P3.4
1: Enable Timer0 overflow divided by 64 output to P3.4

9. UART

The UART uses SCON and SBUF SFRs. SCON is the control register, SBUF is the data register. Data is written to SBUF for transmission and SBUF is read to obtain received data. The received data and transmitted data registers are completely independent. In addition to standard 8051's full duplex mode, this Chip also provides one wire mode. If the UART1W bit is set, both transmit and receive data use P3.1 pin.

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.7 **SMOD:** UART double baud rate control bit
0: Disable UART double baud rate
1: Enable UART double baud rate

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.7 **UART1W:** One wire UART mode enable, both TXD/RXD use P3.1 pin
0: Disable one wire UART mode
1: Enable one wire UART mode

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** Serial port mode select bit 0,1
00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2
01: Mode1: 8 bit UART, Baud Rate is variable
10: Mode2: 9 bit UART, Baud Rate=F_{SYSCLK}/32 or /64
11: Mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

F_{SYSCLK} denotes System clock frequency.

- Mode 0:
  Baud Rate=$F_{SYSCLK}/2$
- Mode 1, 3: if using Timer1 auto reload mode
  Baud Rate= (SMOD+1) xF_{SYSCLK}/ (32x2x (256–TH1))
- Mode 1, 3: if using Timer2
  Baud Rate=Timer2 overflow rate/16=F_{SYSCLK}/ (32x (65536–RCP2H, RCP2L))
- Mode 2:
  Baud Rate= (SMOD+1) x$F_{SYSCLK}/64$

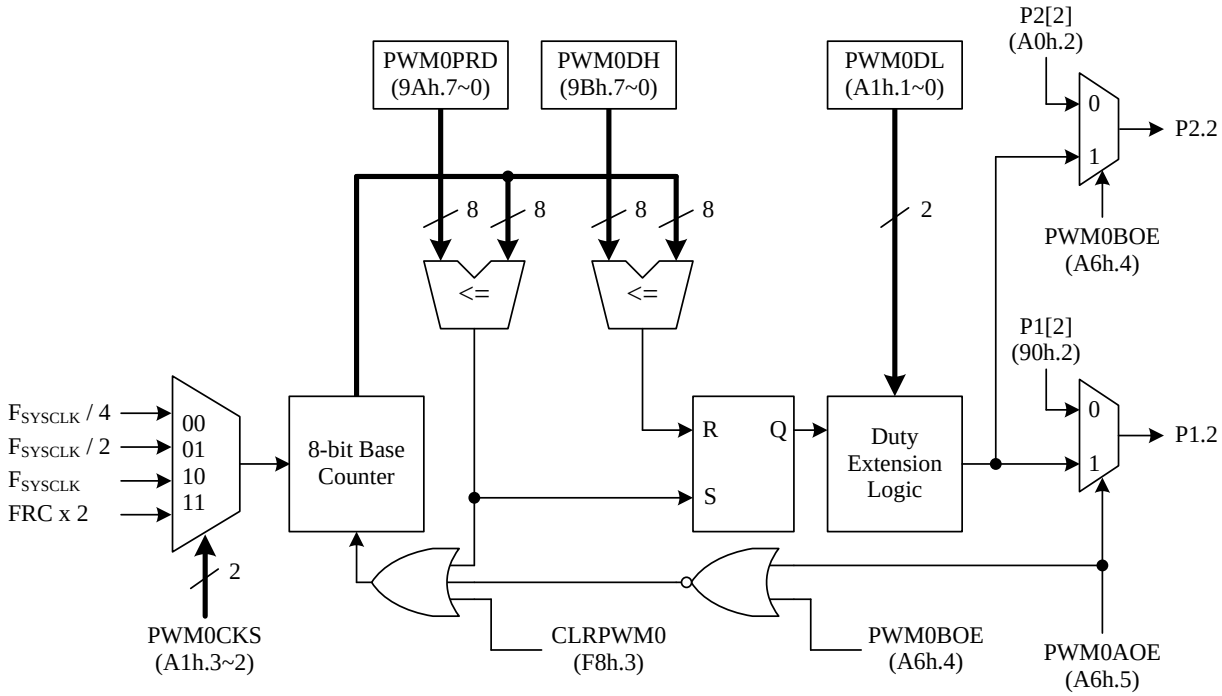
Note: also refer to Section 6 for more information about UART Interrupt enable and priority.
Note: also refer to Section 8 for more information about how Timer2 controls UART clock.

10. PWMs

The Chip has two independent PWM modules, PWM0 and PWM1. Each PWM module's waveform signal can output to two different pins. For example, user can select PWM0 output to P1.2 pin (PWM0A) or P2.2 pin (PWM0B) by PINMOD SFR setting. The PWM can generate a fixed frequency waveform with 1024 duty resolution on the basis of the PWM clock. The PWM clock can select FRC double frequency (FRCx2) or F_{SYSCLK} divided by 1, 2, or 4 as its clock source. A spread LSB technique allows PWM to run its frequency at the "PWM clock divided by 256" instead of at the "PWM clock divided by 1024", which means the PWM is four times faster than normal. The advantage of a higher PWM frequency is that the post RC filter can transform the PWM signal to a more stable DC voltage level.

The PWM output signal resets to a low level whenever the 8-bit base counter matches the 8-bit MSB of the PWM duty register. When the base counter rolls over, the 2-bit LSB of the PWM duty register decides whether to set the PWM output signal high immediately or set it high after one clock cycle delay. The PWM period can be set by writing the period value to the 8-bit PWM period register.

The pin mode SFR controls the PWM output waveform format. Mode1 makes the PWM open drain output and Mode2 makes the PWM CMOS push-pull output. (***see section 7***)



PWM Structure

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ah.7~0 **PWM0PRD:** PWM0 8-bit period register

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Bh.7~0 **PWM0DH:** bits 9~2 of the PWM0 10-bit duty register

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

9Ch.7~0 **PWM1PRD:** PWM1 8-bit period register

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

9Dh.7~0 **PWM1DH:** bits 9~2 of the PWM1 10-bit duty register

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
R/W	R/W		R/W		R/W		R/W	
Reset	1	0	0	0	1	0	0	0

A1h.7~6 **PWM1CKS:** PWM1 clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRCx2

A1h.5~4 **PWM1DL:** bits 1~0 of the PWM1 10-bit duty register

A1h.3~2 **PWM0CKS:** PWM0 clock source
00: $F_{SYSCLK}/4$
01: $F_{SYSCLK}/2$
10: F_{SYSCLK}
11: FRCx2

A1h.1~0 **PWM0DL:** bits 1~0 of the PWM0 10-bit duty register

SFR **A6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PINMOD	PWM1AOE	PWM1BOE	PWM0AOE	PWM0BOE	TCOE	T2OE	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

A6h.7 **PWM1AOE:** PWM1A signal output enable
0: Disable PWM1A signal output to P1.3
1: Enable PWM1A signal output to P1.3

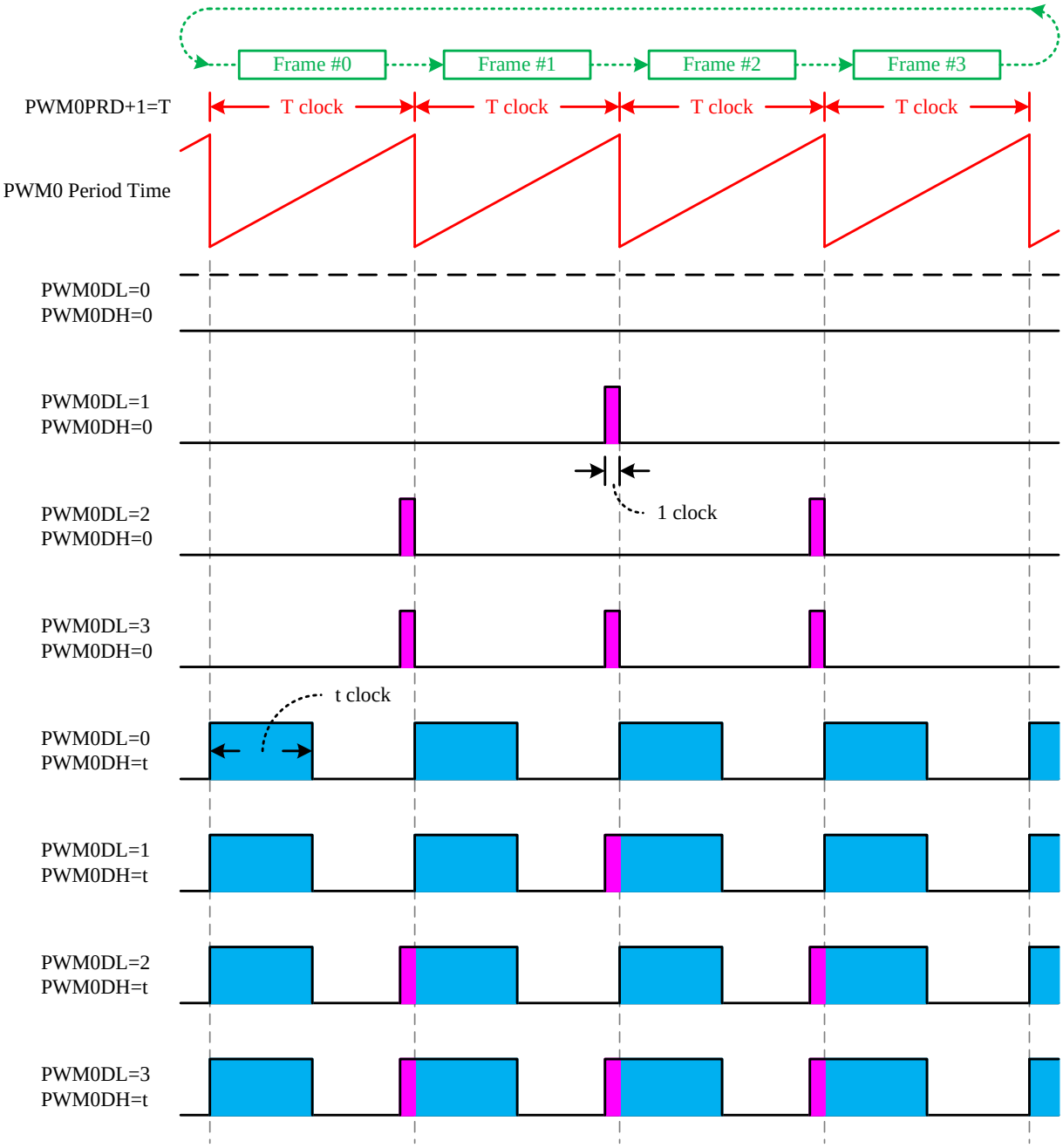
A6h.6 **PWM1BOE:** PWM1B signal output enable (PWM1A and PWM1B signals are identical)
0: Disable PWM1B signal output to P2.3
1: Enable PWM1B signal output to P2.3

A6h.5 **PWM0AOE:** PWM0A signal output enable
0: Disable PWM0A signal output to P1.2
1: Enable PWM0A signal output to P1.2

A6h.4 **PWM0BOE:** PWM0B signal output enable (PWM0A and PWM0B signals are identical)
0: Disable PWM0B signal output to P2.2
1: Enable PWM0B signal output to P2.2

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

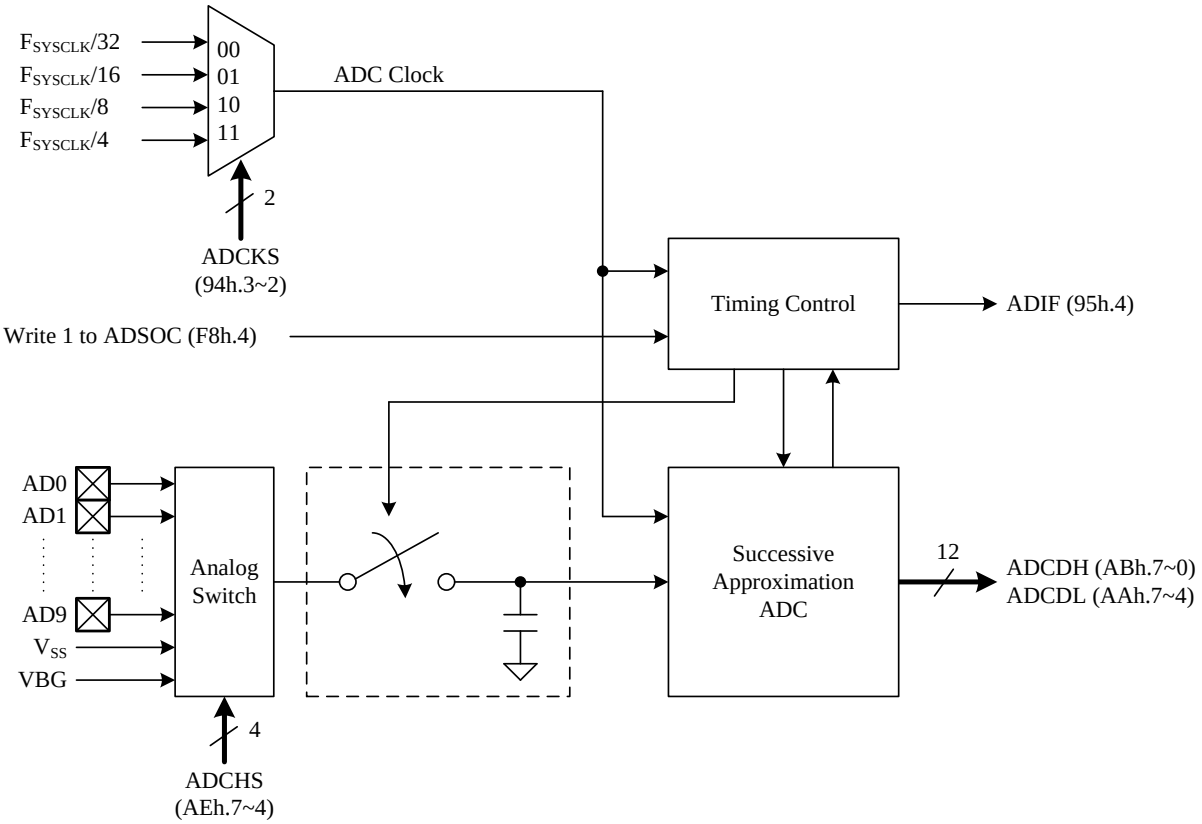
F8h.3 **CLRPWM0:** PWM0 clear enable
0: PWM0 is running
1: PWM0 is cleared and held



PWM Waveform

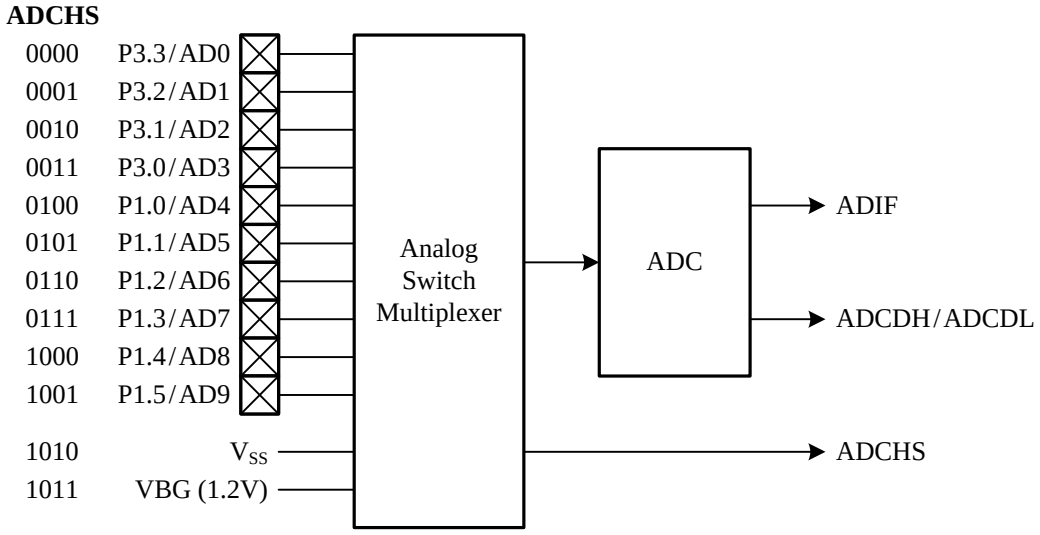
11. ADC

The Chip offers a 12-bit ADC consisting of a 12-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register. To use the ADC, set the ADCKS bit first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit. Because certain channels are shared with the Touch Key, the ADC channel must be configured differently from the Touch Key channel to avoid affecting the channel input sensitivity. The analog input level must remain within the range from V_{SS} to V_{CC}.



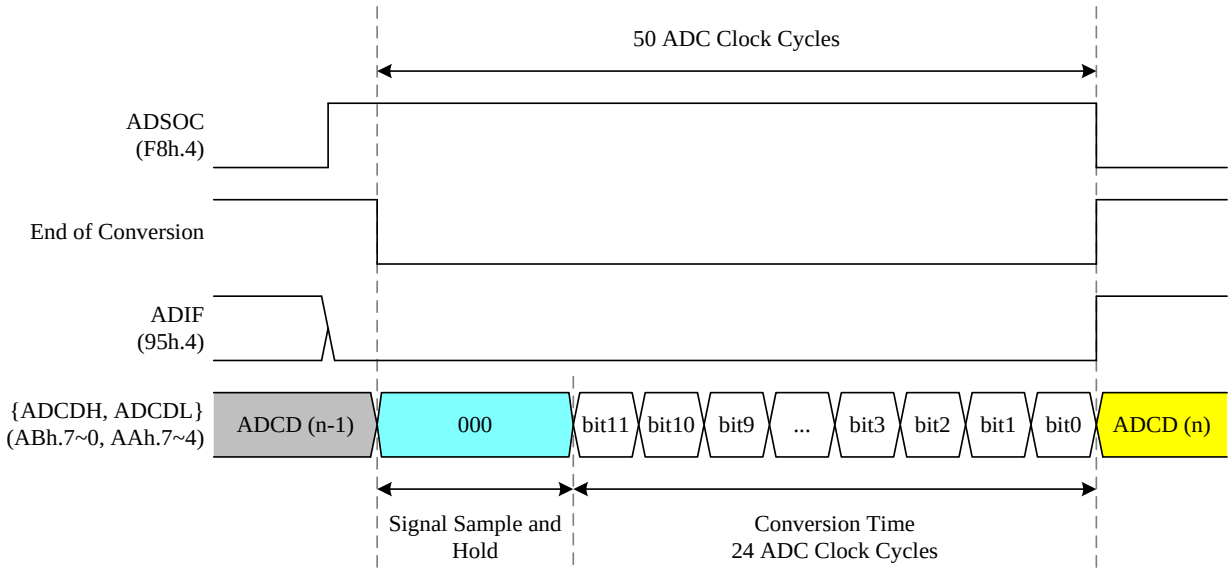
11.1 ADC Channels

The 12-bit ADC has a total of 12 channels, designated AD0~AD9, V_{SS}, and VBG. The ADC channels are connected to the analog input pins via the analog switch multiplexer. The analog switch multiplexer is controlled by the ADCHS register. The Chip offers up to 10 analog input pins, designated AD0~AD9. In addition, there are two analog input pins for voltage reference connections. When ADCHS is set to 1010b, the analog input will connect to V_{SS}, and when ADCHS is set to 1011b, the analog input will connect to VBG. VBG is an internal voltage reference at 1.2V.



11.2 ADC Conversion Time

The conversion time is the time required for the ADC to convert the voltage. The ADC requires two ADC clock cycles to convert each bit and several clock cycles to sample and hold the input voltage. A total of 50 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
R/W	R/W	R/W	R/W		R/W		R/W	
Reset	0	0	0	0	0	0	0	0

94h.3~2 **ADCKS:** ADC clock rate select
00: $F_{SYSCLK}/32$
01: $F_{SYSCLK}/16$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/4$

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.4 **ADIF:** ADC interrupt flag
Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				TKEOC	TKOVF	TKDH	
R/W	R				R	R	R	
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				TKCHS			
R/W	R/W				R/W			
Reset	1	1	1	1	1	1	1	1

AEh.7~4 **ADCHS:** ADC channel select
0000: ADC0 (P3.3)
0001: ADC1 (P3.2)
0010: ADC2 (P3.1)
0011: ADC3 (P3.0)
0100: ADC4 (P1.0)
0101: ADC5 (P1.1)
0110: ADC6 (P1.2)
0111: ADC7 (P1.3)
1000: ADC8 (P1.4)
1001: ADC9 (P1.5)
1010: V_{SS}
1011: VBG (internal reference voltage)
11xx: Undefined

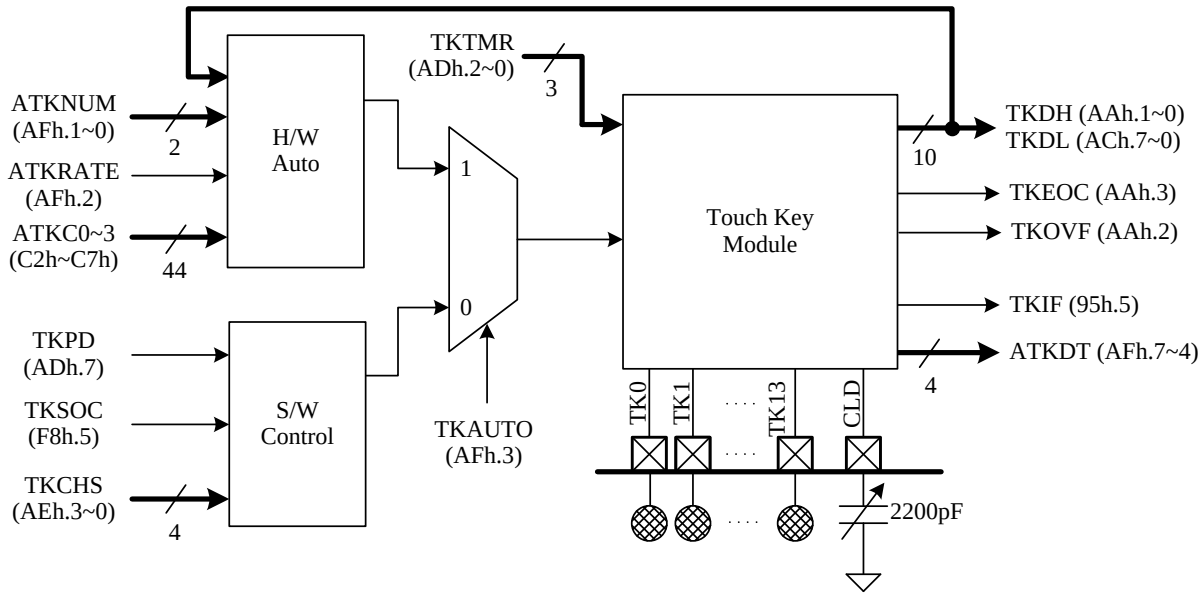
SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

F8h.4 **ADSOC:** Start ADC conversion
Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: also refer to Section 6 for more information about ADC Interrupt enable and priority.
Note: also refer to Section 7 for more information about ADC pin input setting.

12. Touch Key

The Touch Key offers an easy, simple and reliable method to implement finger touch detection. During the key scan operation, it only requires an external capacitor component on CLD pin. The device support 14 channels touch key detection with S/W manual mode and H/W Auto Mode (ATK). Only one mode can be active at a time.



Touch Key Structure

To use the Touch Key, user must setup the pin mode correctly as below table. Setting Mode0 for an Idling Touch Key pin can pull up the pin and reduce the Key's mutual interference. While a TK pin is under scanning, user must set the pin to Mode3 to disable the pull up resistor.

P1MODx/P3MODx setting for Touch Key	TK0~TK3	TK4~TK8	TK9~TK13	CLD
Pin is not Touch Key	Mode0/1/2/3	Mode0/1/2/3	Mode0/1/2	Mode0/1/2/3
Pin is Touch Key, Idling	Mode0	Mode0	Mode0	Mode3
Pin is Touch Key, S/W Scanning	Mode3	Mode3	Mode3	Mode3
Pin is Touch Key, H/W Auto Scan (ATK)	Mode0	–	–	Mode3

S/W Manual Mode Touch Key Detection

All Touch Key (TK0~TK13) can be used for S/W manual mode. To start the S/W mode, user assigns TKAUTO=0 and TKPD=0, then set the TKSOC bit to start touch key conversion, the TKSOC bit can be automatically cleared while end of conversion. However, if the SYSCLK is too slow, H/W might fail to clear TKSOC due to clock sampling rate. TKEOC=0 means conversion is in process. TKEOC=1 means the conversion is finish, and the touch key counting result is stored into the 10 bits TK Data Counter TKDH and TKDL. After TKEOC=1, user must wait at least 10 μs for next conversion. If TKOVF=1, means the conversion transaction exceeds period time. Reduce/Increase TKTMR can reduce/increase TK Data Count to adapt the system board circumstances.

The Touch Key unit has an internal built-in reference capacitor to simulate the KEY behavior. Set TKCHS=15 and start the S/W scan mode can get the TK Data Count of this capacitor. Since the internal capacitor would not be affected by water or mobile phone, it is useful for comparing the environment background noise.

H/W Auto Touch Key Detection (ATK)

Only TK0~TK3 are eligible for H/W auto mode. This function can work in Fast/Slow/Idle mode and save the S/W effort as well as minimize the Chip current consumption. To use this function, user need to set TKAUTO=1 and TKPD=1 to enable H/W fully control the TK unit. H/W then automatically detects the TK0~TK3's TK Data Count at every 2048 or 4096 Slow clock cycles. If a Key's TK Data Count is less than the pre-set compare threshold (ATKC0~3), H/W generates interrupt and wake up CPU. User can switch the TK module back to S/W Manual Mode after the TK interrupt and identify/confirm the Key touch event.

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVD	–	TKIF	ADIF	–	IE2	P1IF	TF3
R/W	R	–	R/W	R/W	–	R/W	R/W	R/W
Reset	–	–	0	0	–	0	0	0

95h.5 **TKIF:** Touch Key interrupt flag
In the S/W Manual mode: Set by H/W at the end of conversion. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag.
In the ATK mode: Set by H/W when a TK channel's touch event is detected. It is cleared automatically when the program performs the interrupt service routine. S/W can write DFh to INTFLG to clear this bit.
Note: In ATK mode, this flag may be cleared improperly by ADC module. User should not start the ADC conversion in ATK mode.

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADTKDT	ADCDL				TKEOC	TKOVF	TKDH	
R/W	R				R	R	R	
Reset	–	–	–	–	–	–	–	–

AAh.3 **TKEOC:** Touch Key end of conversion flag, TKEOC may have 3uS delay after TKSOC=1, so F/W must wait enough time before polling this Flag.
0: Indicates conversion is in progress
1: Indicates conversion is finished

AAh.2 **TKOVF:** Touch Key counter overflow
0: Indicates that the counter has not overflow
1: Indicates that the counter has overflow

AAh.1~0 **TKDH:** Touch Key counter data bit 9~8

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKDL	TKDL							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ACh.7~0 **TKDL:** Touch Key counter data bit 7~0

SFR **ADh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON	TKPD	–	–	–	–	TKTMR		
R/W	R/W	–	–	–	–	R/W		
Reset	1	–	–	–	–	1	0	0

ADh.7 **TKPD:** Touch Key power down
0: Touch Key running
1: Touch Key power down

ADh.2~0 **TKTMR:** Touch Key conversion time select
TKTMR adjusts the value of Touch Key reference voltage. A larger value of TKTMR requires a longer charging time, which can affect the sensitivity of touch sensing.
000: Conversion time shortest
…
111: Conversion time longest

SFR **AEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CHSEL	ADCHS				TKCHS			
R/W	R/W				R/W			
Reset	1	1	1	1	1	1	1	1

AEh.3~0 **TKCHS:** Touch Key channel select
0000: TK0 (P1.0)
0001: TK1 (P1.1)
0010: TK2 (P1.2)
0011: TK3 (P1.3)
0100: TK4 (P3.3)
0101: TK5 (P3.2)
0110: TK6 (P3.1)
0111: TK7 (P3.0)
1000: TK8 (P1.4)
1001: TK9 (P1.6)
1010: TK10 (P1.7)
1011: TK11 (P3.6)
1100: TK12 (P3.5)
1101: TK13 (P3.4)
1110: Undefined
1111: Internal reference capacitor

SFR **AFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TKCON2	ATKDT				TKAUTO	ATKRATE	ATKNUM	
R/W	R				R/W	R/W	R/W	
Reset	–	–	–	–	0	0	1	1

AFh.7~4 **ATKDT:** Touch Key Auto Scan Result (for H/W ATK Mode)
xxx1: TK0 has a Touch event
xx1x: TK1 has a Touch event
x1xx: TK2 has a Touch event
1xxx: TK3 has a Touch event
AFh.3 **TKAUTO:** Touch Key Auto Scan Mode Enable
0: S/W Mode
1: H/W ATK Mode
AFh.2 **ATKRATE:** Touch Key Scan Rate (for H/W ATK Mode)
0: ATK scan rate at every 4096 Slow clock cycles
1: ATK scan rate at every 2048 Slow clock cycles
AFh.1~0 **ATKNUM:** Touch Key Auto Scan Channel Number (for H/W ATK Mode)
00: ATK only detect TK0
01: ATK detect TK0 and TK1
10: ATK detect TK0~TK2
11: ATK detect TK0~TK3

SFR **C2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC10H	–	ATKC1H			–	ATKC0H		
R/W	–	R/W			–	R/W		
Reset	–	0	0	0	–	0	0	0

C2h.6~4 **ATKC1H:** Data Threshold bit 10~8 Compared with TK1 scan (for H/W ATK Mode)
C2h.2~0 **ATKC0H:** Data Threshold bit 10~8 Compared with TK0 scan (for H/W ATK Mode)

SFR **C3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC32H	–	ATKC3H			–	ATKC2H		
R/W	–	R/W			–	R/W		
Reset	–	0	0	0	–	0	0	0

C3h.6~4 **ATKC3H:** Data Threshold bit 10~8 Compared with TK3 scan (for H/W ATK Mode)
C3h.2~0 **ATKC2H:** Data Threshold bit 10~8 Compared with TK2 scan (for H/W ATK Mode)

SFR **C4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC0L	ATKC0L							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C4h.7~0 **ATKC0L:** Data Threshold bit 7~0 Compared with TK0 scan (for H/W ATK Mode)

SFR **C5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC1L	ATKC1L							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C5h.7~0 **ATKC1L:** Data Threshold bit 7~0 Compared with TK1 scan (for H/W ATK Mode)

SFR **C6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC2L	ATKC2L							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C6h.7~0 **ATKC2L:** Data Threshold bit 7~0 Compared with TK2 scan (for H/W ATK Mode)

SFR **C7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ATKC3L	ATKC3L							
R/W	R/W							
Reset	0	1	0	0	0	0	0	0

C7h.7~0 **ATKC3L:** Data Threshold bit 7~0 Compared with TK3 scan (for H/W ATK Mode)

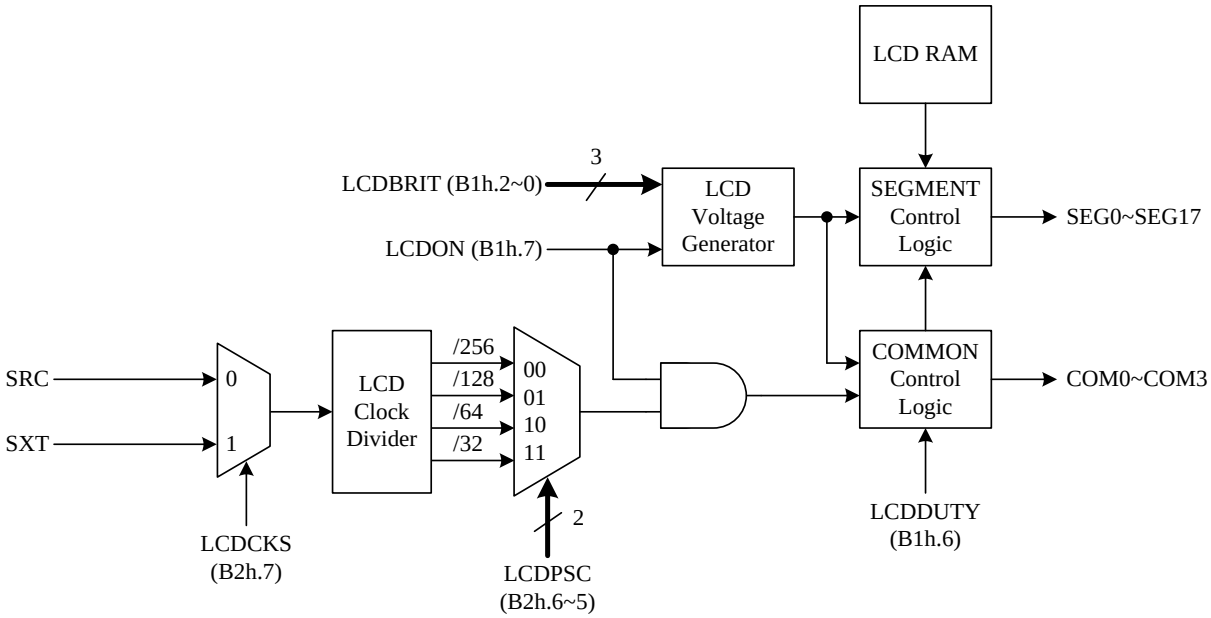
SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	–	–	R/W
Reset	0	0	0	0	0	–	–	0

F8h.5 **TKSOC:** Start Touch Key conversion
Set the TKSOC bit to start Touch Key conversion, and the TKSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.

Note: also refer to Section 6 for more information about Touch Key Interrupt enable and priority.
Note: also refer to Section 7 for more information about Touch Key pin input setting.

13. LCD Controller/Driver

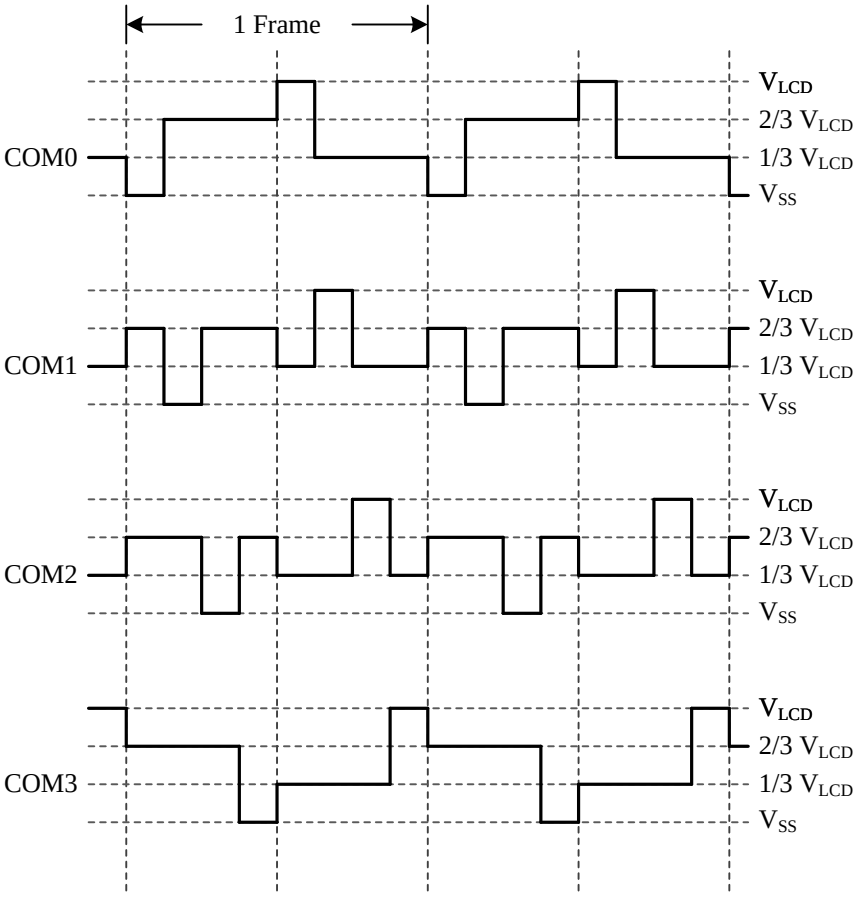
The Chip supports an LCD controller and driver. The LCD driver is capable of driving the LCD panel with 72 dots by 4 Commons and 18 Segments. It is capable of driving 1/3 bias. The LCD clock source is generated from SRC or SXT depends on LCDCKS bit. The clock rate can be divided by 32, 64, 128, and 256 by the LCDPSC bits. If SRC is the LCD clock source, the V_{CC} voltage level would affect the SRC frequency and LCD frame rate. The LCDRAM is located in the 8051's External Data Memory space, addressing from F000h to F008h.



LCD RAM (External Data Memory)

Addr.	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
F000h	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0
F001h	SEG3	SEG3	SEG3	SEG3	SEG2	SEG2	SEG2	SEG2
F002h	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4
F003h	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6
F004h	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8
F005h	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10
F006h	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12
F007h	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14
F008h	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16

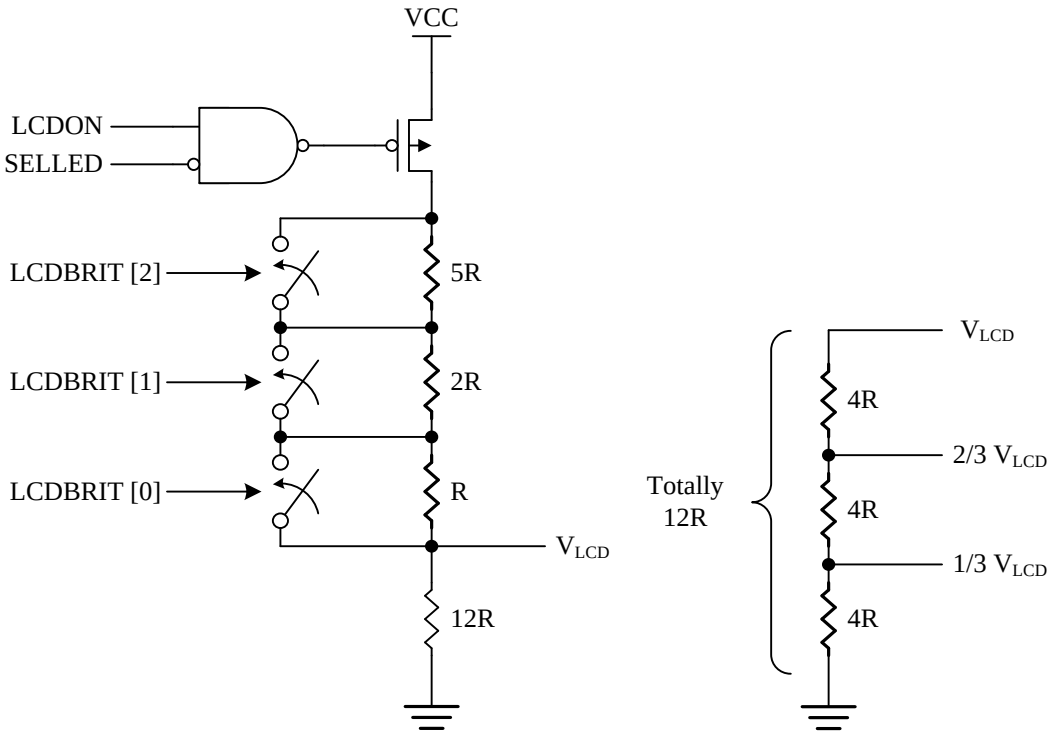
The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



The frame rate table for each lighting system is shown below.

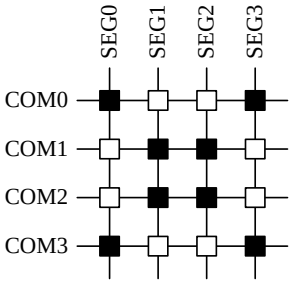
LCDCKS (B2h.7)	LCDPSC (B2h.6~5)	LCD Frame Rate (Hz)	
		LCDDUTY (B1h.6)	
		0 (1/3 duty)	1 (1/4 duty)
0 (SRC) 24000 Hz	00 (/256)	15.63	11.72
	01 (/128)	31.25	23.44
	10 (/64)	62.5	46.88
	11 (/32)	125	93.75
1 (SXT) 32768 Hz	00 (/256)	21.33	16.00
	01 (/128)	42.67	32.00
	10 (/64)	85.33	64.00
	11 (/32)	170.67	128.00

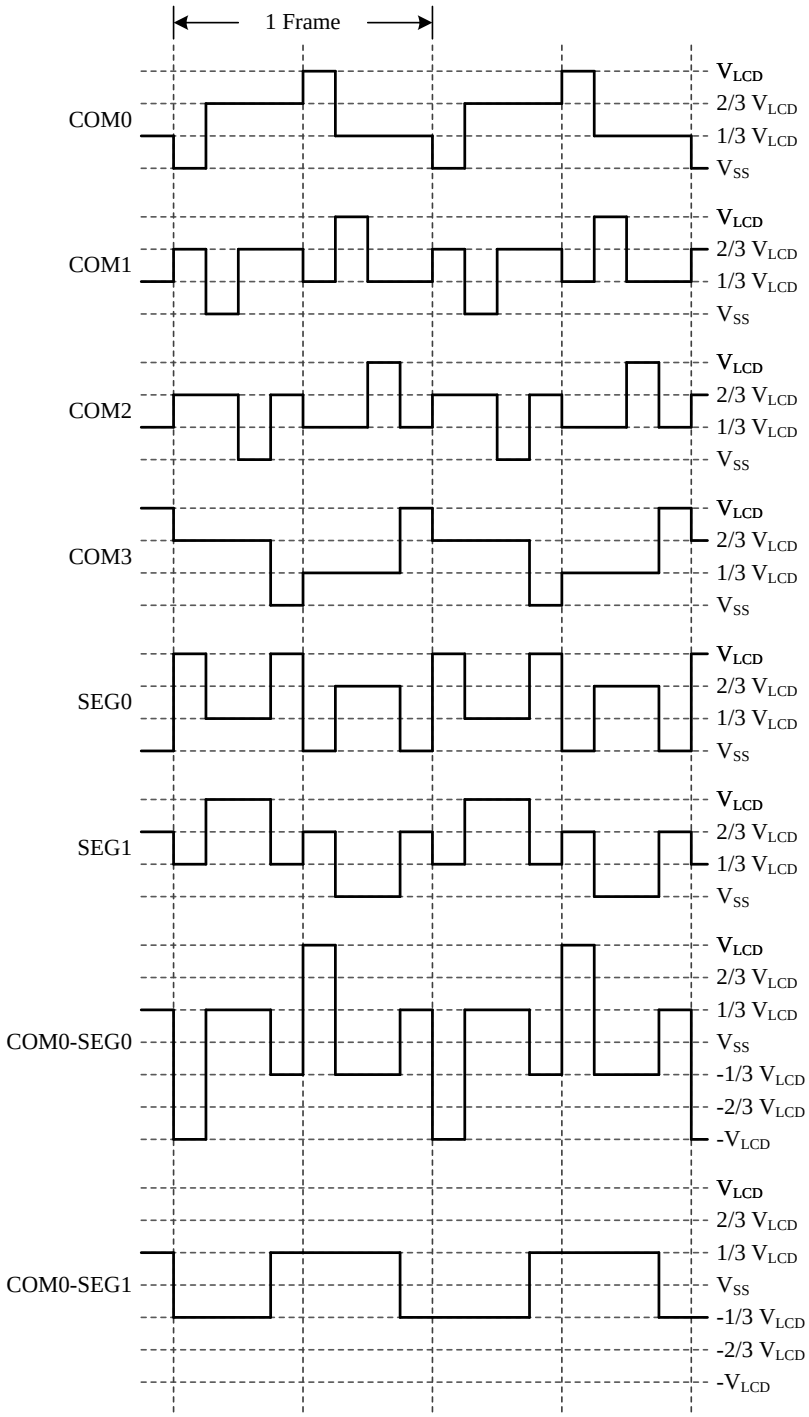
The following figure of the LCD voltage generator shows the internal voltage generator composed by resistors. LCDON and SELLED control the current flows from V_{CC} to ground. If LCDON=0 or SELLED=1, the PMOS will turn off the path so that all LCD voltages will be 0 V. If LCDON=1 and SELLED=0, the resistor divider will work to generate multi voltages to provide the LCD control module for generating the desired waveforms. The LCDBRIT control bits will open/short the switches to determine V_{LCD}. The table below shows V_{LCD} corresponding to LCDBRIT. The voltage divider circuit will consume current because the DC path is always on when LCDON=1 and SELLED=0.



LCDBRIT	V_{LCD}
000	(12/20) x V_{CC}
001	(12/19) x V_{CC}
010	(12/18) x V_{CC}
011	(12/17) x V_{CC}
100	(12/15) x V_{CC}
101	(12/14) x V_{CCc}
110	(12/13) x V_{CC}
111	V_{CC}

1/4 Duty, 1/3 Bias Output Waveform





SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON	LCDON	LCDDUTY	–	–	–	LCDBRIT		
R/W	R/W	R/W	–	–	–	R/W		
Reset	0	1	–	–	–	1	0	0

B1h.7 **LCDON:** LCD/LED enable bit
0: LCD/LED disable
1: LCD/LED enable

B1h.6 **LCDDUTY:** LCD/LED duty select
0: 1/3 duty
1: 1/4 duty

B1h.2~0 **LCDBRIT:** LCD brightness select
000: (12/20) x V_{CC}
001: (12/19) x V_{CC}
010: (12/18) x V_{CC}
011: (12/17) x V_{CC}
100: (12/15) x V_{CC}
101: (12/14) x V_{CC}
110: (12/13) x V_{CC}
111: V_{CC}

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON2	LCDCKS	LCDPSC		SELLED	LEDPOL	LEDDTE	–	–
R/W	R/W	R/W		R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

B2h.7 **LCDCKS:** LCD/LED clock source select
0: SRC
1: SXT

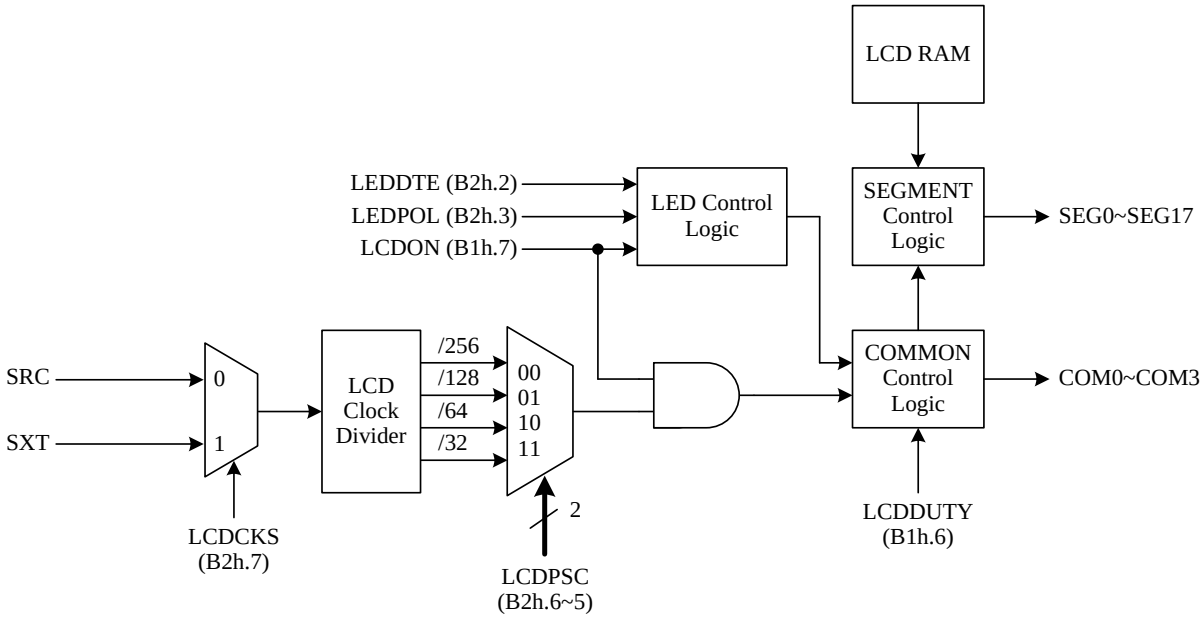
B2h.6~5 **LCDPSC:** LCD/LED clock prescaler select
00: LCD/LED clock is divided by 256
01: LCD/LED clock is divided by 128
10: LCD/LED clock is divided by 64
11: LCD/LED clock is divided by 32

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDPIN	LCDPIN7	LCDPIN6	LCDPIN5	LCDPIN4	LCDPIN3	LCDPIN2	LCDPIN1	LCDPIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

B3h.7 **LCDPIN7:** P3.2 (SEG17) LCD/LED mode enable
B3h.6 **LCDPIN6:** P3.1 (SEG16) LCD/LED mode enable
B3h.5 **LCDPIN5:** P3.0 (SEG15) LCD/LED mode enable
B3h.4 **LCDPIN4:** P1.0 (SEG14) LCD/LED mode enable
B3h.3 **LCDPIN3:** P1.1 (SEG13) LCD/LED mode enable
B3h.2 **LCDPIN2:** P1.2 (SEG12) LCD/LED mode enable
B3h.1 **LCDPIN1:** P1.3~P1.6 (SEG11~8) LCD/LED mode enable
Note: SEG9 and Touch Key CLD share the same pin. If this bit is set, the Touch Key function would be affected.
B3h.0 **LCDPIN0:** P17, P3.6~P3.4 (SEG7~4) LCD/LED mode enable
0: I/O mode
1: LCD/LED mode

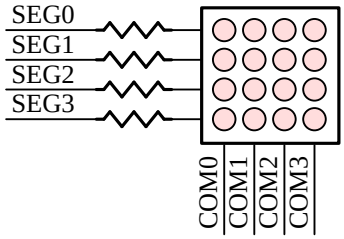
14. LED Controller/Driver

The Chip supports an LED controller and driver. If the LED mode option SELLED is set, The Chip will switch the LCD driver to the LED driver. It provides 18 Segment pins and 4 Common pins to drive an LED module with 72 pixels. The LED and LCD module share the same clock source and LCDRAM. For LED application, the COM pins have a high sink current, which can drive an LED directly. Besides, the LED provides COM pin polarity and dead time options, by setting the LEDPOL bit and the LEDDTE bit respectively.

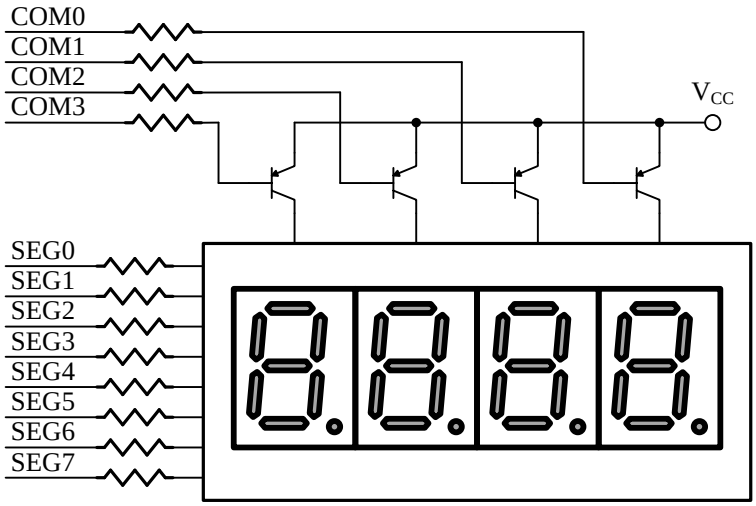


Application Circuit

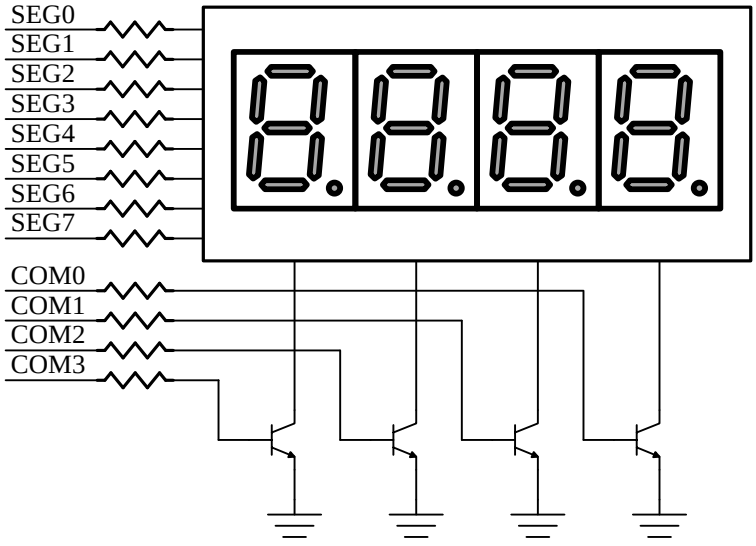
COM Active Low and SEG Active High



COM Active Low and SEG Active Low

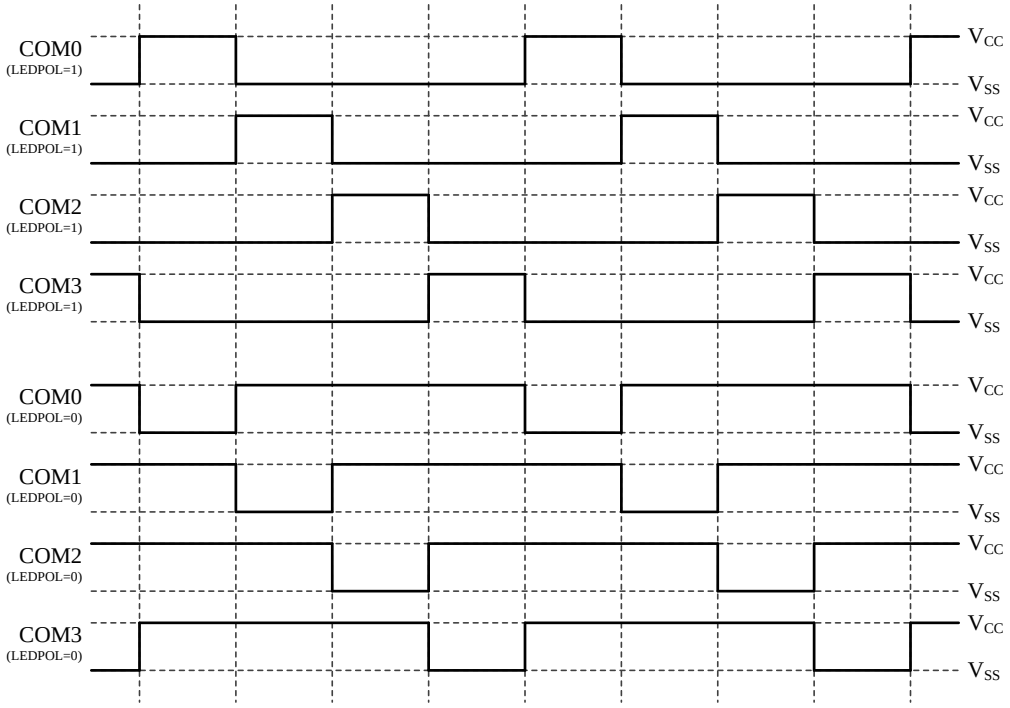


COM Active High and SEG Active High

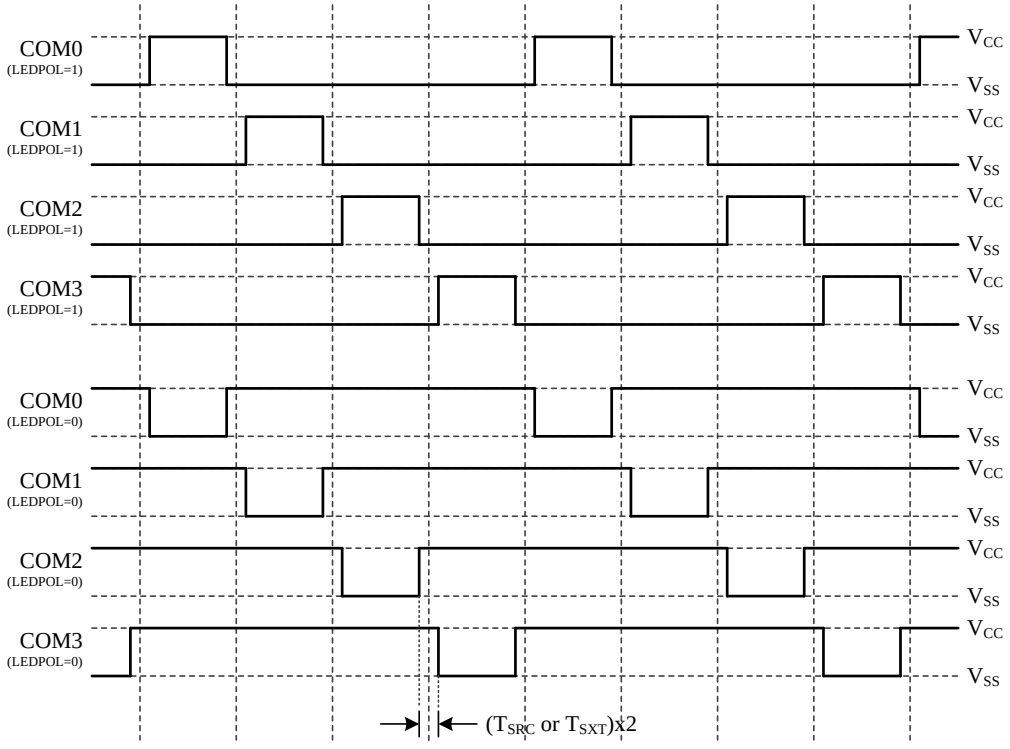


To avoid LED flicker when the common signal is changing, the Chip provides a dead time option. Setting the SELLED bit selects the LED mode, and setting the LEDDTE bit enables the dead time. In the dead time period, a common pin will output a short inactive signal instead of changing the signal immediately.

1/4 Duty, LEDDTE=0



1/4 Duty, LEDDTE=1



SFR **B1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON	LCDON	LCDDUTY	–	–	–	LCDBRIT		
R/W	R/W	R/W	–	–	–	R/W		
Reset	0	1	–	–	–	1	0	0

B1h.7 **LCDON:** LCD/LED enable bit
0: LCD/LED disable
1: LCD/LED enable

SFR **B2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCON2	LCDCKS	LCDPSC		SELLED	LEDPOL	LEDDTE	–	–
R/W	R/W	R/W		R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

B2h.7 **LCDCKS:** LCD/LED clock source select
0: SRC
1: SXT

B2h.6~5 **LCDPSC:** LCD/LED clock prescaler select
00: LCD/LED clock is divided by 256
01: LCD/LED clock is divided by 128
10: LCD/LED clock is divided by 64
11: LCD/LED clock is divided by 32

B2h.4 **SELLED:** LED select mode
0: LCD mode
1: LED mode

B2h.3 **LEDPOL:** LED COM polarity select
0: Active low (with high sink)
1: Active high

B2h.2 **LEDDTE:** LED COM dead time enable
0: LED COM dead time disable
1: LED COM dead time enable

SFR **B3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDPIN	LCDPIN7	LCDPIN6	LCDPIN5	LCDPIN4	LCDPIN3	LCDPIN2	LCDPIN1	LCDPIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

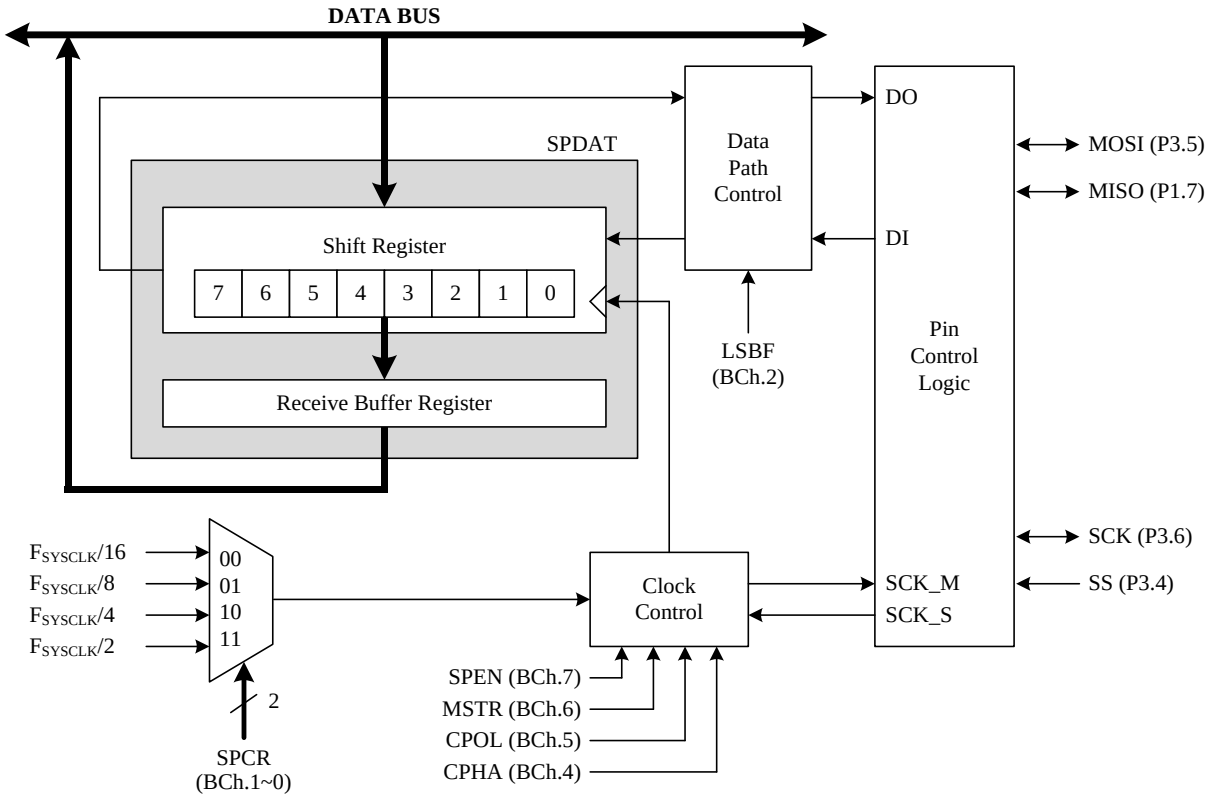
B3h.7 **LCDPIN7:** P3.2 (SEG17) LCD/LED mode enable
B3h.6 **LCDPIN6:** P3.1 (SEG16) LCD/LED mode enable
B3h.5 **LCDPIN5:** P3.0 (SEG15) LCD/LED mode enable
B3h.4 **LCDPIN4:** P1.0 (SEG14) LCD/LED mode enable
B3h.3 **LCDPIN3:** P1.1 (SEG13) LCD/LED mode enable
B3h.2 **LCDPIN2:** P1.2 (SEG12) LCD/LED mode enable
B3h.1 **LCDPIN1:** P1.3~P1.6 (SEG11~8) LCD/LED mode enable
Note: SEG9 and Touch Key CLD share the same pin. If this bit is set, the Touch Key function would be affected.
B3h.0 **LCDPIN0:** P17, P3.6~P3.4 (SEG7~4) LCD/LED mode enable
0: I/O mode
1: LCD/LED mode

15. Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) module is capable of full-duplex, synchronous, serial communication between the MCU and peripheral devices. The peripheral devices can be other MCUs, A/D converter, sensors, or flash memory, etc. The SPI runs at a clock rate up to the system clock divided by two. Firmware can read the status flags, or the operation can be interrupt driven. Following figure shows the SPI system block diagram.

The features of the SPI module include:

- Master or Slave mode operation
- 3-wire or 4-wire mode operation
- Full-duplex operation
- Programmable transmit bit rate
- Single buffer receive
- Serial clock phase and polarity options
- MSB-first or LSB-first shifting selectable



The four signals used by SPI are described below. The MOSI (P3.5) signal is an output from a Master Device and an input to Slave Devices. The MISO (P1.7) signal is an output from a Slave Device and an input to a Master Device. Data is transferred most-significant bit (MSB) or least-significant bit (LSB) first by setting the LSBF bit. The SCK (P3.6) signal is an output from a Master Device and an input to Slave Devices. It is used to synchronize the data on the MOSI and MISO lines of Master and Slave. SPI generates the signal with eight programmable clock rates in Master mode. The SS (P3.4) signal is a low active slave select pin. In 4-wire Slave mode, the signal is ignored when the Slave is not selected (SS=1). The SS is ignored when the SSDIS in SPCON is set in both Master and Slave modes. In Slave mode and the SSDIS is clear, the SPI active when SS stay low. For multiple-slave mode, only one slave device is selected at a time to avoid bus collision on the MISO line. In Master mode and the SSDIS is cleared, the MODF in SPSTA is set when this signal is low. For multiple-master mode, enable SS line to avoid multiple driving on MOSI and SCK lines from multiple masters.

Master Mode

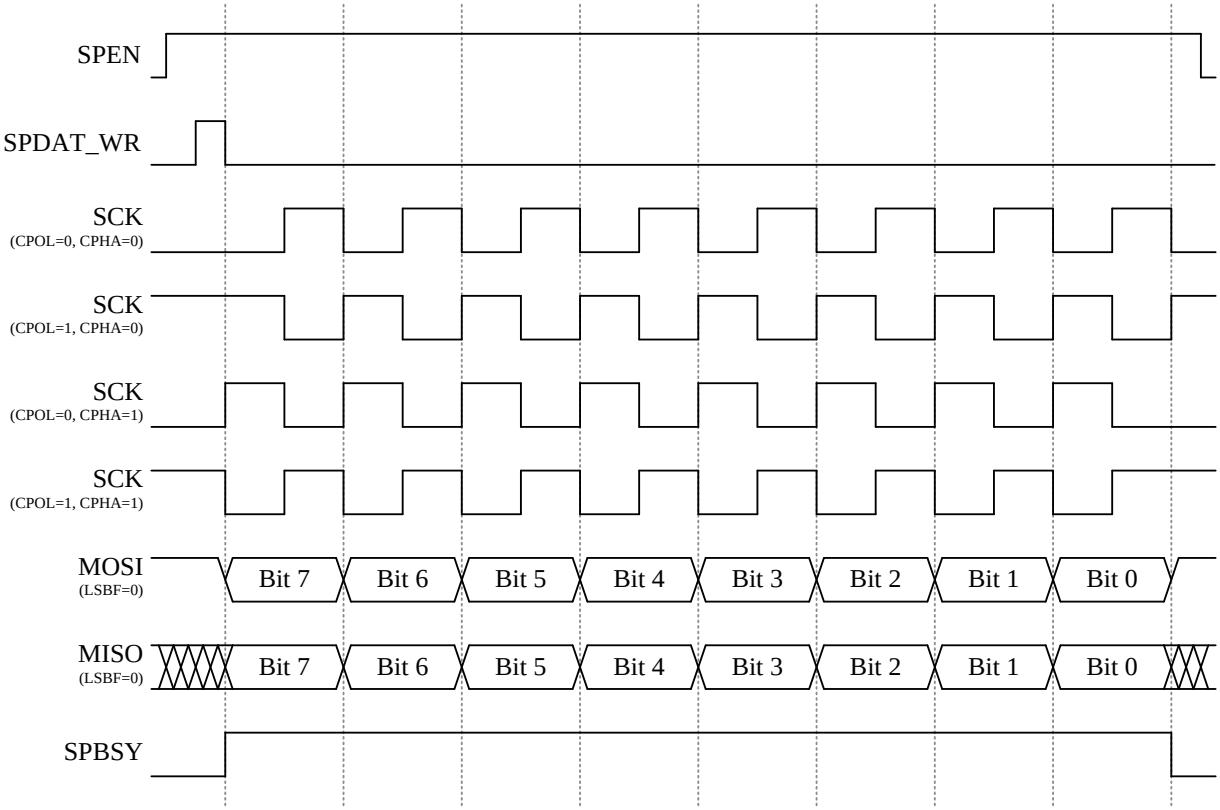
The SPI operates in Master mode by setting the MSTR bit in the SPCON. To start transmit, writing a data to the SPDAT. If the SPBSY bit is cleared, the data will be transferred to the shift register and starts shift out on the MOSI line. The data of the slave shift in from the MISO line at the same time. When the SPIF bit in the SPSTA becomes set at the end of the transfer, the receive data is written to receiver buffer and the RCVBF bit in the SPSTA is set. To prevent an overrun condition, software must read the SPDAT before next byte enters the shift register. The SPBSY bit will be set when writing a data to SPDAT to start transmit, and be cleared at the end of the eighth SCK period in Master mode.

Slave Mode

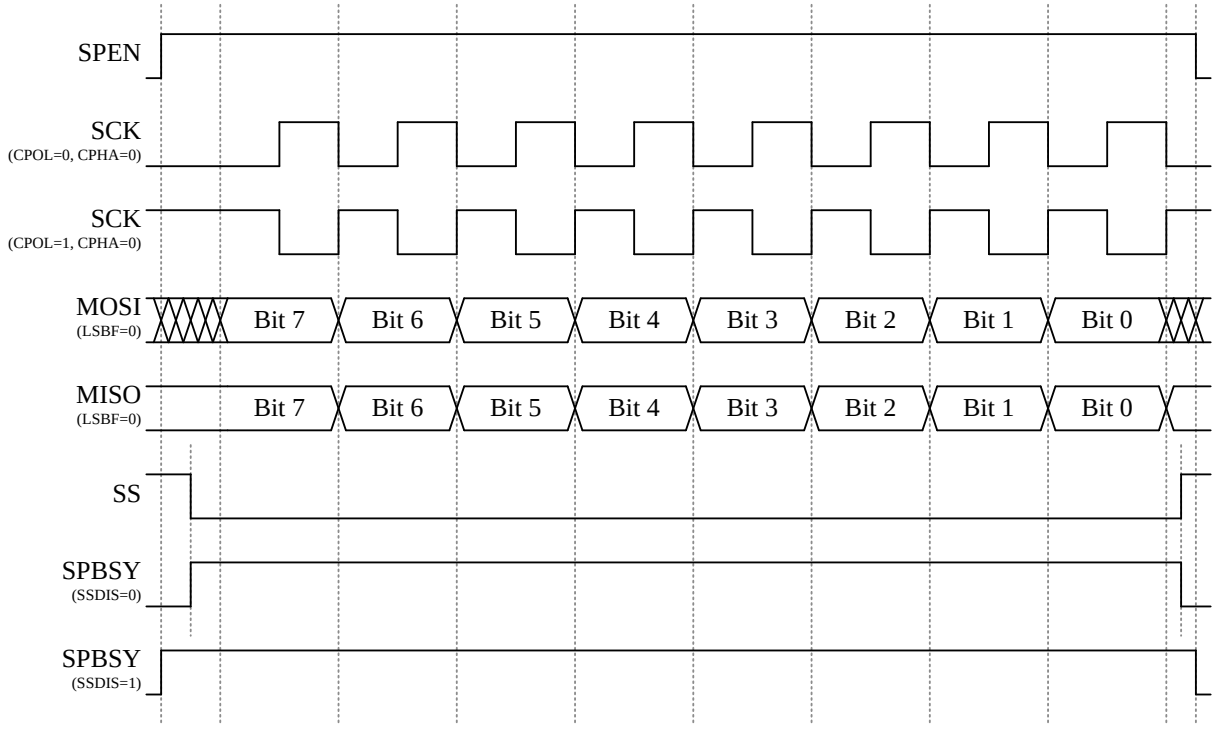
The SPI operates in Slave mode by clearing the MSTR bit in the SPCON. If the SSDIS is cleared, the transmission will start when the SS become low and remain low until the end of a data transfer. If the SSDIS is set, the transmission will start when the SPEN bit in the SPCON is set, and don't care the SS. The data from a master will shift into the shift register through the MOSI line, and shift out from the shift register on the MISO line. When a byte enters the shift register, the data will be transferred to receiver buffer if the RCVBF is cleared. If the RCVBF is set, the newer receive data will not be transferred to receiver buffer and the RCVOVF bit is set. After a byte enters the shift register, the SPIF and RCVBF bits are set. To prevent an overrun condition, software must read the SPDAT or write 0 to RCVBF before next byte enters the shift register. The maximum SCK frequency allowed in Slave mode is $F_{SYSCLK}/4$. In Slave mode, the SPBSY bit refers to the SS pin when the SSDIS bit is cleared, and refer to the SPEN bit when SSDIS bit is set.

Serial Clock

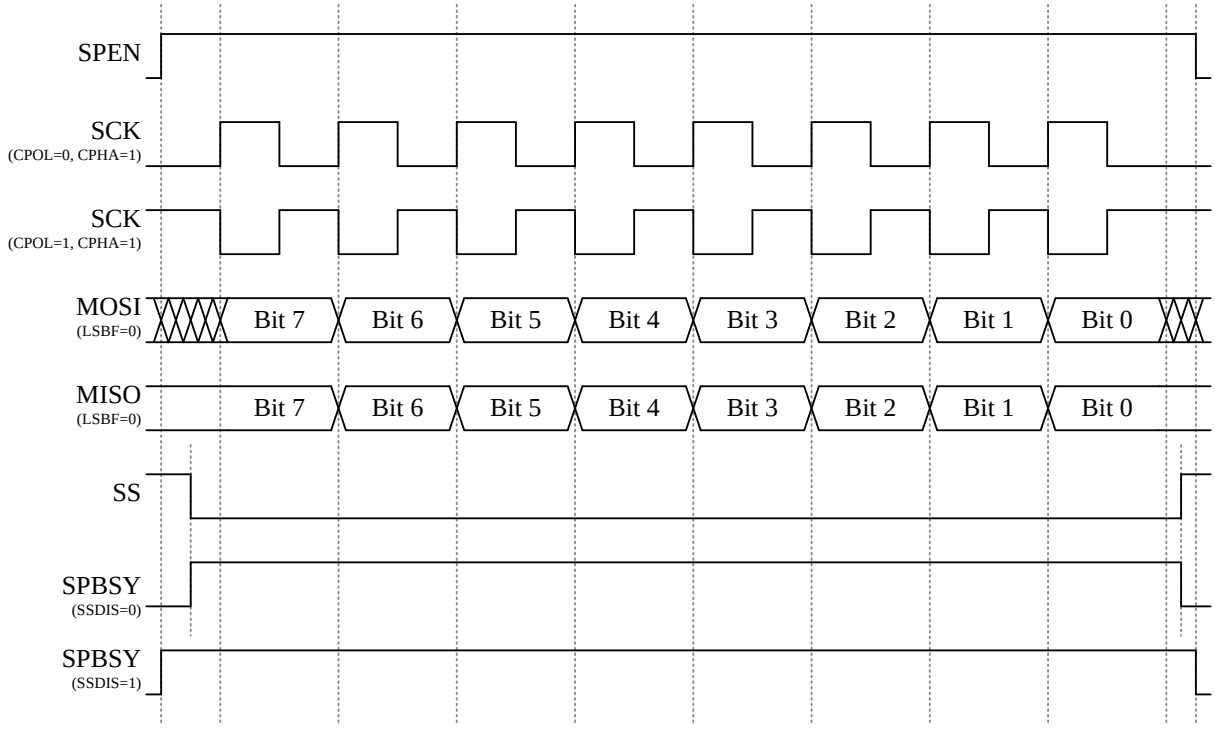
The SPI has four clock types by setting the CPOL and CPHA bits in the SPCON register. The CPOL bit defines the level of the SCK in SPI idle state. The level of the SCK in idle state is low when the CPOL bit is cleared, and is high when the CPOL bit is set. The CPHA bit defines the edges used to sample and shift data. The SPI sample data on the first edge of SCK period and shift data on the second edge of SCK period when the CPHA bit is cleared. The SPI sample data on the second edge of SCK period and shift data on first edge of SCK period when the CPHA bit is set. The figures below show the detail timing in Master and Slave modes. Both Master and Slave devices must be configured to use the same clock type before the SPEN bit is set. The SPCR controls the Master mode serial clock frequency. This register is ignored when operating in Slave mode. The SPI clock can select System clock divided by 2, 4, 8, or 16 in Master mode.



Master Mode Timing



Slave Mode Timing (CPHA=0)



Slave Mode Timing (CPHA=1)

In both Master and Slave modes, the SPIF bit is set by H/W at the end of a data transfer and generates an interrupt if SPI interrupt is enabled. The SPIF bit is cleared automatically when the program performs the interrupt service routines. S/W can also write 0 to clear this flag. If write data to SPDAT when the SPBSY is set, the WCOL bit will be set by H/W and generates an interrupt if SPI interrupt is enabled. When this occurs, the data write to SPDAT will be ignored, and shift register will not be written. Write 0 to this bit or when SPBSY is cleared and rewrite data to SPDAT will clear this flag. The MODF bit is set when SSDIS is cleared and SS pin is pulled low in Master mode. If SPI interrupt is enabled, an interrupt will be generated. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W. Write 0 to this bit will clear this flag.

SFR **BCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPCON	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

BCh.7 **SPEN:** SPI enable
0: SPI disable
1: SPI enable

BCh.6 **MSTR:** Master mode enable
0: Slave mode
1: Master mode

BCh.5 **CPOL:** SPI clock polarity
0: SCK is low in idle state
1: SCK is high in idle state

BCh.4 **CPHA:** SPI clock phase
0: Data sample on first edge of SCK period
1: Data sample on second edge of SCK period

BCh.3 **SSDIS:** SS pin disable
0: Enable SS pin
1: Disable SS pin

BCh.2 **LSBF:** LSB first
0: MSB first
1: LSB first

BCh.1~0 **SPCR:** SPI clock rate
00: $F_{SYSCLK}/2$
01: $F_{SYSCLK}/4$
10: $F_{SYSCLK}/8$
11: $F_{SYSCLK}/16$

SFR **BDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPSTA	SPIF	WCOL	MODF	RCVOVF	RCVBF	SPBSY	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	–	–
Reset	0	0	0	0	0	0	–	–

BDh.7 **SPIF:** SPI interrupt flag
This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.

BDh.6 **WCOL:** Write collision interrupt flag
Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.

BDh.5 **MODF:** Mode fault interrupt flag
Set by H/W when SSDIS is cleared and SS pin is pulled low in Master mode. Write 0 to this bit will clear this flag. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W.

BDh.4 **RCVOVF:** Received buffer overrun flag
Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.3 **RCVBF:** Receive buffer full flag
Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.

BDh.2 **SPBSY:** SPI busy flag
Set by H/W when a SPI transfer is in progress.

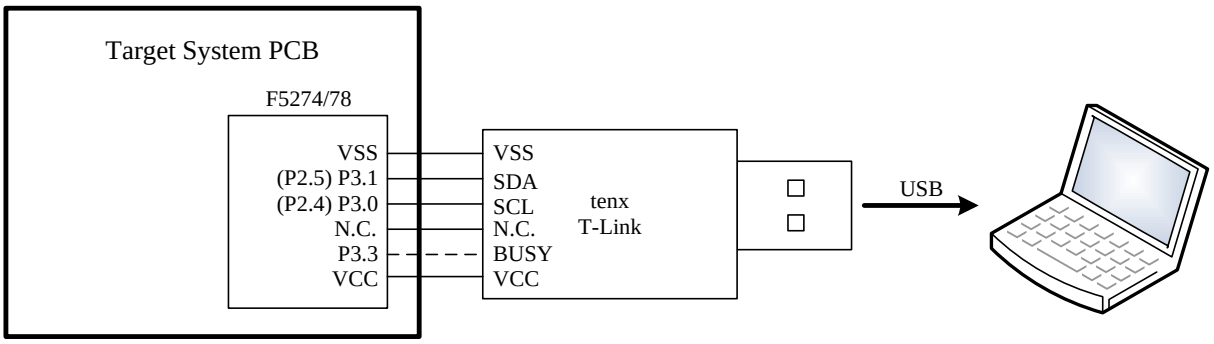
SFR **BEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPDAT	SPDAT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

BEh.7~0 **SPDAT:** SPI transmit and receive data
The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.

16. In Circuit Emulation (ICE) Mode

This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.
2. The device's P3.0 and P3.1 pins must work in input Mode (P3MOD0=0/1 and P3MOD1=0/1).
3. During Program Code download, P3.3 sent acknowledge signal to T-Link unit. After download stage, P3.3 can be emulated as any other pins.
4. The Program Memory's addressing space 0D00h~0FFFh and 0033h~003Ah are occupied by tenx EV module. So user Program cannot access these spaces.
5. The P3.0 and P3.1 pin's function cannot be emulated.
6. The P3.0 and P3.1 pin's can be replaced by P2.4 and P2.5.



SFR & CFGW MAP

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	1111-1111	**P0**	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0000-0000	**P0OE**	P0OE							
93h	0000-0101	**P2MOD**	P2OE				P2MOD1		P2MOD0	
94h	0000-0000	**OPTION**	UART1W	MODE3V	WDTPSC		ADCKS		TM3PSC	
95h	xx00-x000	**INTFLG**	LVDO	–	TKIF	ADIF	–	IE2	P1IF	TF3
96h	0000-0000	**P1WKUP**	P1WKUP							
97h	xxxx-xxx0	**SWCMD**	IAPALL/SWRST							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	1111-1111	**PWM0PRD**	PWM0PRD							
9Bh	1000-0000	**PWM0DH**	PWM0DH							
9Ch	1111-1111	**PWM1PRD**	PWM1PRD							
9Dh	1000-0000	**PWM1DH**	PWM1DH							
A0h	1111-1111	**P2**	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0
A1h	1000-1000	**PWMCON**	PWM1CKS		PWM1DL		PWM0CKS		PWM0DL	
A2h	0000-0000	**P1MODL**	P1MOD3		P1MOD2		P1MOD1		P1MOD0	
A3h	0000-0000	**P1MODH**	P1MOD7		P1MOD6		P1MOD5		P1MOD4	
A4h	0101-0101	**P3MODL**	P3MOD3		P3MOD2		P3MOD1		P3MOD0	
A5h	0x00-0000	**P3MODH**	T0OE	–	P3MOD6		P3MOD5		P3MOD4	
A6h	0000-00xx	**PINMOD**	PWM1AOE	PWM1BOE	PWM0AOE	PWM0BOE	TCOE	T2OE	–	–
A8h	0x00-0000	**IE**	EA	–	ET2	ES	ET1	EX1	ET0	EX0
A9h	0000-0000	**INTE1**	IAPWE			SPIE	ADTKIE	EX2	P1IE	TM3IE
AAh	xxxx-xxxx	**ADTKDT**	ADCDL				TKEOC	TKOVF	TKDH	
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
ACh	xxxx-xxxx	**TKDL**	TKDL							
ADh	1xxx-x100	**TKCON**	TKPD	–	–	–	–	TKTMR		
AEh	1111-1111	**CHSEL**	ADCHS				TKCHS			
AFh	xxxx-0011	**TKCON2**	ATKDT				TKAUTO	ATKRATE	ATKNUM	
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B1h	01xx-x100	**LCDCON**	LCDON	LCDDUTY	–	–	–	LCDBRIT		
B2h	0000-00xx	**LCDCON2**	LCDCKS	LCDPSC		SELLED	LEDPOL	LEDDTE	–	–
B3h	0000-0000	**LCDPIN**	LCDPIN7	LCDPIN6	LCDPIN5	LCDPIN4	LCDPIN3	LCDPIN2	LCDPIN1	LCDPIN0
B8h	xx00-0000	**IP**	–	–	PT2	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	PT2H	PSH	PT1H	PX1H	PT0H	PX0H
BAh	xxx0-0000	**IP1**	–	–	–	PSPI	PADTKI	PX2	PP1	PT3

Adr	Rst	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BBh	xxx0-0000	**IP1H**	–	–	–	PSPIH	PADTKIH	PX2H	PP1H	PT3H
BCh	0000-0000	**SPCON**	SPEN	MSTR	CPOL	CPHA	SSDIS	LSBF	SPCR	
BDh	0000-0xxx	**SPSTA**	SPIF	WCOL	MODF	RCVOVF	RCVBF	SPBSY	–	–
BEh	0000-0000	**SPDAT**	SPDAT							
C2h	x000-x000	**ATKC10H**	–	ATKC1H			–	ATKC0H		
C3h	x000-x000	**ATKC32H**	–	ATKC3H			–	ATKC2H		
C4h	0100-0000	**ATKC0L**	ATKC0L							
C5h	0100-0000	**ATKC1L**	ATKC1L							
C6h	0100-0000	**ATKC2L**	ATKC2L							
C7h	0100-0000	**ATKC3L**	ATKC3L							
C8h	0000-0000	**T2CON**	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2N	CPRL2N
CAh	0000-0000	**RCP2L**	RCP2L							
CBh	0000-0000	**RCP2H**	RCP2H							
CCh	0000-0000	**TL2**	TL2							
CDh	0000-0000	**TH2**	TH2							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D8h	00x0-0011	**CLKCON**	SCKTYPE	FCKTYPE	–	STPPCK	STPFCK	SELFCK	CLKPSC	
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F7h	xxxx-xxxx	**CFGWL**	WDTE		–	FRCF				
F8h	0000-0xx0	**AUX1**	CLRWDT	CLRTM3	TKSOC	ADSOC	CLRPWM0	–	–	DPSEL

Flash Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FFEh	**CFGWL**	–	–	–	FRCF				
1FFFh	**CFGWH**	PROT	XRSTE	LVRE		VCCFLT	PWRSAV	MVCLOCK	–

SFR & CFGW DESCRIPTION

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
80h	P0	7~0	P0	R/W	FFh	Port0 data, also controls the P0.n pin's pull-up function. If the P0.n SFR data is "1" and the corresponding P0OE.n=0 (input mode), the pull-up is enabled.
81h	SP	7~0	SP	R/W	07h	Stack Point
82h	DPL	7~0	DPL	R/W	00h	Data Point low byte
83h	DPH	7~0	DPH	R/W	00h	Data Point high byte
87h	PCON	7	SMOD	R/W	0	UART double baud rate control bit 0: Disable UART double baud rate 1: Enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Stop bit. If 1 Stop mode is entered.
		0	IDL	R/W	0	Idle bit. If 1, Idle mode is entered.
88h	TCON	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control 0: Timer1 stops 1: Timer1 runs
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control 0: Timer0 stops 1: Timer0 runs
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	TMOD	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
89h	TMOD	5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	TL0	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	TL1	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	TH0	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	TH1	7~0	TH1	R/W	00h	Timer1 data high byte
90h	P1	7~0	P1	R/W	FFh	Port1 data
91h	P0OE	7~0	P0OE	R/W	00h	Port0 CMOS Push-Pull output enable control 0: Disable 1: Enable
93h	P2MOD	7~4	P2OE	R/W	0000	P2.5~P2.2 CMOS Push-Pull output enable control 0: Disable 1: Enable
		3~2	P2MOD1	R/W	01	P2.1 pin control
		1~0	P2MOD0	R/W	01	P2.0 pin control
94h	OPTION	7	UART1W	R/W	0	One wire UART mode enable, both TXD/RXD use P3.1 pin 0: Disable one wire UART mode 1: Enable one wire UART mode
		6	MODE3V	R/W	0	3V mode selection control bit If this bit is set, the Chip can be only operated in the condition of V_{CC}<3.6V, and LDO is turned off to save current
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 360ms WDT overflow rate 01: 180ms WDT overflow rate 10: 90ms WDT overflow rate 11: 45ms WDT overflow rate

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
94h	OPTION	3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
		1~0	TM3PSC	R/W	00	Timer3 interrupt rate control select 00: Interrupt rate is 32768 Slow clock cycle 01: Interrupt rate is 16384 Slow clock cycle 10: Interrupt rate is 8192 Slow clock cycle 11: Interrupt rate is 128 Slow clock cycle
95h	INTFLG	7	LVDO	R		Low Voltage Detect flag Set by H/W when a low voltage occurs. The flag is valid when LVR is 2.0V. This flag is disabled in Stop mode or if MODE3V=1 and PWRSAV=1.
		5	TKIF	R/W	0	Touch Key interrupt flag In the S/W Manual mode: Set by H/W at the end of conversion. S/W writes DFh to INTFLG or sets the TKSOC bit to clear this flag. In the ATK mode: Set by H/W when a TK channel's touch event is detected. It is cleared automatically when the program performs the interrupt service routine. S/W can write DFh to INTFLG to clear this bit. ***Note:*** In ATK mode, this flag may be cleared improperly by ADC module. User should not start the ADC conversion in ATK mode.
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.
		2	IE2	R/W	0	External Interrupt 2 (INT2 pin) edge flag Set by H/W when a falling edge is detected on the INT2 pin state, no matter the EX2 is 0 or 1. It is cleared automatically when the program performs the interrupt service routine. S/W can write FBh to INTFLG to clear this bit.
		1	P1IF	R/W	0	Port1 pin change interrupt flag Set by H/W when a P1 pin state change is detected, and its interrupt enable bit is set (P1WKUP). P1IE does not affect this flag's setting. It is cleared automatically when the program performs the interrupt service routine. S/W can write FDh to INTFLG to clear this bit.
		0	TF3	R/W	0	Timer 3 interrupt flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
96h	P1WKUP	7~0	P1WKUP	R/W	00h	P1.7~P1.0 pin individual Wake up/Interrupt enable control 0: Disable 1: Enable
97h	SWCMD	7~0	SWRST	W		Write 56h to generate S/W Reset
		7~0	IAPALL	W		Write 65h to set IAPALL control flag; Write other value to clear IAPALL flag. It is recommended to clear it immediately after IAP access.
		0	IAPALL	R	0	Flag indicates Flash memory sectors can be accessed by IAP or not. This bit combines with MVCLOCK to define the accessible IAP area.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
98h	SCON	7	SM0	R/W	0	Serial port mode select bit 0,1 00: Mode0: 8 bit shift register, Baud Rate=F_{SYSCLK}/2 01: Mode1: 8 bit UART, Baud Rate is variable 10: Mode2: 9 bit UART, Baud Rate = F_{SYSCLK}/32 or /64 11: Mode3: 9 bit UART, Baud Rate is variable
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	UART reception enable 0: Disable reception 1: Enable reception
		3	TB8	R/W	0	Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit in Mode 1 if SM2=0
		1	TI	R/W	0	Transmit interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.
		0	RI	R/W	0	Receive interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	SBUF	7~0	SBUF	R/W		UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	PWM0PRD	7~0	PWM0PRD	R/W	FFh	PWM0 8-bit period register
9Bh	PWM0DH	7~0	PWM0DH	R/W	80h	bits 9~2 of the PWM0 10-bit duty register
9Ch	PWM1PRD	7~0	PWM1PRD	R/W	FFh	PWM1 8-bit period register
9Dh	PWM1DH	7~0	PWM1DH	R/W	80h	bits 9~2 of the PWM1 10-bit duty register
A0h	P2	7~0	P2	R/W	FFh	Port2 data, also controls the P2.n pin's pull-up function. If the P2.n SFR data is "1" and the corresponding P2OE.n=0 (input mode), the pull-up is enabled.
A1h	PWMCON	7~6	PWM1CKS	R/W	10	PWM1 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRCx2
		5~4	PWM1DL	R/W	00	bits 1~0 of the PWM1 10-bit duty register
		3~2	PWM0CKS	R/W	10	PWM0 clock source 00: F_{SYSCLK}/4 01: F_{SYSCLK}/2 10: F_{SYSCLK} 11: FRCx2
		1~0	PWM0DL	R/W	00	bits 1~0 of the PWM0 10-bit duty register
A2h	P1MODL	7~6	P1MOD3	R/W	00	P1.3 pin control
		5~4	P1MOD2	R/W	00	P1.2 pin control
		3~2	P1MOD1	R/W	00	P1.1 pin control
		1~0	P1MOD0	R/W	00	P1.0 pin control

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
A3h	P1MODH	7~6	P1MOD7	R/W	00	P1.7 pin control
		5~4	P1MOD6	R/W	00	P1.6 pin control
		3~2	P1MOD5	R/W	00	P1.5 pin control
		1~0	P1MOD4	R/W	00	P1.4 pin control
A4h	P3MODL	7~6	P3MOD3	R/W	01	P3.3 pin control
		5~4	P3MOD2	R/W	01	P3.2 pin control
		3~2	P3MOD1	R/W	01	P3.1 pin control
		1~0	P3MOD0	R/W	01	P3.0 pin control
A5h	P3MODH	7	T0OE	R/W	0	Timer0 signal output (T0O) control 0: Disable Timer0 overflow divided by 64 output to P3.4 1: Enable Timer0 overflow divided by 64 output to P3.4
		5~4	P3MOD6	R/W	00	P3.6 pin control
		3~2	P3MOD5	R/W	00	P3.5 pin control
		1~0	P3MOD4	R/W	00	P3.4 pin control
A6h	PINMOD	7	PWM1AOE	R/W	0	PWM1A signal output enable 0: Disable PWM1A signal output to P1.3 1: Enable PWM1A signal output to P1.3
		6	PWM1BOE	R/W	0	PWM1B signal output enable (PWM1A and PWM1B signals are identical) 0: Disable PWM1B signal output to P2.3 1: Enable PWM1B signal output to P2.3
		5	PWM0AOE	R/W	0	PWM0A signal output enable 0: Disable PWM0A signal output to P1.2 1: Enable PWM0A signal output to P1.2
		4	PWM0BOE	R/W	0	PWM0B signal output enable (PWM0A and PWM0B signals are identical) 0: Disable PWM0B signal output to P2.2 1: Enable PWM0B signal output to P2.2
		3	TCOE	R/W	0	TCOE: System clock signal output (CKO) control 0: Disable System clock divided by 2 output to P1.4 1: Enable System clock divided by 2 output to P1.4
		2	T2OE	R/W	0	Timer2 signal output (T2O) enable 0: Disable Timer2 overflow divided by 2 output to P1.0 1: Enable Timer2 overflow divided by 2 output to P1.0
A8h	IE	7	EA	R/W	0	Global interrupt enable 0: Disable all interrupts 1: Each interrupt is enabled or disabled by its individual interrupt control bit
		5	ET2	R/W	0	Timer2 interrupt enable 0: Disable Timer2 interrupt 1: Enable Timer2 interrupt
		4	ES	R/W	0	Serial Port (UART) interrupt enable 0: Disable Serial Port (UART) interrupt 1: Enable Serial Port (UART) interrupt
		3	ET1	R/W	0	Timer1 interrupt enable 0: Disable Timer1 interrupt 1: Enable Timer1 interrupt

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
A8h	IE	2	EX1	R/W	0	INT1 pin Interrupt enable and Stop mode wake up enable 0: Disable INT1 pin Interrupt and Stop mode wake up 1: Enable INT1 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	ET0	R/W	0	Timer0 interrupt enable 0: Disable Timer0 interrupt 1: Enable Timer0 interrupt
		0	EX0	R/W	0	INT0 pin Interrupt enable and Stop mode wake up enable 0: Disable INT0 pin Interrupt and Stop mode wake up 1: Enable INT0 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
A9h	INTE1	7~5	IAPWE	R/W	000	Set to 101 to enable IAP write. It is recommended to clear it immediately after IAP write.
		4	SPIE	R/W	0	SPI interrupt enable 0: Disable SPI interrupt 1: Enable SPI interrupt
		3	ADTKIE	R/W	0	ADC/Touch Key interrupt enable 0: Disable ADC/Touch Key interrupt 1: Enable ADC/Touch Key interrupt
		2	EX2	R/W	0	INT2 pin Interrupt enable and Stop mode wake up enable 0: Disable INT2 pin Interrupt and Stop mode wake up 1: Enable INT2 pin Interrupt and Stop mode wake up, it can wake up CPU from Stop mode no matter EA is 0 or 1.
		1	P1IE	R/W	0	Port1 pin change interrupt enable 0: Disable Port1 pin change interrupt 1: Enable Port1 pin change interrupt
		0	TM3IE	R/W	0	Timer3 interrupt enable 0: Disable Timer3 interrupt 1: Enable Timer3 interrupt
AAh	ADTKDT	7~4	ADCDL	R		ADC data bit 3~0
		3	TKEOC	R		Touch Key end of conversion flag 0: Indicates conversion is in progress 1: Indicates conversion is finished
		2	TKOVF	R		Touch Key counter overflow 0: Indicates that the counter has not overflow 1: Indicates that the counter has overflow
		1~0	TKDH	R		Touch Key counter data bit 9~8
ABh	ADCDH	7~0	ADCDH	R		ADC data bit 11~4
ACh	TKDL	7~0	TKDL	R		Touch Key counter data bit 7~0
ADh	TKCON	7	TKPD	R/W	1	Touch Key power down 0: Touch Key running 1: Touch Key power down
		2~0	TKTMR	R/W	100	Touch Key conversion time select TKTMR adjusts the value of Touch Key reference voltage. A larger value of TKTMR requires a longer charging time, which can affect the sensitivity of touch sensing. 000: Conversion time shortest … 111: Conversion time longest

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
AEh	CHSEL	7~4	ADCHS	R/W	1111	ADC channel select 0000: ADC0 (P3.3) 0001: ADC1 (P3.2) 0010: ADC2 (P3.1) 0011: ADC3 (P3.0) 0100: ADC4 (P1.0) 0101: ADC5 (P1.1) 0110: ADC6 (P1.2) 0111: ADC7 (P1.3) 1000: ADC8 (P1.4) 1001: ADC9 (P1.5) 1010: V_{SS} 1011: VBG (internal reference voltage) 11xx: Undefined
		3~0	TKCHS	R/W	1111	Touch Key channel select 0000: TK0 (P1.0) 0001: TK1 (P1.1) 0010: TK2 (P1.2) 0011: TK3 (P1.3) 0100: TK4 (P3.3) 0101: TK5 (P3.2) 0110: TK6 (P3.1) 0111: TK7 (P3.0) 1000: TK8 (P1.4) 1001: TK9 (P1.6) 1010: TK10 (P1.7) 1011: TK11 (P3.6) 1100: TK12 (P3.5) 1101: TK13 (P3.4) 1110: Undefined 1111: Internal reference capacitor
AFh	TKCON2	7~4	ATKDT	R		Touch Key Auto Scan Result (for H/W ATK Mode) xxx1: TK0 has a Touch event xx1x: TK1 has a Touch event x1xx: TK2 has a Touch event 1xxx: TK3 has a Touch event
		3	TKAUTO	R/W	0	Touch Key Auto Scan Mode Enable 0: S/W Mode 1: H/W ATK Mode
		2	ATKRATE	R/W	0	Touch Key Scan Rate (for H/W ATK Mode) 0: ATK scan rate at every 4096 Slow clock cycles 1: ATK scan rate at every 2048 Slow clock cycles
		1~0	ATKNUM	R/W	11	Touch Key Auto Scan Channel Number (for H/W ATK Mode) 00: ATK only detect TK0 01: ATK detect TK0 and TK1 10: ATK detect TK0~TK2 11: ATK detect TK0~TK3
B0h	P3	7~0	P3	R/W	FFh	Port3 data

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
B1h	LCDCON	7	LCDON	R/W	0	LCD/LED enable bit 0: LCD/LED disable 1: LCD/LED enable
		6	LCDDUTY	R/W	1	LCD/LED duty select 0: 1/3 duty 1: 1/4 duty
		2~0	LCDBRIT	R/W	100	LCD brightness select 000: (12/20) x V_{CC} 001: (12/19) x V_{CC} 010: (12/18) x V_{CC} 011: (12/17) x V_{CC} 100: (12/15) x V_{CC} 101: (12/14) x V_{CC} 110: (12/13) x V_{CC} 111: V_{CC}
B2h	LCDCON2	7	LCDCKS	R/W	0	LCD/LED clock source select 0: SRC 1: SXT
		6~5	LCDPSC	R/W	00	LCD/LED clock prescaler select 00: LCD/LED clock is divided by 256 01: LCD/LED clock is divided by 128 10: LCD/LED clock is divided by 64 11: LCD/LED clock is divided by 32
		4	SELLED	R/W	0	LED select mode 0: LCD mode 1: LED mode
		3	LEDPOL	R/W	0	LED COM polarity select 0: Active low (with high sink) 1: Active high
		2	LEDDTE	R/W	0	LED COM dead time enable 0: LED COM dead time disable 1: LED COM dead time enable
B3h	LCDPIN	7	LCDPIN7	R/W	0	P3.2 (SEG17) LCD/LED mode enable
		6	LCDPIN6	R/W	0	P3.1 (SEG16) LCD/LED mode enable
		5	LCDPIN5	R/W	0	P3.0 (SEG15) LCD/LED mode enable
		4	LCDPIN4	R/W	0	P1.0 (SEG14) LCD/LED mode enable
		3	LCDPIN3	R/W	0	P1.1 (SEG13) LCD/LED mode enable
		2	LCDPIN2	R/W	0	P1.2 (SEG12) LCD/LED mode enable
		1	LCDPIN1	R/W	0	P1.3~P1.6 (SEG11~8) LCD/LED mode enable ***Note***: SEG9 and Touch Key CLD share the same pin. If this bit is set, the Touch Key function would be affected.
		0	LCDPIN0	R/W	0	P1.7, P3.6~P3.4 (SEG7~4) LCD/LED mode enable 0: I/O mode 1: LCD/LED mode
B8h	IP	5	PT2	R/W	0	Timer2 interrupt priority low bit
		4	PS	R/W	0	Serial Port interrupt priority low bit
		3	PT1	R/W	0	Timer1 interrupt priority low bit
		2	PX1	R/W	0	INT1 interrupt priority low bit
		1	PT0	R/W	0	Timer0 interrupt priority low bit
		0	PX0	R/W	0	INT0 interrupt priority low bit

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
B9h	IPH	5	PT2H	R/W	0	Timer2 interrupt priority high bit
		4	PSH	R/W	0	Serial Port interrupt priority high bit
		3	PT1H	R/W	0	Timer1 interrupt priority high bit
		2	PX1H	R/W	0	INT1 interrupt priority high bit
		1	PT0H	R/W	0	Timer0 interrupt priority high bit
		0	PX0H	R/W	0	INT0 interrupt priority high bit
BAh	IP1	4	PSPI	R/W	0	SPI interrupt priority low bit
		3	PADTKI	R/W	0	ADC/Touch Key interrupt priority low bit
		2	PX2	R/W	0	INT2 interrupt priority low bit
		1	PP1	R/W	0	Port1 pin change interrupt priority low bit
		0	PT3	R/W	0	Timer3 interrupt priority low bit
BBh	IP1H	4	PSPIH	R/W	0	SPI interrupt priority high bit
		3	PADTKIH	R/W	0	ADC/Touch Key interrupt priority high bit
		2	PX2H	R/W	0	INT2 interrupt priority high bit
		1	PP1H	R/W	0	Port1 interrupt priority high bit
		0	PT3H	R/W	0	Timer3 interrupt priority high bit
BCh	SPCON	7	SPEN	R/W	0	SPI enable 0: SPI disable 1: SPI enable
		6	MSTR	R/W	0	Master mode enable 0: Slave mode 1: Master mode
		5	CPOL	R/W	0	SPI clock polarity 0: SCK is low in idle state 1: SCK is high in idle state
		4	CPHA	R/W	0	SPI clock phase 0: Data sample on first edge of SCK period 1: Data sample on second edge of SCK period
		3	SSDIS	R/W	0	SS pin disable 0: Enable SS pin 1: Disable SS pin
		2	LSBF	R/W	0	LSB first 0: MSB first 1: LSB first
		1~0	SPCR	R/W	00	SPI clock rate 00: $F_{SYSCLK}/2$ 01: $F_{SYSCLK}/4$ 10: $F_{SYSCLK}/8$ 11: $F_{SYSCLK}/16$
BDh	SPSTA	7	SPIF	R/W	0	SPI interrupt flag This is set by H/W at the end of a data transfer. Cleared by H/W when an interrupt is vectored into. Writing 0 to this bit will clear this flag.
		6	WCOL	R/W	0	Write collision interrupt flag Set by H/W if write data to SPDAT when SPBSY is set. Write 0 to this bit or rewrite data to SPDAT when SPBSY is cleared will clear this flag.
		5	MODF	R/W	0	Mode fault interrupt flag Set by H/W when SSDIS is cleared and SS pin is pulled low in Master mode. Write 0 to this bit will clear this flag. When this bit is set, the SPEN and MSTR in SPCON will be cleared by H/W.

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
BDh	SPSTA	4	RCVOVF	R/W	0	Received buffer overrun flag Set by H/W at the end of a data transfer and RCVBF is set. Write 0 to this bit or read SPDAT register will clear this flag.
		3	RCVBF	R/W	0	Receive buffer full flag Set by H/W at the end of a data transfer. Write 0 to this bit or read SPDAT register will clear this flag.
		2	SPBSY	R		SPI busy flag Set by H/W when a SPI transfer is in progress.
BEh	SPDAT	7~0	SPDAT	R/W	0	SPI transmit and receive data The SPDAT register is used to transmit and receive data. Writing data to SPDAT place the data into shift register and start a transfer when in master mode. Reading SPDAT returns the contents of the receive buffer.
C2h	ATKC10H	6~4	ATKC1H	R/W	000	Data Threshold bit 10~8 Compared with TK1 scan (for H/W ATK Mode)
		2~0	ATKC0H	R/W	000	Data Threshold bit 10~8 Compared with TK0 scan (for H/W ATK Mode)
C3h	ATKC32H	6~4	ATKC3H	R/W	000	Data Threshold bit 10~8 Compared with TK3 scan (for H/W ATK Mode)
		2~0	ATKC2H	R/W	000	Data Threshold bit 10~8 Compared with TK2 scan (for H/W ATK Mode)
C4h	ATKC0L	7~0	ATKC0L	R/W	40h	Data Threshold bit 7~0 Compared with TK0 scan (for H/W ATK Mode)
C5h	ATKC1L	7~0	ATKC1L	R/W	40h	Data Threshold bit 7~0 Compared with TK1 scan (for H/W ATK Mode)
C6h	ATKC2L	7~0	ATKC2L	R/W	40h	Data Threshold bit 7~0 Compared with TK2 scan (for H/W ATK Mode)
C7h	ATKC3L	7~0	ATKC3L	R/W	40h	Data Threshold bit 7~0 Compared with TK3 scan (for H/W ATK Mode)
C8h	T2CON	7	TF2	R/W	0	Timer2 overflow flag Set by H/W when Timer/Counter 2 overflows unless RCLK=1 or TCLK=1. This bit must be cleared by S/W.
		6	EXF2	R/W	0	T2EX interrupt pin falling edge flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. This bit must be cleared by S/W.
		5	RCLK	R/W	0	UART receive clock control bit 0: Use Timer1 overflow as receive clock for serial port in mode 1 or 3 1: Use Timer2 overflow as receive clock for serial port in mode 1 or 3
		4	TCLK	R/W	0	UART transmit clock control bit 0: Use Timer1 overflow as transmit clock for serial port in mode 1 or 3 1: Use Timer2 overflow as transmit clock for serial port in mode 1 or 3
		3	EXEN2	R/W	0	T2EX pin enable 0: T2EX pin disable 1: T2EX pin enable, it cause a capture or reload when a negative transition on T2EX pin is detected if RCLK= TCLK=0
		2	TR2	R/W	0	Timer2 run control 0: Timer2 stops 1: Timer2 runs

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
C8h	T2CON	1	CT2N	R/W	0	Timer2 Counter/Timer select bit 0: Timer mode, Timer2 data increases at 2 System clock cycle rate 1: Counter mode, Timer2 data increases at T2 pin's negative edge
		0	CPRL2N	R/W	0	Timer2 Capture/Reload control bit 0: Reload mode, auto-reload on Timer2 overflows or negative transitions on T2EX pin if EXEN2=1 1: Capture mode, capture on negative transitions on T2EX pin if EXEN2=1 If RCLK=1 or TCLK=1, CPRL2N is ignored and timer is forced to auto-reload on Timer2 overflow
CAh	RCP2L	7~0	RCP2L	R/W	00h	Timer2 reload/capture data low byte
CBh	RCP2H	7~0	RCP2H	R/W	00h	Timer2 reload/capture data high byte
CCh	TL2	7~0	TL2	R/W	00h	Timer2 data low byte
CDh	TH2	7~0	TH2	R/W	00h	Timer2 data high byte
D0h	PSW	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	The contents of (RS1, RS0) enable the working register banks as: 00: Bank 0 (00h~07h) 01: Bank 1 (08h~0Fh) 10: Bank 2 (10h~17h) 11: Bank 3 (18h~1Fh)
		3	RS0	R/W	0	
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of "one" bits in the accumulator.
D8h	CLKCON	7	SCKTYPE	R/W	0	Slow clock type. This bit can be changed only in Fast mode (SELFCK=1). 0: SRC 1: SXT
		6	FCKTYPE	R/W	0	Fast clock type. This bit can be changed only in Slow mode (SELFCK=0). 0: FRC 1: FXT
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/Timer1/Timer2/ADC clock in Idle mode
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock source selection. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. 00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
E0h	ACC	7~0	ACC	R/W	00h	Accumulator
F0h	B	7~0	B	R/W	00h	B register

SFR Adr	SFR Name	Bit #	Bit Name	R/W	Rst	Description
F7h	CFGWL	7~6	WDTE	R/W		Watchdog Timer Reset control 0x: Watchdog Timer Reset disable 10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Stop mode 11: Watchdog Timer Reset always enable
		4~0	FRCF	R/W		Fast RC frequency adjustment
F8h	AUX1	7	CLRWDT	R/W	0	Set to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set to clear Timer3, H/W auto clear it at next clock cycle
		5	TKSOC	R/W	0	Start Touch Key conversion Set the TKSOC bit to start Touch Key conversion, and the TKSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		4	ADSOC	R/W	0	Start ADC conversion Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
		3	CLRPWM0	R/W	0	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held
		0	DPSEL	R/W	0	Active DPTR Select

Flash Adr	Bit #	Name	Description
1FFEh	4~0	FRCF	Fast RC frequency adjustment
1FFFh	7	PROT	Flash Memory Code Protect 0: Disable protect 1: Enable protect
	6	XRSTE	External Pin Reset control 0: Disable External Pin Reset 1: Enable External Pin Reset
	5~4	LVRE	Low Voltage Reset function select 00: Set LVR at 2.9V 01: Set LVR at 2.3V 10: LVR disable and set LVD at 2.3V 11: Set LVR at 1.8V and LVD at 2.3V
	3	VCCFLT	Set 1 to enhance the Chip's power noise immunity
	2	PWRSAV	Power save function control bit 0: Disable Power save function 1: Enable Power save function
	1	MVCLOCK	If 1, the MOVC & MOVX instruction's accessibility to MOVC-Lock area is limited.

INSTRUCTION SET

Instructions are 1, 2 or 3 Bytes long as listed in the 'byte' column below. Each instruction takes 2~8 System clock cycles to execute as listed in the 'cycle' column below.

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A, Rn	Add register to A	1	2	28-2F
ADD A, dir	Add direct byte to A	2	2	25
ADD A, @Ri	Add indirect memory to A	1	2	26-27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	2	38-3F
ADDC A, dir	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A, dir	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8	A4
DIV AB	Divide A by B	1	8	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A, Rn	AND register to A	1	2	58-5F
ANL A, dir	AND direct byte to A	2	2	55
ANL A, @Ri	AND indirect memory to A	1	2	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL dir, A	AND A to direct byte	2	2	52
ANL dir, #data	AND immediate to direct byte	3	4	53
ORL A, Rn	OR register to A	1	2	48-4F
ORL A, dir	OR direct byte to A	2	2	45
ORL A, @Ri	OR indirect memory to A	1	2	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL dir, A	OR A to direct byte	2	2	42
ORL dir, #data	OR immediate to direct byte	3	4	43
XRL A, Rn	Exclusive-OR register to A	1	2	68-6F
XRL A, dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A, #data	Exclusive-OR immediate to A	2	2	64
XRL dir, A	Exclusive-OR A to direct byte	2	2	62
XRL dir, #data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RLC A	Rotate A left through carry	1	2	33
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A, Rn	Move register to A	1	2	E8-EF
MOV A, dir	Move direct byte to A	2	2	E5
MOV A, @Ri	Move indirect memory to A	1	2	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	2	F8-FF
MOV Rn, dir	Move direct byte to register	2	4	A8-AF
MOV Rn, #data	Move immediate to register	2	2	78-7F
MOV dir, A	Move A to direct byte	2	2	F5
MOV dir, Rn	Move register to direct byte	2	4	88-8F
MOV dir, dir	Move direct byte to direct byte	3	4	85
MOV dir, @Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir, #data	Move immediate to direct byte	3	4	75
MOV @Ri, A	Move A to indirect memory	1	2	F6-F7
MOV @Ri, dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri, #data	Move immediate to indirect memory	2	2	76-77
MOV DPTR, #data	Move immediate to data pointer	3	4	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	4	93
MOVC A, @A+PC	Move code byte relative PC to A	1	4	83
MOVX A, @Ri	Move external data(A8) to A	1	4	E2-E3
MOVX A, @DPTR	Move external data(A16) to A	1	4	E0
MOVX @Ri, A	Move A to external data(A8)	1	4	F2-F3
MOVX @DPTR, A	Move A to external data(A16)	1	4	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A, Rn	Exchange A and register	1	2	C8-CF
XCH A, dir	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A, @Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	4	82
ANL C, /bit	AND direct bit inverse to carry	2	4	B0
ORL C, bit	OR direct bit to carry	2	4	72
ORL C, /bit	OR direct bit inverse to carry	2	4	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	4	11-F1
LCALL addr 16	Long jump to subroutine	3	4	12
RET	Return from subroutine	1	4	22
RETI	Return from interrupt	1	4	32
AJMP addr 11	Absolute jump unconditional	2	4	01-E1
LJMP addr 16	Long jump unconditional	3	4	02
SJMP rel	Short jump (relative address)	2	4	80
JC rel	Jump on carry=1	2	4	40
JNC rel	Jump on carry=0	2	4	50
JB bit, rel	Jump on direct bit=1	3	4	20
JNB bit, rel	Jump on direct bit=0	3	4	30
JBC bit, rel	Jump on direct bit=1 and clear	3	4	10
JMP @A+DPTR	Jump indirect relative DPTR	1	4	73
JZ rel	Jump on accumulator=0	2	4	60
JNZ rel	Jump on accumulator … 0	2	4	70
CJNE A, dir,rel	Compare A,direct, jump not equal relative	3	4	B5
CJNE A, #data,rel	Compare A,immediate, jump not equal relative	3	4	B4
CJNE Rn, #data,rel	Compare register,immediate, jump not equal relative	3	4	B8-BF
CJNE @Ri, #data,rel	Compare indirect,immediate, jump not equal relative	3	4	B6-B7
DJNZ Rn, rel	Decrement register, jump not zero relative	2	4	D8-DF
DJNZ dir, rel	Decrement direct byte, jump not zero relative	3	4	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25°C)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output current high per 1 PIN	–25	mA
Output current high per all PIN	–80	
Output current low per 1 PIN	+30	
Output current low per all PIN	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–20 ~ +70	°C
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25°C, V_{CC}=2.0V ~ 5.5V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	V_{CC}	Fast mode, F_{SYSCLK}=7.3728 MHz		2.3	–	5.5	V
		Fast mode, F_{SYSCLK}=3.6864 MHz		2.0	–	5.5	
		Fast mode, F_{SYSCLK}=1.8432 MHz		1.3	–	5.5	
		Fast mode, F_{SYSCLK}=0.4608 MHz		1.3	–	5.5	
		Slow mode, SRC		1.3	–	5.5	
Input High Voltage	V_{IH}	All Input, except P3.7, P2.1	V_{CC}=5V	0.6V_{CC}	–	–	V
			V_{CC}=3V	0.6V_{CC}	–	–	
		P3.7, P2.1	V_{CC}=5V	0.8V_{CC}	–	–	
			V_{CC}=3V	0.8V_{CC}	–	–	
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	
I/O Port Source Current	I_{OH}	All Output, except P3.7	V_{CC}=5V V_{OH}=0.9V_{CC}	6	12	–	mA
			V_{CC}=3V V_{OH}=0.9V_{CC}	2.5	5	–	
I/O Port Sink Current	I_{OL}	All Output, except P0.0~P0.3	V_{CC}=5V V_{OL}=0.1V_{CC}	12	24	–	mA
			V_{CC}=3V V_{OL}=0.1V_{CC}	6	12	–	
		P0.0~P0.3	V_{CC}=5V V_{OL}=0.1V_{CC}	35	70	–	
			V_{CC}=3V V_{OL}=0.1V_{CC}	20	40	–	
Input Leakage Current (pin high)	I_{ILH}	All Input	V_{in}=V_{CC}	–	–	1	µA
Input Leakage Current (pin low)	I_{IILL}	All Input	V_{in}=0V	–	–	–1	

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Supply Current	I_{CC}	Fast, V_{CC}=5V LVR enable MODE3V=0	FXT=8 MHz	–	3.7	–	mA
			FRC=7.3728 MHz	–	3	–	
			FRC=3.6864 MHz	–	1.8	–	
		Fast, V_{CC}=3V LVR enable MODE3V=0	FXT=8 MHz	–	2.7	–	
			FRC=7.3728 MHz	–	2.5	–	
			FRC=3.6864 MHz	–	1.5	–	
		Fast, V_{CC}=3V LVR enable MODE3V=1	FXT=8 MHz	–	2.5	–	
			FRC=7.3728 MHz	–	2.3	–	
			FRC=3.6864 MHz	–	1.4	–	
		Slow, V_{CC}=5V LVR enable MODE3V=0	SXT=32 KHz	–	220	–	µA
			SRC=24 KHz	–	205	–	
		Slow, V_{CC}=3V LVR enable MODE3V=0	SXT=32 KHz	–	180	–	
			SRC=24 KHz	–	175	–	
		Slow, V_{CC}=3V MODE3V=1 PWRSAV=1	SXT=32 KHz	–	13	–	
			SRC=24 KHz	–	9	–	
		Slow, V_{CC}=3V MODE3V=1 PWRSAV=0	SXT=32 KHz	–	54	–	
			SRC=24 KHz	–	50	–	
		Idle, V_{CC}=5V LVR enable MODE3V=0	SXT=32 KHz	–	205	–	
			SRC=24 KHz	–	195	–	
		Idle, V_{CC}=3V LVR enable MODE3V=0	SXT=32 KHz	–	168	–	
			SRC=24 KHz	–	166	–	
		Idle, V_{CC}=3V MODE3V=1 PWRSAV=1	SXT=32 KHz	–	5	–	
			SRC=24 KHz	–	3	–	
		Idle, V_{CC}=3V MODE3V=1 PWRSAV=0	SXT=32 KHz	–	46	–	
			SRC=24 KHz	–	43	–	
		Stop, V_{CC}=5V LVR disable MODE3V=0	PWRSAV=1	–	0.1	–	
			PWRSAV=0	–	158	–	
		Stop, V_{CC}=3V LVR disable MODE3V=0	PWRSAV=1	–	–	0.1	
			PWRSAV=0	–	136	–	
		Stop, V_{CC}=5V LVR enable MODE3V=0	PWRSAV=1	–	1.7	–	
			PWRSAV=0	–	194	–	
		Stop, V_{CC} = 3V LVR enable MODE3V=0	PWRSAV=1	–	0.5	–	
			PWRSAV=0	–	165	–	
		Stop, V_{CC}=3V MODE3V=1	LVR disable	–	–	0.1	
			LVR enable PWRSAV=1	–	0.5	–	
			LVR enable PWRSAV=0	–	41	–	

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
System Clock Frequency	F_{SYSCLK}	V_{CC}>LVR_{th}	V_{CC}=2.9V	–	–	8	MHz
			V_{CC}=2.3V	–	–	7.3728	
			V_{CC}=2.0V	–	–	4	
LVR Reference Voltage	V_{LVR}	T_A=25°C		+3%	2.9	+3%	V
				+3%	2.3	+3%	
				-8%	1.8	+8%	
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
LVD Reference Voltage	V_{LVD}	T_A=25°C		–	2.3	–	V
Low Voltage Detection time	t_{LVR}	T_A=25°C		100	–	–	µs
Pull-Up Resistor	R_P	V_{IN}=0V All except P3.7	V_{CC}=5V	–	120	–	KΩ
			V_{CC}=3V		240		
		V_{IN}=0V P3.7	V_{CC}=5V	–	170	–	
			V_{CC}=3V		170		

3. Clock Timing (T_A= –40°C ~ +85°C, V_{CC}=2.6V ~ 5.5V)

Parameter	Conditions	Min.	Typ.	Max.	Unit
Internal RC Frequency	25°C, V_{CC}=3.0 ~ 5.5V	7.142	7.3728	7.6032	MHz
	25°C, V_{CC}=2.6 ~ 3.0V	7.004	7.3728	7.7414	
	–40°C ~ 85°C, V_{CC}=2.6 ~ 5.5V	6.192	7.3728	7.8336	

4. Reset Timing Characteristics (T_A= –40°C ~ +85°C, V_{CC}=3.0V ~ 5.0V)

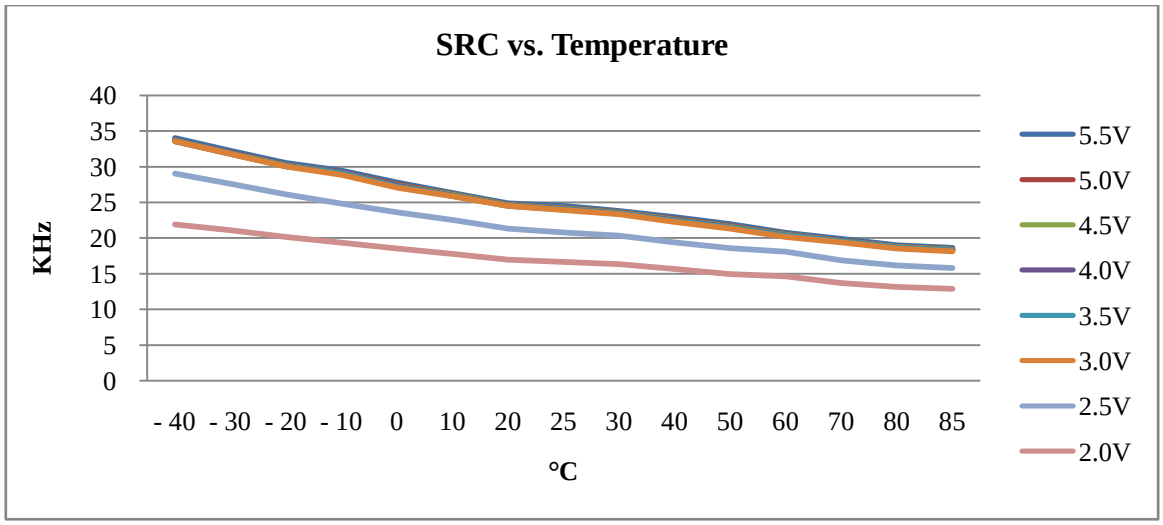
Parameter	Conditions	Min.	Typ.	Max.	Unit
RESET Input Low width	Input V_{CC}=5.0V ±10 %	90	–	–	µs
WDT wakeup time	V_{CC}=5.0V, WDTPSC=11	–	40	–	ms
	V_{CC}=3.0V, WDTPSC=11	–	40	–	

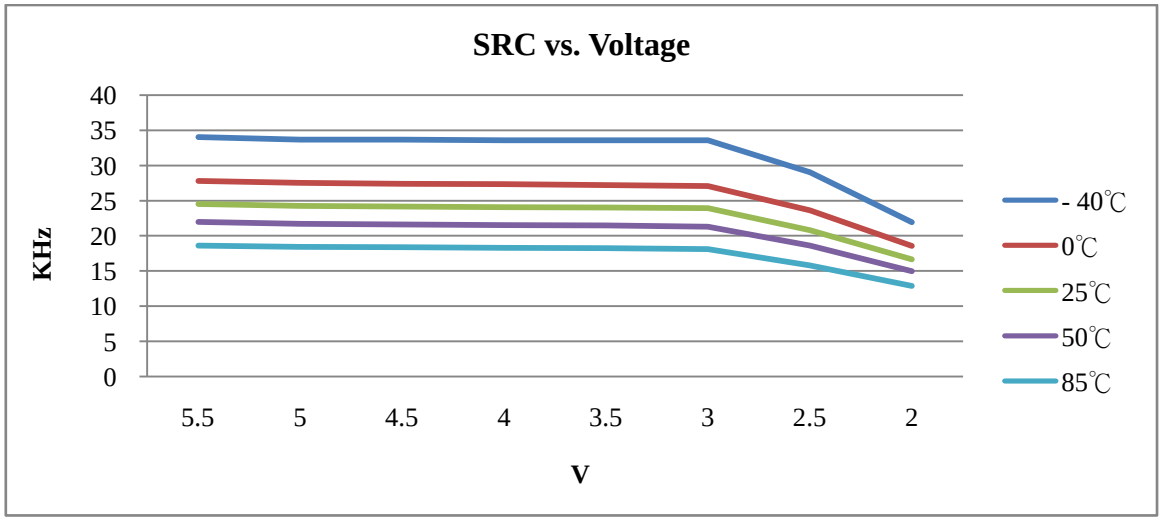
5. ADC Electrical Characteristics (T_A=25°C, V_{CC}=3.0V ~ 5.5V, V_{SS}=0V)

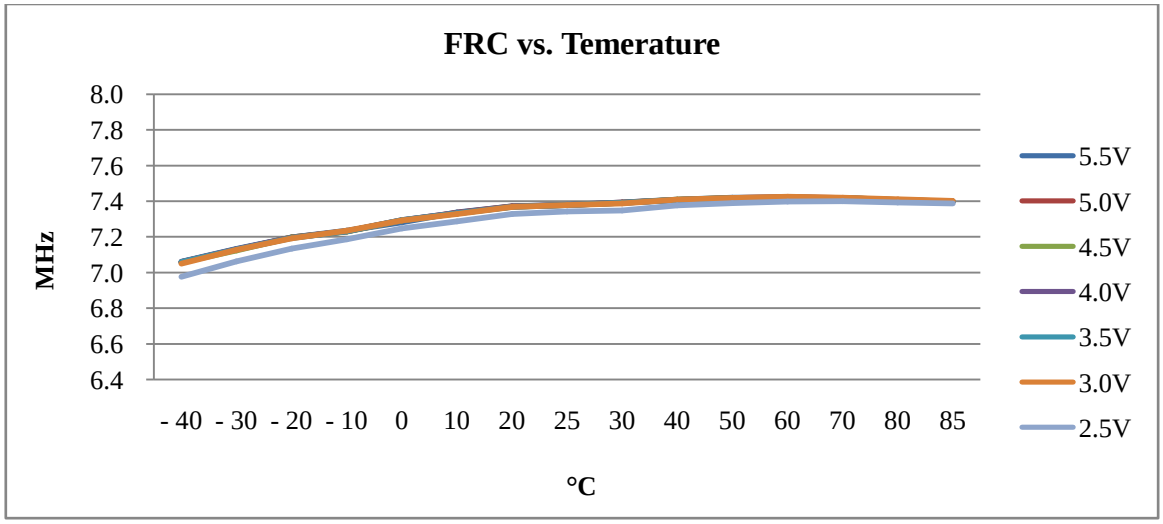
Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Accuracy	V_{CC}=5.12V, V_{SS}=0V	–	±2.5	±4	LSB
Integral Non-Linearity		–	±3.2	±5	
Max Input Clock (f_{ADC})	–	–	–	1	MHz
Conversion Time	f_{ADC}=1 MHz	–	50	–	µs
BandGap Voltage Reference	V_{CC}=3V	1.14	1.22	1.30	V
	V_{CC}=5V	1.15	1.25	1.35	
Input Voltage	–	V_{SS}	–	V_{CC}	V

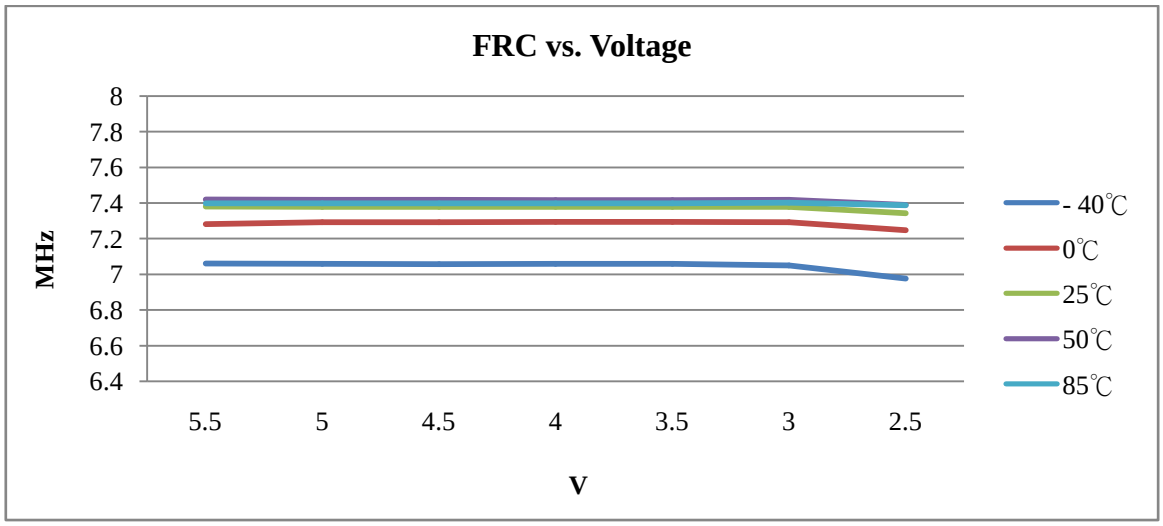
Note: also refer to AP-TM52XXXXX_05S for using ADC to trim BandGap.

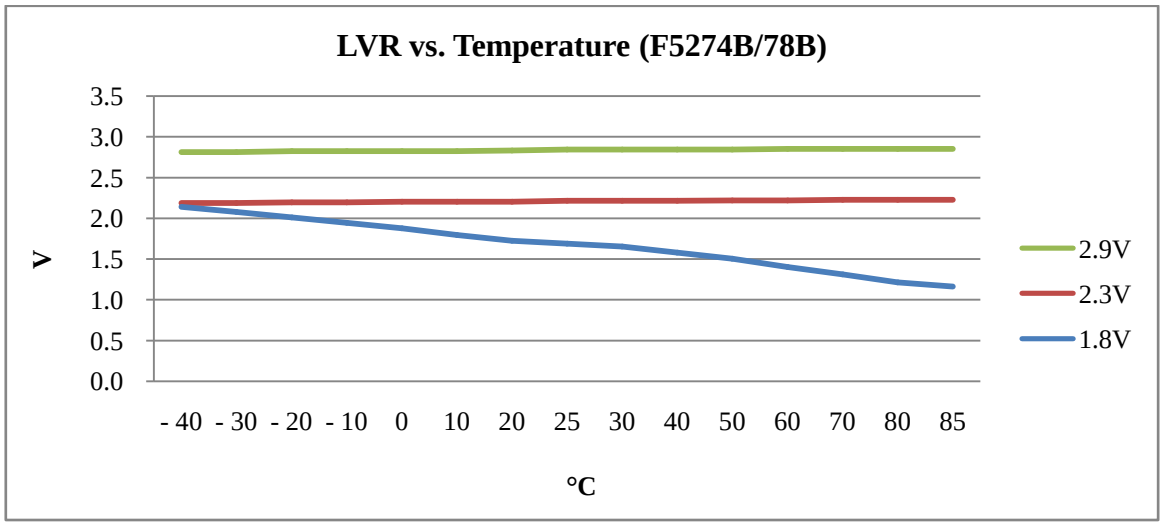
6. Characteristics Graphs

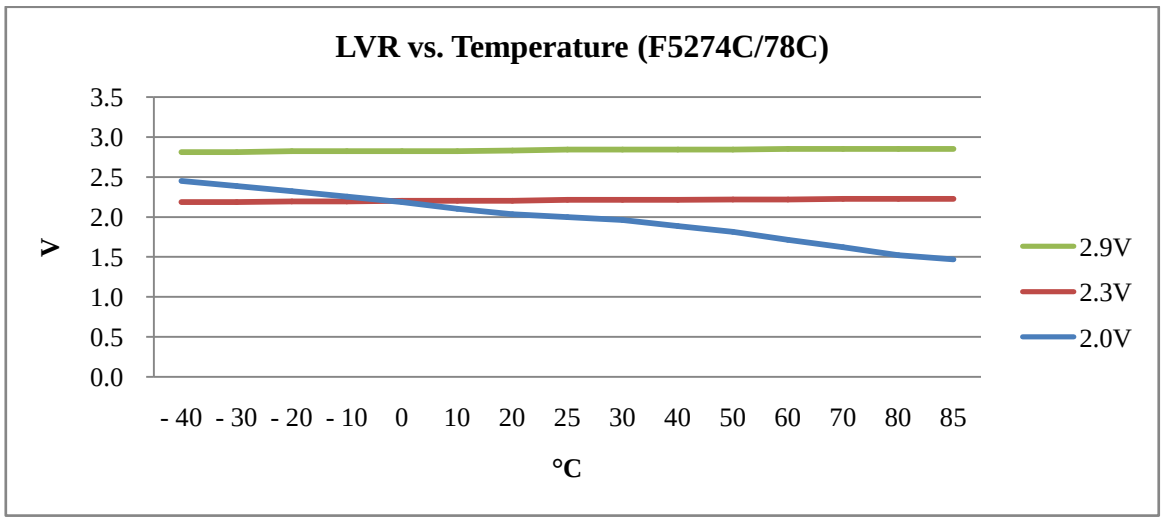












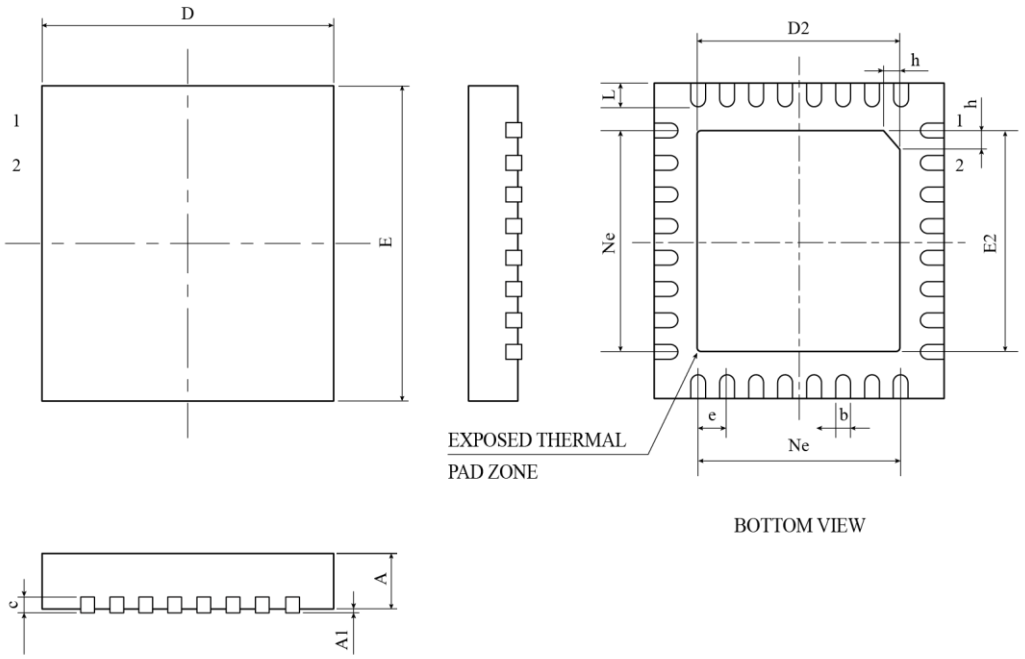
Note: Due to the variation of manufacturing process, this LVR will slightly vary between different chips.

Package Information

Ordering Information

Ordering Number	Package
TM52F0200-MTP-98	QFN32 Pin (5*5*0.75mm)
TM52F0200-COD-98	QFN32 Pin (5*5*0.75mm)

QFN 32 pin(5*5*0.75 – 0.5mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	--	0.02	0.05	--	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
c	0.18	0.20	0.25	0.007	0.008	0.010
D	4.90	5.00	5.10	0.193	0.197	0.201
D2	3.40	3.50	3.60	0.134	0.138	0.142
e	0.50 BSC			0.020 BSC		
Ne	3.50 BSC			0.138 BSC		
E	4.90	5.00	5.10	0.193	0.197	0.201
E2	3.40	3.50	3.60	0.134	0.138	0.142
L	0.35	0.40	0.45	0.014	0.016	0.018
h	0.30	0.35	0.40	0.012	0.014	0.016