十速科技股份有限公司
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TM87P18M

4-Bit Microcontroller

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	Jul, 2012	New release

CONTENTS

GENERAL DESCRIPTION

The TM87P18M is a One Time PROM embedded high-performance 4-bit microcontroller with LCD driver. It contains all the following functions on a single chip: 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, Resistance to Frequency Converter (RFC), LCD driver, look-up table, watchdog timer and key matrix scanning circuitry.

FEATURES

1. Powerful instruction set (173 instructions).

- Binary addition, subtraction, BCD adjusts, logical operation in direct and index addressing mode.
- Single-bit manipulation (set, reset, decision for branch).
- Various conditional branches.
- 16 working registers and manipulation.
- Table look-up.
- LCD driver data transfer.

2. Memory capacity.

- ROM capacity 4096 x 16 bits
- Data RAM capacity 512 x 4 bits.

3. Input/output ports.

- Port IOA 4 pins (with internal pull-low), muxed with SEG24~SEG27.
- Port IOB 4 pins (with internal pull-low), muxed with SEG28~SEG30, DC31.
- Port IOC 4 pins (with internal pull-low, low-level-hold, chattering prevention clock).
- Port IOD 4 pins (with internal pull-low, chattering prevention clock).

4. 8-level subroutine nesting.

5. Interrupt function.

- External factor 4 (INT pin, Port IOC, IOD & KI input).
- Internal factor 4 (Pre-Divider, Timer1, Timer2, RFC).

6. Built-in Alarm, Frequency or Melody generator.

7. BZB, BZ (Mux with IOB3/SEG30, IOB4/DC31).

8. Built-in R to F Converter circuit.

- CX, RR, RT, RH (Mux with IOA1~IOA4/SEG24~27).

9. Built-in KEY_BOARD scanning function.

- K1~K16 (Share with SEG1~SEG16).
- KI1~KI4 (Mux with IOC1~IOC4).

10. Two 6-bit programmable timers with programmable clock source.

11. Watch dog timer.

12. LCD driver output.

- 32 LCD/LED driver outputs (up to 256 LCD segment drivable).
- 1/2 ~ 1/8 Duty for LCD/LED.
- 1/2 Bias or 1/3 Bias for LCD/LED selected by option.
- Single instruction to turn off all segments.
- Option is used to select COM5~8, DC9/OD9, SEG17~ SEG23, DC31/OD31,SEG40, SEG41,as DC outputs/P_open drain.
- 32 LCD address.

13. Built-in Voltage doubler, halver charge pump circuit.

14. Dual clock operation, and X'tal type slow oscillation, and fast oscillation can set 3.58 MHz ceramic resonator, internal R or external R by switch option.

15. HALT function.

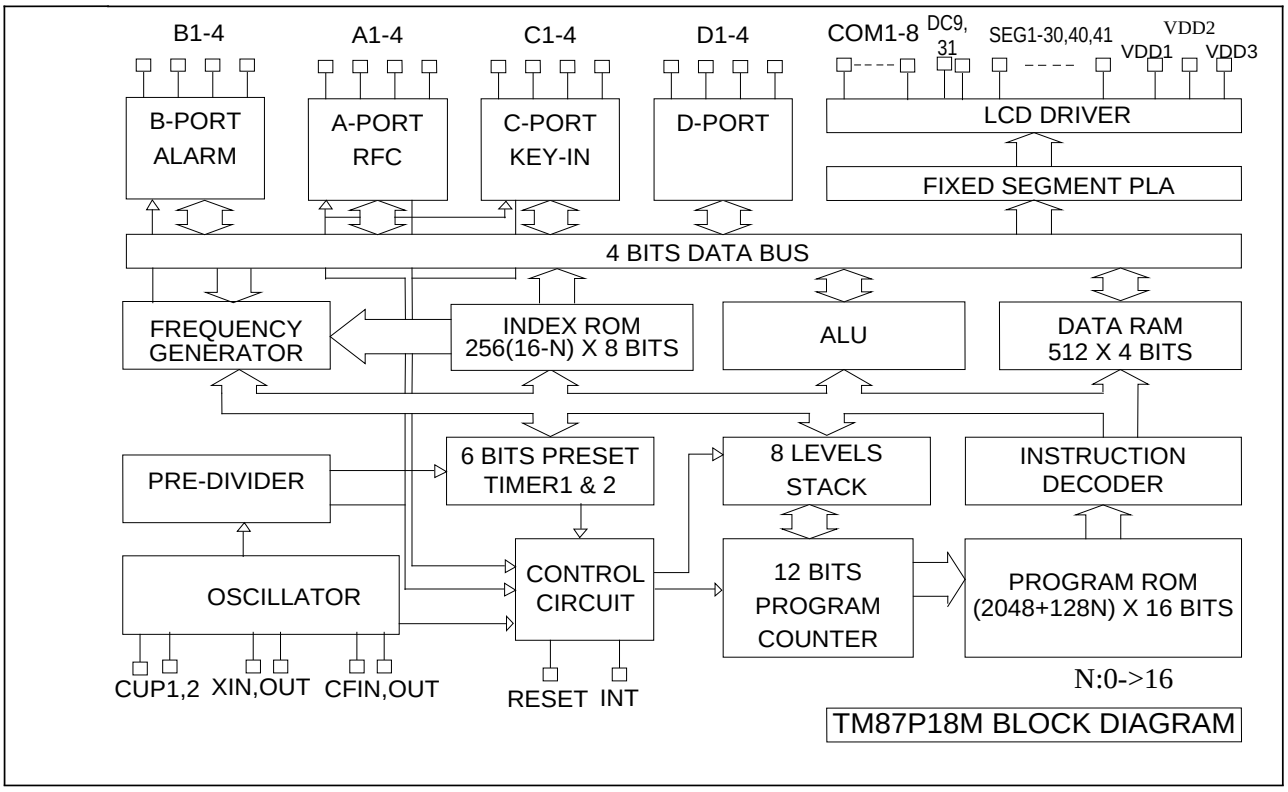
16. STOP function.

17. ROM code protect fuse.

APPLICATION

■ Timer / Calendar / Calculator

BLOCK DIAGRAM



PIN ASSIGNMENT

No	Name	No	Name
1	BAK	33	SEG13 (K13)
2	XIN	34	SEG14 (K14)
3	XOUT	35	SEG15 (K15)
4	CFIN	36	SEG16 (K16)
5	CFOUT	37	SEG17/DC17/OD17
6	GND	38	SEG18/DC18/OD18
7	VDD1	39	SEG19/DC19/OD19
8	VDD2	40	SEG20/DC20/OD20
9	VDD3	41	SEG21/DC21/OD21
10	CUP1	42	SEG22/DC22/OD22
11	CUP2	43	SEG23/DC23/OD23
12	COM1	44	SEG24/IOA1/CX
13	COM2	45	SEG25/IOA2/RR
14	COM3	46	SEG26/IOA3/RT
15	COM4	47	SEG27/IOA4/RH
16	COM5/DC5/OD5	48	SEG28/IOB1
17	COM6/DC6/OD6	49	SEG29/IOB2
18	COM7/DC7/OD7	50	SEG30/IOB3/BZB
19	COM8/DC8/OD8	51	DC31/OD31/IOB4/BZ
20	DC9/OD9	52	IOC1/KI1
21	SEG1 (K1)	53	IOC2/KI2
22	SEG2 (K2)	54	IOC3/KI3
23	SEG3 (K3)	55	IOC4/KI4
24	SEG4 (K4)	56	IOD1
25	SEG5 (K5)	57	IOD2
26	SEG6 (K6)	58	IOD3
27	SEG7 (K7)	59	IOD4
28	SEG8 (K8)	60	SEG40/DC40/OD40
29	SEG9 (K9)	61	SEG41/DC41/OD41
30	SEG10 (K10)	62	RESET
31	SEG11 (K11)	63	INT
32	SEG12 (K12)	64	VPP

PIN DESCRIPTION

Name	I/O	Description
BAK	P	Positive Back-up voltage, connect a 0.1u capacitor to GND. Positive voltage is needed to BAK pin for Serial Program/Read Mode.
VDD2	P	Positive supply voltage. Connect +3.0V battery positive pin to VDD2. Positive voltage is needed to VDD2 for Serial Program/Read Mode.
VDD1, 3	P	LCD supply voltage, and positive supply voltage. Positive voltage is needed to VDD3 for Serial Program/Read Mode.
RESET	I	Input pin from LSI reset request signal, with internal pull-down resistor. Instruction Reset Time can select “PH15/2” or “PH12/2” by option. Reset Type can select “Level” or “Pulse” by option. Signal for Serial Program/Read Mode.
INT	I I/O	Input pin for external INT request signal. Falling edge or rising edge triggered by option. Internal pull-down or pull-up resistor is selected by option. Signal for Serial Program/Read Mode.
CUP1, 2	O	Switching pins for supply the LCD driving voltage to the VDD1, VDD2, VDD3 pins. Connect the CUP1 and CUP2 pins with non-polarized electrolytic capacitor if 1/2 or 1/3 bias mode has been selected. In no BIAS mode, these pins should be open.
XIN XOUT	**I** O	Low speed oscillator, generates clock for time base functions (clock specified, LCD alternating frequency, Alarm signal frequency) or system clock oscillation. 32 KHz Crystal oscillator for Slow Clock.
CFIN CFOUT	**I** O	High speed oscillator, system clock oscillation for FAST clock only or DUAL clock operation. The usage of 3.58 MHz ceramic/resonator oscillator or external R type oscillator is defined by mask option
COM1~8	O	Output pins for driving the common pins of the LCD or LED panel. COM5~8 is muxed with DC/Open Drain, and set mask option
DC9,31	O	DC/Open Drain,
SEG1-30,40, 41	O	Output pins for driving the LCD or LED panel segment.
IOA1-4	I/O	Input / Output port A, can use software to define internal pull-low Resistor. This port is muxed with SEG24~27, and set by option.
IOB1-4	I/O	Input / Output port B, can use software to define internal pull-low Resistor. This port is muxed with SEG28~30, DC31 / BZB, BZ, and set by option.
IOC1-4	I/O	Input / Output port C, can use software to define internal pull-low / low-level-hold Resistor and Chattering clock to reduce input bounce. This port is muxed with KI1~4, and set by option.
IOD1-4	I/O	Input / Output port D, can use software to define internal pull-low Resistor, and Chattering clock to reduce input bounce.
(RFC)CX RR/RT/RH	I O	1 input pin and 3 output pins for RFC application. This port is muxed with SEG24~27 / IOA1~4, and set by option.
(ALM) BZB/BZ	 O	Output port for alarm, frequency or melody generator This port is muxed with SEG 30, DC 31 / IOB3, 4, and set by option.
KI1~4	I	Keyboard scanning input port. This port is muxed with IOC1~4, and set by option.
GND	P	Negative supply voltage. Connect for Serial Program/Read Mode.
VPP	P	High Voltage is need to VPP for Serial Program/Read Mode. Connected VDD2 to VPP or floating for Normal Mode.

Serial Program/Read Connect Pins:

VPP, VDD2, VDD3, GND, RESET, INT, BAK

Configuration of LCD RAM Area

	< 1/8 Duty >									
SEG	Lz	COM1	COM2	COM3	COM4	Lz	COM5	COM6	COM7	COM8
SEG1	00H	DBUSA	DBUSB	DBUSC	DBUSD	10H	DBUSA	DBUSB	DBUSC	DBUSD
SEG2		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG3	01H	DBUSA	DBUSB	DBUSC	DBUSD	11H	DBUSA	DBUSB	DBUSC	DBUSD
SEG4		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG5	02H	DBUSA	DBUSB	DBUSC	DBUSD	12H	DBUSA	DBUSB	DBUSC	DBUSD
SEG6		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG7	03H	DBUSA	DBUSB	DBUSC	DBUSD	13H	DBUSA	DBUSB	DBUSC	DBUSD
SEG8		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG9	04H	DBUSA	DBUSB	DBUSC	DBUSD	14H	DBUSA	DBUSB	DBUSC	DBUSD
SEG10		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG11	05H	DBUSA	DBUSB	DBUSC	DBUSD	15H	DBUSA	DBUSB	DBUSC	DBUSD
SEG12		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG13	06H	DBUSA	DBUSB	DBUSC	DBUSD	16H	DBUSA	DBUSB	DBUSC	DBUSD
SEG14		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG15	07H	DBUSA	DBUSB	DBUSC	DBUSD	17H	DBUSA	DBUSB	DBUSC	DBUSD
SEG16		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG17	08H	DBUSA	DBUSB	DBUSC	DBUSD	18H	DBUSA	DBUSB	DBUSC	DBUSD
SEG18		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG19	09H	DBUSA	DBUSB	DBUSC	DBUSD	19H	DBUSA	DBUSB	DBUSC	DBUSD
SEG20		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG21	0AH	DBUSA	DBUSB	DBUSC	DBUSD	1AH	DBUSA	DBUSB	DBUSC	DBUSD
SEG22		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG23	0BH	DBUSA	DBUSB	DBUSC	DBUSD	1BH	DBUSA	DBUSB	DBUSC	DBUSD
SEG24		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG25	0CH	DBUSA	DBUSB	DBUSC	DBUSD	1CH	DBUSA	DBUSB	DBUSC	DBUSD
SEG26		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG27	0DH	DBUSA	DBUSB	DBUSC	DBUSD	1DH	DBUSA	DBUSB	DBUSC	DBUSD
SEG28		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG29	0EH	DBUSA	DBUSB	DBUSC	DBUSD	1EH	DBUSA	DBUSB	DBUSC	DBUSD
SEG30		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH
SEG40	0FH	DBUSA	DBUSB	DBUSC	DBUSD	1FH	DBUSA	DBUSB	DBUSC	DBUSD
SEG41		DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH

LZ					LZ				
20H	**SEG17 DC/OD**	**SEG18 DC/OD**	**SEG19 DC/OD**	**SEG20 DC/OD**	21H	**COM5 DC5/OD5**	**COM6 DC6/OD6**	**COM7 DC7/OD7**	**COM8 DC8/OD8**
	DBUSA	DBUSB	DBUSC	DBUSD		DBUSA	DBUSB	DBUSC	DBUSD
	SEG21 DC/OD	**SEG22 DC/OD**	**SEG23 DC/OD**			**DC9/OD9**	**DC31/OD31**	**SEG40 DC/OD**	**SEG41 DC/OD**
	DBUSE	DBUSF	DBUSG	DBUSH		DBUSE	DBUSF	DBUSG	DBUSH

※ Duty 1/8:COM1~8, Duty 1/7:COM1~7…

ABSOLUTE MAXIMUM RATINGS

(GND= 0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 5.5	V
	VDD2	-0.3 to 5.5	V
	VDD3	-0.3 to 8.5	V
	VPP	-0.3 to 13.5	V
Maximum Input Voltage	Vin	-0.3 to VDD1/VDD2+0.3	V
Maximum Output Voltage	Vout1	-0.3 to VDD1/VDD2+0.3	V
	Vout2	-0.3 to VDD3+0.3	V
Maximum Operating Temperature	Topg	-40 to +80	℃
Maximum Storage Temperature	Tstg	-25 to +125	℃

POWER CONSUMPTION

At VDD2= 3.0V, Ta=-40℃ to 80℃, GND= 0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT	Only 32.768 KHz Crystal oscillator operating, without loading. BCF = 0, 1/4 duty, ph0=BCLK		3	6	uA
STOP mode	ISTOP				1	uA
Normal Mode	I_{32K}	Only 32.768 KHz Crystal oscillator operating, without loading. BCF = 0, 1/4 duty, ph0=BCLK	8			uA
External R	$I_{Ext.\ R}$	R = 150 KΩ oscillator operating, without loading. BCF = 0, 1/4 duty, ph0=BCLK	36			uA
3.58MHz ceramic resonator	$I_{3.58Mcr}$	Only 3.58 MHz ceramic resonator operating, without loading. BCF = 0, 1/4 duty, ph0=BCLK	480			uA

Note: When External R oscillator mode is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

At Ta=-40℃ to 80℃,GND= 0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD2		2.4	5.25	V
	VDD3		2.4	8.0	V
	VPP		2.4	12.5	V
Oscillator Start-Up Voltage	VDD_{stup}	32.768 KHz Crystal Mode	1.4		V
		3.58 ceramic resonator Mode	1.8		V
Oscillator Sustain Voltage	VDD_{sut}	32.768 KHz Crystal Mode	1.3		V
		3.58 ceramic resonator Mode	1.55		V
Supply Voltage	VDD2	Li Mode	2.4	3.6	V
Input “H” Voltage	Vih1	Li Battery Mode	VDD2-0.7	VDD2+0.7	V
Input “L” Voltage	Vil1		-0.7	0.7	V
Input “H” Voltage	Vih2	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	V
Input “L” Voltage	Vil2		0	0.2xVDD2	V
Input “H” Voltage	Vih3	CFIN at Li Battery	0.8xVDD2	VDD2	V
Input “L” Voltage	Vil3		0	0.2xVDD2	V
Operating Freq	Fopg1	32.768 KHz Crystal Mode	32		KHz
	Fopg2	External R mode	10	1000	KHz

ALLOWABLE OPERATING FREQUENCY

At Ta=-40℃ to 80℃, GND= 0V

Condition	Max. Operating Frequency
BAK=3V	4 MHz

ELECTRICAL CHARACTERISTICS

At#1:VDD2=3.0V(Li); at#2:VDD2=5.0V;

Input Resistance

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
“L” Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD2,#1	10	40	100	KΩ
	Rllh2	Vi=0.2VDD2,#2	5	20	50	KΩ
IOA,B,C Pull-Down Tr	Rmad1	Vi=VDD2,#1	200	500	1000	KΩ
	Rmad2	Vi=VDD2,#2	100	250	500	KΩ
INT Pull-up Tr	Rintu1	Vi=VDD2,#1	200	500	1000	KΩ
	Rintu2	Vi=VDD2,#2	100	250	500	KΩ
INT Pull-Down Tr	Rintd1	Vi=GND,#1	200	500	1000	KΩ
	Rintd2	Vi=GND,#2	100	250	500	KΩ
RES Pull-Down R	Rres	Vi=GND or VDD2,#1,#2	10	45	100	KΩ

DC Output Characteristics

At#3:VDD2=2.4V(Li); At#4:VDD2=4.0V;

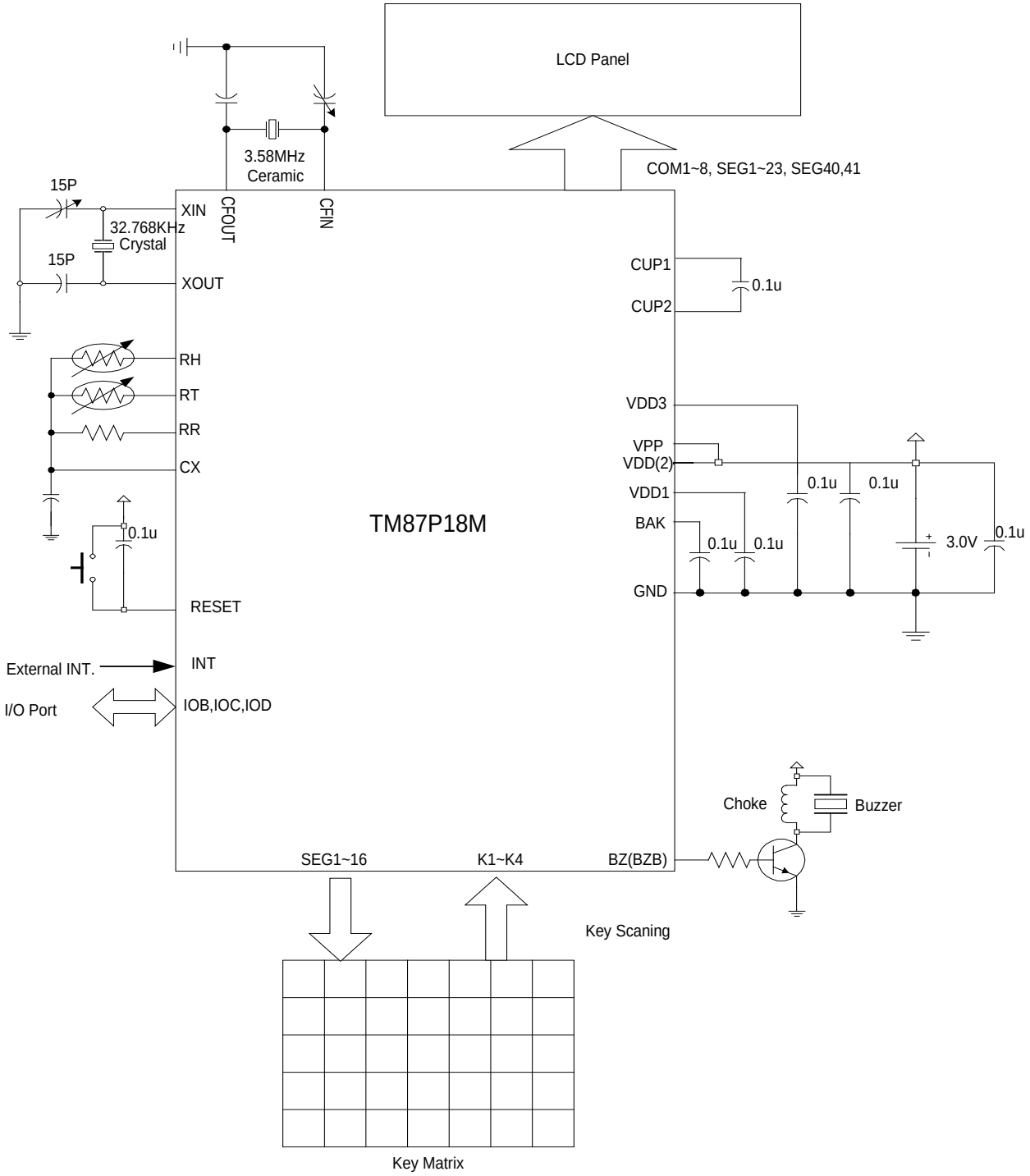
Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output “H” Voltage	Voh3c	Ioh=-1 mA,#3	COM5~8,DC9 SEG28~30,DC31, SEG40,41, IOC, IOD	2.0			V
	Voh4c	Ioh=-3 mA,#4		3.2			V
Output “L” Voltage	Vol3c	Iol=2 mA,#3				0.4	V
	Vol4c	Iol=6 mA,#4				0.8	V
Output “H” Voltage	Voh3c	Ioh=-3 mA,#3	SEG24~27,INT	2.0			V
	Voh4c	Ioh=-5 mA,#4		3.2			V
Output “L” Voltage	Vol3c	Iol=5 mA,#3				0.4	V
	Vol4c	Iol=10 mA,#4				0.8	V

Segment Driver Output Characteristics

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output “H” Voltage	Voh3f	Ioh=-1 uA,#3	SEG-n	2.2			V
	Voh4f	Ioh=-1 uA,#4		3.8			V
Output “L” Voltage	Vol3f	Iol=1 uA,#3				0.2	V
	Vol4f	Iol=1 uA,#4				0.2	V
Output “H” Voltage	Voh3g	Ioh=-10 uA,#3	COM-n	2.2			V
	Voh4g	Ioh=-10 uA,#4		3.8			V
Output “M” Voltage	Vom3g	Iol/h=+/-10 uA,#3	COM-n	1.0		1.4	V
	Vom4g	Iol/h=+/-10 uA,#4		1.8		2.2	V
Output “L” Voltage	Vol3g	Iol=10 uA,#3				0.2	V
	Vol4g	Iol=10 uA,#4				0.2	V
1/3 Bias display Mode							
Output “H” Voltage	Voh3i	Ioh=-1 uA,#3	SEG-n	3.4			V
	Voh4i	Ioh=-1 uA,#4		5.8			V
Output “M1” Voltage	Vom13i	Iol/h=+/-10 uA,#3		1.0		1.4	V
	Vom14i	Iol/h=+/-10 uA,#4		1.8		2.2	V
Output “M2” Voltage	Vom23i	Iol/h=+/-10 uA,#3		2.2		2.6	V
	Vom24i	Iol/h=+/-10 uA,#4		3.8		4.2	V
Output “L” Voltage	Vol3i	Iol=1 uA,#3				0.2	V
	Vol4i	Iol=1 uA,#4				0.2	V
Output “H” Voltage	Voh3j	Ioh=-10 uA,#3	COM-n	3.4			V
	Voh4j	Ioh=-10 uA,#4		5.8			V
Output “M1” Voltage	Vom13j	Iol/h=+/-10 uA,#3		1.0		1.4	V
	Vom14j	Iol/h=+/-10 uA,#4		1.8		2.2	V
Output “M2” Voltage	Vom23j	Iol/h=+/-10 uA,#3		2.2		2.6	V
	Vom24j	Iol/h=+/-10 uA,#4		3.8		4.2	V
Output “L” Voltage	Vol3j	Iol=10 uA,#3				0.2	V
	Vol4j	Iol=10 uA,#4				0.2	V

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



1/3 Bias, 1/8Duty

INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 001Z ZZZZ ZYYY	Lz	← (7SEG ← Ry)	(Ry=70H~77H) LZ page: 00~21h
LCB	Lz,Ry	0000 010Z ZZZZ ZYYY	Lz	← (7SEG ← Ry) Blank Zero	(Ry=70H~77H) LZ page: 00~21h
LCP	Lz,Ry	0000 011Z ZZZZ ZYYY	Lz	← Ry & AC	(Ry=70H~77H) LZ page: 00~21h
LCD	Lz,@HL	0000 100Z ZZZZ Z000	Lz	← T@HL	LZ page: 00~21h
LCT	Lz,@HL	0000 100Z ZZZZ Z001	Lz	← (7SEG ← @HL)	LZ page: 00~21h
LCB	Lz,@HL	0000 100Z ZZZZ Z010	Lz	← (7SEG ← @HL) Blank Zero	LZ page: 00~21h
LCP	Lz,@HL	0000 100Z ZZZZ Z011	Lz	← @HL & AC	LZ page: 00~21h
OPA	Rx	0000 1010 0XXX XXXX	Port(A)	← Rx	
OPAS	Rx,D	0000 1011 DXXX XXXX	A1,2,3,4	← Rx0,Rx1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port(B)	← Rx	
OPC	Rx	0000 1101 0XXX XXXX	Port(C)	← Rx	
OPD	Rx	0000 1110 0XXX XXXX	Port(D)	← Rx	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D,@HL	0001 01DD 0000 0000	FREQ	←T@HL	
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	IDBF0~3	← Rx	
MVH	Rx	0001 1101 0XXX XXXX	IDBF4~7	← Rx	
MVU	Rx	0001 1110 0XXX XXXX	IDBF8~11	← Rx	
ADC	Rx	0010 0000 0XXX XXXX	AC	← Rx + AC + CF	CF
ADC	@HL	0010 0000 1000 0000	AC	← @HL + AC + CF	CF
ADC#	@HL	0010 0000 1100 0000	AC HL	← @HL + AC + CF ←HL+1	CF
ADC*	Rx	0010 0001 0XXX XXXX	AC,Rx	← Rx + AC + CF	CF
ADC*	@HL	0010 0001 1000 0000	AC,@HL	← @HL + AC + CF	CF
ADC*#	@HL	0010 0001 1100 0000	AC,@HL HL	← @HL + AC + CF ←HL+1	CF
SBC	Rx	0010 0010 0XXX XXXX	AC	← Rx + ACB + CF	CF
SBC	@HL	0010 0010 1000 0000	AC	← @HL + ACB + CF	CF
SBC#	@HL	0010 0010 1100 0000	AC HL	← @HL + ACB + CF ←HL+1	CF
SBC*	Rx	0010 0011 0XXX XXXX	AC,Rx	← Rx + ACB + CF	CF
SBC*	@HL	0010 0011 1000 0000	AC,@HL	← @HL + ACB + CF	CF
SBC*#	@HL	0010 0011 1100 0000	AC,@HL HL	← @HL + ACB + CF ←HL+1	CF
ADD	Rx	0010 0100 0XXX XXXX	AC	← Rx + AC	CF
ADD	@HL	0010 0100 1000 0000	AC	← @HL + AC	CF
ADD#	@HL	0010 0100 1100 0000	AC HL	← @HL + AC ←HL+1	CF
ADD*	Rx	0010 0101 0XXX XXXX	AC,Rx	← Rx + AC	CF
ADD*	@HL	0010 0101 1000 0000	AC,@HL	← @HL + AC	CF

Instruction		Machine Code	Function		Flag/Remark
ADD*#	@HL	0010 0101 1100 0000	AC,@HL HL	← @HL + AC ←HL+1	CF
SUB	Rx	0010 0110 0XXX XXXX	AC	← Rx + ACB + 1	CF
SUB	@HL	0010 0110 1000 0000	AC	← @HL + ACB + 1	CF
SUB#	@HL	0010 0110 1100 0000	AC HL	← @HL + ACB + 1 ←HL+1	CF
SUB*	Rx	0010 0111 0XXX XXXX	AC,Rx	← Rx + ACB + 1	CF
SUB*	@HL	0010 0111 1000 0000	AC,@HL	← @HL + ACB + 1	CF
SUB*#	@HL	0010 0111 1100 0000	AC,@HL HL	← @HL + ACB + 1 ←HL+1	CF
ADN	Rx	0010 1000 0XXX XXXX	AC	← Rx + AC	
ADN	@HL	0010 1000 1000 0000	AC	← @HL + AC	
ADN#	@HL	0010 1000 1100 0000	AC HL	← @HL + AC ←HL+1	
ADN*	Rx	0010 1001 0XXX XXXX	AC,Rx	← Rx + AC	
ADN*	@HL	0010 1001 1000 0000	AC,@HL	← @HL + AC	
ADN*#	@HL	0010 1001 1100 0000	AC,@HL HL	← @HL + AC ←HL+1	
AND	Rx	0010 1010 0XXX XXXX	AC	← Rx AND AC	
AND	@HL	0010 1010 1000 0000	AC	← @HL AND AC	
AND#	@HL	0010 1010 1100 0000	AC HL	← @HL AND AC ←HL+1	
AND*	Rx	0010 1011 0XXX XXXX	AC,Rx	← Rx AND AC	
AND*	@HL	0010 1011 1000 0000	AC,@HL	← @HL AND AC	
AND*#	@HL	0010 1011 1100 0000	AC,@HL HL	← @HL AND AC ←HL+1	
EOR	Rx	0010 1100 0XXX XXXX	AC	← Rx EOR AC	
EOR	@HL	0010 1100 1000 0000	AC	← @HL EOR AC	
EOR#	@HL	0010 1100 1100 0000	AC HL	← @HL EOR AC ←HL+1	
EOR*	Rx	0010 1101 0XXX XXXX	AC,Rx	← Rx EOR AC	
EOR*	@HL	0010 1101 1000 0000	AC,@HL	← @HL EOR AC	
EOR*#	@HL	0010 1101 1100 0000	AC,@HL HL	← @HL EOR AC ←HL+1	
OR	Rx	0010 1110 0XXX XXXX	AC	← Rx OR AC	
OR	@HL	0010 1110 1000 0000	AC	← @HL OR AC	
OR#	@HL	0010 1110 1100 0000	AC HL	← @HL OR AC ←HL+1	
OR*	Rx	0010 1111 0XXX XXXX	AC,Rx	← Rx OR AC	
OR*	@HL	0010 1111 1000 0000	AC,@HL	← @HL OR AC	
OR*#	@HL	0010 1111 1100 0000	AC,@HL HL	← @HL OR AC ←HL+1	
ADCI	Ry,D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC,Ry	← Ry + D + CF	
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC,Ry	← Ry + DB + CF	
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	← Ry + D	
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC,Ry	← Ry + D	
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC,Ry	← Ry + DB + 1	
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	← Ry + D	

Instruction		Machine Code	Function		Flag/Remark
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC,Ry	← Ry + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC,Ry	← Ry AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC,Ry	← Ry EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC,Ry	← Ry OR D	
INC*	Rx	0100 0000 0XXX XXXX	AC,Rx	← Rx + 1	CF
INC*	@HL	0100 0000 1000 0000	AC,@HL	← @HL + 1	CF
INC*#	@HL	0100 0000 1100 0000	AC,@HL HL	← @HL + 1 ←HL+1	CF
DEC*	Rx	0100 0001 0XXX XXXX	AC,Rx	← Rx – 1	CF
DEC*	@HL	0100 0001 1000 0000	AC,@HL	← @HL - 1	CF
DEC*#	@HL	0100 0001 1100 0000	AC,@HL HL	← @HL - 1 ←HL+1	CF
IPA	Rx	0100 0010 0XXX XXXX	AC,Rx	← Port(A)	
IPB	Rx	0100 0100 0XXX XXXX	AC,Rx	← Port(B)	
IPC	Rx	0100 0111 0XXX XXXX	AC,Rx	← Port(C)	
IPD	Rx	0100 1000 0XXX XXXX	AC,Rx	← Port(D)	
MAF	Rx	0100 1010 0XXX XXXX	AC,Rx	← STS1	B3 : CF B2 : ZERO B1 : (No use) B0 : (No use)
MSB	Rx	0100 1011 0XXX XXXX	AC,Rx	← STS2	B3 : SCF3(DPT) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF
MSC	Rx	0100 1100 0XXX XXXX	AC,Rx	← STS3	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT)
MCX	Rx	0100 1101 0XXX XXXX	AC,Rx	← STS3X	B3 : SCF9(RFC) B2 : (unused) B1 : SCF6(TM2) B0 : SCF8(SKI)
MSD	Rx	0100 1110 0XXX XXXX	AC,Rx	← STS4	B3 : (No use) B2 : FROVF B1 : WDF B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD(AC)	CF
DAA*	Rx	0101 0101 0XXX XXXX	AC,Rx	← BCD(AC)	CF
DAA*	@HL	0101 0101 1000 0000	AC,@HL	← BCD(AC)	CF
DAA*#	@HL	0101 0101 1100 0000	AC,@HL HL	← BCD(AC) ←HL+1	CF

Instruction		Machine Code	Function		Flag/Remark
DAS		0101 0110 0000 0000	AC	← BCD(AC)	CF
DAS*	Rx	0101 0111 0XXX XXXX	AC,Rx	← BCD(AC)	CF
DAS*	@HL	0101 0111 1000 0000	AC,@HL	← BCD(AC)	CF
DAS*#	@HL	0101 0111 1100 0000	AC,@HL HL	← BCD(AC) ←HL+1	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	AC,Rx	← D	
LDH	Rx,@HL	0110 0000 0XXX XXXX	AC,Rx	← H(T@HL)	
LDH*	Rx,@HL	0110 0001 0XXX XXXX	AC,Rx HL	← H(T@HL) ← HL + 1	
LDL	Rx,@HL	0110 0010 0XXX XXXX	AC,Rx	← L(T@HL)	
LDL*	Rx,@HL	0110 0011 0XXX XXXX	AC,Rx HL	← L(T@HL) ← HL + 1	
MRF1	Rx	0110 0100 0XXX XXXX	AC,Rx	← RFC3-0	
MRF2	Rx	0110 0101 0XXX XXXX	AC,Rx	← RFC7-4	
MRF3	Rx	0110 0110 0XXX XXXX	AC,Rx	← RFC11-8	
MRF4	Rx	0110 0111 0XXX XXXX	AC,Rx	← RFC15-12	
STA	Rx	0110 1000 0XXX XXXX	Rx	← AC	
STA	@HL	0110 1000 1000 0000	@HL	← AC	
STA#	@HL	0110 1000 1100 0000	@HL HL	← AC ←HL+1	
LDA	Rx	0110 1100 0XXX XXXX	AC	← Rx	
LDA	@HL	0110 1100 1000 0000	AC	← @HL	
LDA#	@HL	0110 1100 1100 0000	AC HL	← @HL ←HL+1	
MRA	Rx	0110 1101 0XXX XXXX	CF	← Rx3	
MRW	@HL,Rx	0110 1110 0XXX XXXX	AC,@HL	← Rx	
MRW#	@HL,Rx	0110 1110 1XXX XXXX	AC,@HL HL	← Rx ←HL+1	
MWR	Rx,@HL	0110 1111 0XXX XXXX	AC,Rx	← @HL	
MWR#	Rx,@HL	0110 1111 1XXX XXXX	AC,Rx HL	← @HL ←HL+1	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	AC,Ry	← Rx	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	AC,Rx	← Ry	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 PXXX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 PXXX XXXX XXXX	PC	← X	
TMS	Rx	1110 0000 0XXX XXXX	Timer1 AC3,2 = 11 AC3,2 = 10 AC3,2 = 01 AC3,2 = 00 AC1,0,PB3~0	← Rx & AC : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMS	@HL	1110 0001 0000 0000	Timer1	← T@HL	

Instruction		Machine Code	Function		Flag/Remark
			TD7,6 = 11 TD7,6 = 10 TD7,6 = 01 TD7,6 = 00 TD5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMSX	X	1110 001X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100X8 ,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2	Rx	1110 0100 0XXX XXXX	Timer2 AC3,2 = 11 AC3,2 = 10 AC3,2 = 01 AC3,2 = 00 AC1,0,PB3~0	← Rx & AC : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2	@HL	1110 0101 0000 0000	Timer2 TD7,6 = 11 TD7,6 = 10 TD7,6 = 01 TD7,6 = 00 TD5~0	← T@HL : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0XXX XXX0	X6 X5 X4 X3 X2 X1	: Enable HEF6 : Enable HEF5 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	RFC KEY_S TMR2 PDV INT TMR1
SIE*	X	1110 1001 0XXX XXXX	X6 X5 X4 X3 X2 X1 X0	: Enable IEF6 : Enable IEF5 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	RFC KEY_S TMR2 PDV INT TMR1 C, DPT
PLC	X	1110 101X 0XXX XXXX	X8 X6-0	: Reset PH15~11 : Reset HRF6-0	
SRF	X	1110 1100 00XX XXXX	X5 X4 X3 X2 X1	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RH Output : Enable RT Output	 ENX EHM ETP

Instruction		Machine Code	Function		Flag/Remark
			X0	: Enable RR Output	ERR
SRE	X	1110 1101 X0XX X000	X7 X5 X4 X3	: Enable SRF7(key_s) : Enable SRF5(INT) : Enable SRF4(C port) : Enable SRF3(D port)	
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1110 1000 0000	SCLK	: Low Speed Clock	
CPHL	X	1110 1111 XXXX XXXX	(PC+1)	← force "NOP" if X7~0=IDBF7~0	
SPK	Rx	1111 0000 0XXX XXXX	KO1~16	← Rx & AC	
SPK	@HL	1111 0001 0000 0000	KO1~16	← T @HL	
SPKX	X	1111 0010 XXXX XXXX	X6=1 X6=0 X7,5,4=000 X7,5,4=001 X7,5,4=010 X7,5,4=10X X7,5,4=110 X7,5,4=111	: KEY_S is released by scanning cycle : KEY_S is released by normal key scanning : Set one of KO1~16 =1 by X3~0 : Set all = 1 : Set all Hi-z : Set eight of KO1~16 =1 by X3 X3=0 => KO1~8 X3=1 => KO9~16 : Set four of KO1~16 =1 by X3,2 X3,2=00 => KO1~4 X3,2=01 => KO5~8 X3,2=10 => KO9~12 X3,2=11 => KO13~16 : Set two of KO1~16 =1 by X3,2,1 X3~1=000=>KO1,2 X3~1=001=>KO3,4 X3~1=010=>KO5,6 X3~1=011=>KO7,8 X3~1=100=>KO9,10 X3~1=101=>KO11,12 X3~1=110=>KO13,14 X3~1=111=>KO15,16	
RTS		1111 0100 0000 0000	PC	← STACK (CALL Return)	
SCC	X	1111 0100 1X0X XXXX	X6 = 1 X6 = 0 X4 = 1 X3 = 1 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 : Set P(C) Cch : Set P(D) Cch : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1111 0101 000X X000	X4 X3	: Enable SEF4(C1-4) : Enable SEF3(D1-4)	
SPA	X	1111 0101 100X XXXX	X4 X3~0	: Set A4-1 Pull-Low : Set A4-1 I/O	1:Pull low 1:Output, 0: Input
SPB	X	1111 0101 101X XXXX	X4	: Set B4-1 Pull-Low	1:Pull low

Instruction		Machine Code	Function		Flag/Remark
			X3~0	: Set B4-1 I/O	1:Output, 0: Input
SPC	X	1111 0101 110X XXXX	X4 X3-0	: Set C4-1 Pull-Low / Low-Level-Hold : Set C4-1 I/O	1:Pull low, 0:LLH 1:Output, 0: Input
SPD	X	1111 0101 111X XXXX	X4 X3-0	: Set D4-1 Pull-Low : Set D4-1 I/O	1:Pull low 1:Output, 0: Input
SF	X	1111 0110 X00X 00XX	X7 X4 X1 X0	: Reload 1 Set : WDT Enable : BCF Set : CF Set	
RF	X	1111 0111 X00X 00XX	X7 X4 X1 X0	:Reload 1 Reset : WDT Reset : BCF Reset : CF Reset	
ALM	X	1111 110X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
SF2	X	1111 1110 0000 XXXX	X3 X2 X1 X0	: Enable INT powerful Pull-low : Close all Segments : Dis-ENX Set : Reload 2 Set	
RF2	X	1111 1110 1000 XXXX	X3 X2 X1 X0	: Disable INT powerful Pull-low : Release Segments : Dis-ENX Reset : Reload 2 Reset	
HALT		1111 1111 0000 0000	Halt Operation		
STOP		1111 1111 1000 0000	Stop Operation		

Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	D	Immediate Data
AC	Accumulator	(D)B	Complement of Immediate Data
(AC)n	Content of Accumulator (bit n)	PC	Program Counter
(AC)B	Complement of content of Accumulator	CF	Carry Flag
X	Address of program or control data	ZERO	Zero Flag
Rx	Address X of data RAM	WDF	Watch-Dog Timer Enable Flag
(Rx)n	Bit n content of Rx	7SEG	7 segment decoder for LCD
Ry	Address Y of working register	BCLK	System clock for instruction
R@HL	Address of data RAM specified by @HL	IEFn	Interrupt Enable Flag
BCF	Backup flag	HRFn	HALT Release Flag
@HL	Generic Index address register	HEFn	HALT Release Enable Flag
(@HL)	Content of generic Index address register	Lz	Address of LCD PLA Latch
(@L)	Content of lowest nibble Index register	SRFn	STOP Release Enable Flag
(@H)	Content of middle nibble Index register	SCFn	Start Condition Flag
(@U)	Content of highest nibble Index register	Cch	Clock Source of Chattering prevention ckt.
T@HL	Address of Table ROM	Cfq	Clock Source of Frequency Generator
H(T@HL)	High Nibble content of Table ROM	SEFn	Switch Enable Flag
L(T@HL)	Low Nibble content of Table ROM	FREQ	Frequency Generator setting Value
TMR	Timer Overflow Release Flag	CSF	Clock Source Flag
Ctm	Clock Source of Timer	P	Program Page
PDV	Pre-Divider	RFOVF	RFC Overflow Flag
STACK	Content of stack	RFC	Resistor to Frequency counter
TM1	Timer 1	(RFC)n	Bit data of Resistor to Frequency counter
TM2	Timer 2		