十速科技股份有限公司
tenx technology inc.

Advance Information

TM8530

4-Bit Microcontroller

Data Sheet

Tenx reserves the right to change or discontinue this product without notice.

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CONTENTS

GENERAL DESCRIPTION

TM8530 is an embedded high-performance 4-bit micro controller with LCD driver.

FEATURES

1. Powerful instruction set (174 instructions)
- Binary addition, subtraction, BCD adjusts, logical operation in direct and index addressing mode
- Single-bit manipulation (set, reset, decision for branch)
- Various conditional branches
- 16 working registers and manipulation
- LCD driver data transfer

2. ROM capacity 3K x 16 bits
- Program ROM Max. capacity 3K x 16 bits
- Table ROM Max. capacity 2K x 8 bits

3. RAM capacity
- Data RAM 128 x 4 bits

4. Input/output ports
- Port IOA 4 pins (with internal pull-low)
- Port IOB 2 pins (with internal pull-low)
- Port IOC 4 pins (with internal pull-low, chattering prevention clock)
- Port IOD 4 pins (with internal pull-low, chattering prevention clock)

5. 8 level subroutine nesting

6. Interrupt function
- External factor 3 (INT pin, Port IOC, IOD)
- Internal factor 4 (Pre-Divider, Timer1, Timer2, RFC)

7. Built in Alarm, Frequency or Melody generator.

8. BZB, BZ [Mux*(Multiplex System)* with IOB3, IOB4]

9. Two 6-bit programmable timers with programmable clock source

10. LCD driver output
- 36 LCD driver outputs (up to 144 LCD segment drivable)
- 1/4 Duty for LCD
- 1/2 Bias or 1/3Bias for LCD selected by mask option
- Single instruction to turn off all segments
- 18 LCD address

11. Built-in LCD Voltage divider Resistor.

12. Dual clock operation, X'tal type slow oscillation, and fast oscillation can set as internal RC (500 KHz) or external R by switch mask option.

13. Watch dog timer

14. HALT function

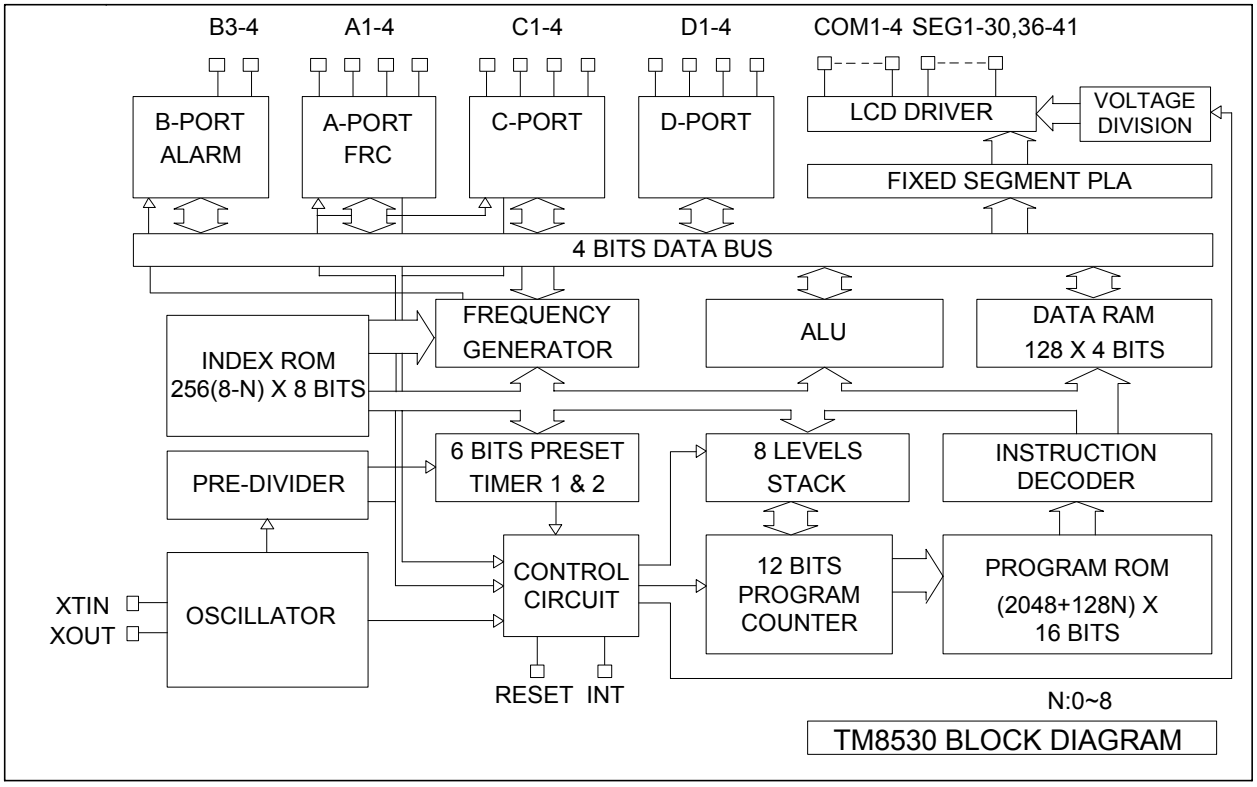
15. STOP function

16. Fixed LCD PLA configuration

APPLICATION

- Timer / Calendar / Calculator

Functional Block Diagram



PIN ASSIGNMENT

No	Name	No	Name
1	SEG36/IOD1	27	SEG10
2	SEG37/IOD2	28	SEG11
3	SEG38/IOD3	29	SEG12
4	SEG39/IOD4	30	SEG13
5	SEG40	31	SEG14
6	SEG41	32	SEG15
7	RESET	33	SEG16
8	INT	34	SEG17
9	XIN	35	SEG18
10	XOUT	36	SEG19
11	GND	37	SEG20
12	VDD	38	SEG21
13	TEST	39	SEG22
14	COM1	40	SEG23
15	COM2	41	SEG24/IOA1/CX
16	COM3	42	SEG25/IOA2/RR
17	COM4	43	SEG26/IOA3/RT
18	SEG1	44	SEG27/IOA4/RH
19	SEG2	45	SEG28
20	SEG3	46	SEG29
21	SEG4	47	SEG30/IOB3/BZB
22	SEG5	48	IOB4/BZ
23	SEG6	49	IOC1
24	SEG7	50	IOC2
25	SEG8	51	IOC3
26	SEG9	52	IOC4

PIN DESCRIPTION

Name	I/O	Description
VDD	P	LCD supply voltage, and positive supply voltage. Connect +3.0V battery positive pin to VDD.
RESET	I	Input pin from LSI reset request signal, with internal pull-down resistor.
INT	I I/O	Input pin for external INT request signal. Falling edge or rising edge triggered by mask option. Internal pull-down or pull-up resistor is selected by mask option. Serial Data for Serial Program/Read Mode.
TEST	I	Test signal input pin.
XIN XOUT	I O	32KHz Crystal oscillator for Slow Clock. External R oscillation for Fast Clock.
COM1~4	O	Output pins for driving the common pins of the LCD panel.
SEG1~30, 36~41	O	Output pins for driving the LCD panel segment.
IOA1-4	I/O	Input / Output port-A, can use software to define internal pull-low Resistor. This port is multiplexed with SEG24~27, and set by mask option.
IOB3-4	I/O	Input / Output port-B, can use software to define internal pull-low Resistor. This port is multiplexed with BZB, BZ, and set by mask option.
IOC1-4	I/O	Input / Output port-C, can use software to define internal pull-low and chattering clock to reduce input bounce.
IOD1-4	I/O	Input / Output port-D, can use software to define internal pull-low Resistor, and Chattering clock to reduce input bounce. This port is multiplexed with SEG36~39, and set by mask option.
(RFC)CX RR/RT/RH	I O	1 input pin and 3 output pins for RFC application. This port is muxed with SEG24~27 / IOA1~4, and set by mask option.
(ALM) BZB/BZ	O	Output port for alarm, frequency or melody generator. This port is multiplexed with IOB3, 4, and set by mask option.
GND	P	Negative supply voltage.

Fixed PLA Table

SEGn	Lz	COM1	COM2	COM3	COM4
SEG1	00H	DBUSA	DBUSB	DBUSC	DBUSD
SEG2		DBUSE	DBUSF	DBUSG	DBUSH
SEG3	01H	DBUSA	DBUSB	DBUSC	DBUSD
SEG4		DBUSE	DBUSF	DBUSG	DBUSH
SEG5	02H	DBUSA	DBUSB	DBUSC	DBUSD
SEG6		DBUSE	DBUSF	DBUSG	DBUSH
SEG7	03H	DBUSA	DBUSB	DBUSC	DBUSD
SEG8		DBUSE	DBUSF	DBUSG	DBUSH
SEG9	04H	DBUSA	DBUSB	DBUSC	DBUSD
SEG10		DBUSE	DBUSF	DBUSG	DBUSH
SEG11	05H	DBUSA	DBUSB	DBUSC	DBUSD
SEG12		DBUSE	DBUSF	DBUSG	DBUSH
SEG13	06H	DBUSA	DBUSB	DBUSC	DBUSD
SEG14		DBUSE	DBUSF	DBUSG	DBUSH
SEG15	07H	DBUSA	DBUSB	DBUSC	DBUSD
SEG16		DBUSE	DBUSF	DBUSG	DBUSH
SEG17	08H	DBUSA	DBUSB	DBUSC	DBUSD
SEG18		DBUSE	DBUSF	DBUSG	DBUSH
SEG19	09H	DBUSA	DBUSB	DBUSC	DBUSD
SEG20		DBUSE	DBUSF	DBUSG	DBUSH
SEG21	0AH	DBUSA	DBUSB	DBUSC	DBUSD
SEG22		DBUSE	DBUSF	DBUSG	DBUSH
SEG23	0BH	DBUSA	DBUSB	DBUSC	DBUSD
SEG24		DBUSE	DBUSF	DBUSG	DBUSH
SEG25	0CH	DBUSA	DBUSB	DBUSC	DBUSD
SEG26		DBUSE	DBUSF	DBUSG	DBUSH
SEG27	0DH	DBUSA	DBUSB	DBUSC	DBUSD
SEG28		DBUSE	DBUSF	DBUSG	DBUSH
SEG29	0EH	DBUSA	DBUSB	DBUSC	DBUSD
SEG30		DBUSE	DBUSF	DBUSG	DBUSH
SEG36	0FH	DBUSA	DBUSB	DBUSC	DBUSD
SEG37		DBUSE	DBUSF	DBUSG	DBUSH
SEG38	10H	DBUSA	DBUSB	DBUSC	DBUSD
SEG39		DBUSE	DBUSF	DBUSG	DBUSH
SEG40	11H	DBUSA	DBUSB	DBUSC	DBUSD
SEG41		DBUSE	DBUSF	DBUSG	DBUSH

Electrical Characteristics

ABSOLOUTE MAXIMUM RATINGS (GND= 0V)

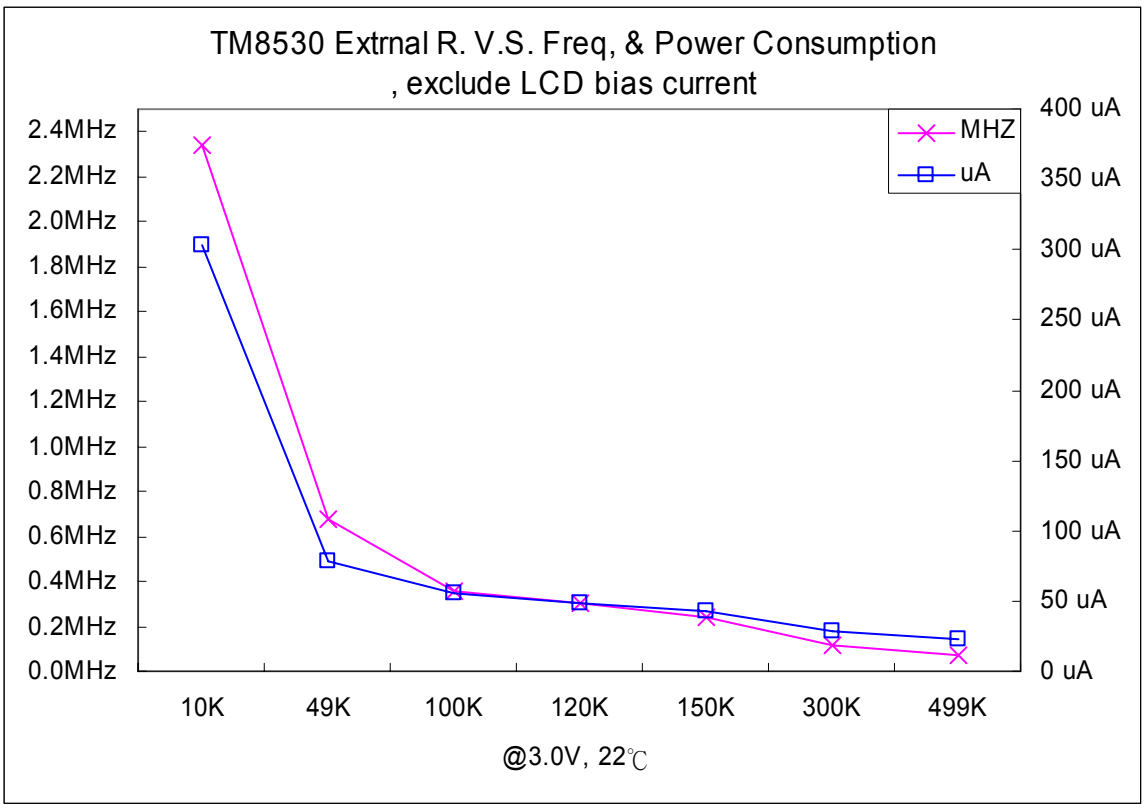
Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to 3.6	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	
Maximum output Voltage	Vout	-0.3 to VDD+0.3	
Maximum Operating Temperature	Topg	-40 to +80	℃
Maximum Storage Temperature	Tstg	-40 to +125	

POWER CONSUMPTION (@ VDD= 3.0V, Ta= 25℃ , GND= 0V)

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
Normal Mode	I_{32K}	32.768KHz Crystal mode, BCF=0, PH0=BCLK **without loading and LCD bias current**		4.5		uA
HALT mode	I_{HALT}			3.5	6	
STOP mode	I_{STOP}				1	
External R	$I_{Ext.\ R}$	R=150KΩ oscillator operating, BCF=0, PH0=BCLK **without loading and LCD bias current**	42.5			
Pure LCD bias (LCD voltage divider resistor)Current	I_{LCD1}	LCD Low bias (Low Driving)		6		
	I_{LCD2}	LCD Normal bias (Normal Driving)		12		
	I_{LCD3}	LCD High bias (High Driving)		24		
	I_{LCD4}	LCD Higher bias (Higher Driving)		60		

Note: **1.** *When External R oscillator mode is operating, the current consumption will depend on the frequency of oscillation.*

2. *Normal Mode & Low Driving : $I_{32K} + I_{LCD1} = (4.5+6)\_uA$ ..(Typ.)*



ALLOWABLE OPERATING CONDITIONS (Ta= 25℃, GND= 0V)

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD		2.0	3.6	V
Oscillator Start-Up Voltage	VDD_{stup}	32.768KHz Crystal Mode	1.4		
Oscillator Sustain Voltage	VDD_{sut}		1.3		
Input "H" Voltage	Vih1		VDD-0.7	VDD+0.7	
Input "L" Voltage	Vil1		-0.7	0.7	
Operating Freq	Fopg1	32.768KHz Crystal Mode	32		KHZ
	Fopg2	External R mode	10	1000	

DC Output Characteristics (@ VDD= 2.0V, Ta= 25℃ , GND= 0V)

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh	Ioh=-1mA	IOA,B,C,D	1.5			V
Output "L" Voltage	Vol	Iol=2mA				0.9	V

ELECTRICAL CHARACTERISTICS

Input Resistance (VDD=3.0V)

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
IOA,B,C Pull-Down Tr	Rmad1	Vi=VDD	200	500	1000	KΩ
INT Pull-Down Tr	Rintu1	Vi=VDD	200	500	1000	
INT Pull-up Tr	Rintd1	Vi=GND	200	500	1000	
RES Pull-Down R	Rres1	Vi=GND or VDD	9	35	90	

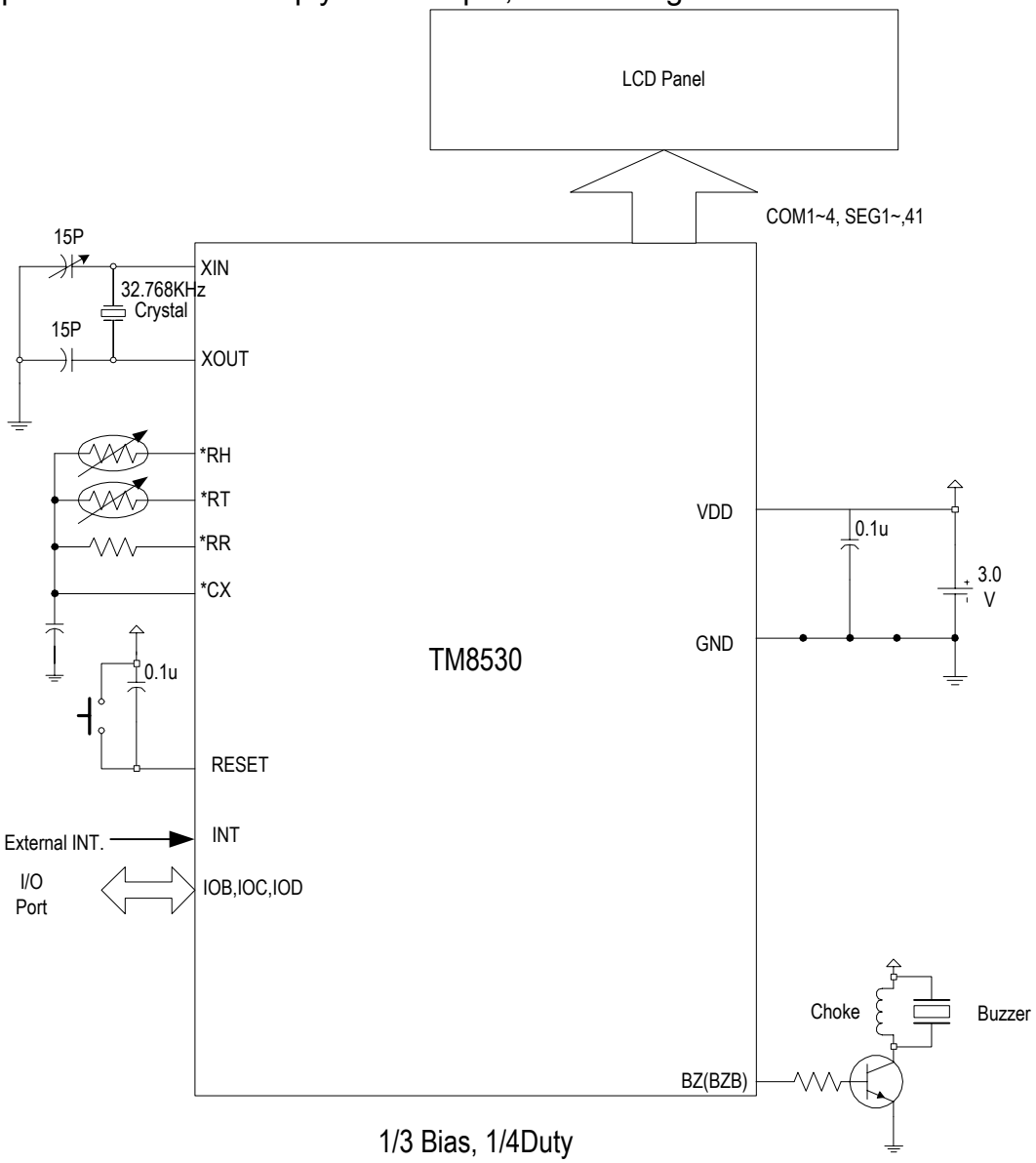
Segment Driver Output Characteristics

(@ VDD= 2.0V, Ta= 25℃ , GND= 0V)

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output "H" Voltage	Vohf	Ioh=-1uA	SEG-n		VDD		V
Output "L" Voltage	Volf	Iol=1uA			0		
Output "H" Voltage	Vohg	Ioh=-10uA	COM-n		VDD		
Output "M" Voltage	Vomg	Iol/h=+/-10uA			0.5 *VDD		
Output "L" Voltage	Volg	Iol=10uA			0		
1/3 Bias display Mode							
Output "H" Voltage	Vohi	Ioh=-1uA	SEG-n		VDD		V
Output "M1" Voltage	Vom1i	Iol/h=+/-10uA			1/3 *VDD		
Output "M2" Voltage	Vom2i	Iol/h=+/-10uA			2/3 *VDD		
Output "L" Voltage	Voli	Iol=1uA			0		
Output "H" Voltage	Vohj	Ioh=-10uA	COM-n		VDD		
Output "M1" Voltage	Vom1j	Iol/h=+/-10uA			1/3 *VDD		
Output "M2" Voltage	Vom2j	Iol/h=+/-10uA			2/3 *VDD		
Output "L" Voltage	Volj	Iol=10uA			0		

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



1/3 Bias, 1/4Duty

INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 001Z ZZZZ YYYY	Lz	← (7SEG ← Ry)	(Ry=70H~7FH)
LCB	Lz,Ry	0000 010Z ZZZZ YYYY	Lz	← (7SEG ← Ry) Blank Zero	(Ry=70H~7FH)
LCP	Lz,Ry	0000 011Z ZZZZ YYYY	Lz	← Ry & AC	(Ry=70H~7FH)
LCD	Lz,@HL	0000 100Z ZZZZ 0000	Lz	← T@HL	
LCT	Lz,@HL	0000 100Z ZZZZ 0001	Lz	← (7SEG ← @HL)	
LCB	Lz,@HL	0000 100Z ZZZZ 0010	Lz	← (7SEG ← @HL) Blank Zero	
LCP	Lz,@HL	0000 100Z ZZZZ 0011	Lz	← @HL & AC	
LCDX	D	0000 100D D000 0100	Multi-Lz D=00 D=01	← T@HL : Multi-Lz=00H~0FH : Multi-Lz=10H~1FH	D: 0~1
LCTX	D	0000 100D D000 0101	Multi-Lz	← (7SEG ← @HL)	D: 0~1
LCBX	D	0000 100D D000 0110	Multi-Lz	← (7SEG ← @HL) Blank Zero	D: 0~1
LCPX	D	0000 100D D000 0111	Multi-Lz	← @HL & AC	D: 0~1
OPA	Rx	0000 1010 0XXX XXXX	Port(A)	← Rx	
OPAS	Rx,D	0000 1011 DXXX XXXX	A1,2,3,4	← Rx0,Rx1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port(B)	← Rx	
OPC	Rx	0000 1101 0XXX XXXX	Port(C)	← Rx	
OPD	Rx	0000 1110 0XXX XXXX	Port(D)	← Rx	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQ	D,@HL	0001 01DD 0000 0000	FREQ	←T@HL	
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
MVL	Rx	0001 1100 0XXX XXXX	IDBF0~3	← Rx	
MVH	Rx	0001 1101 0XXX XXXX	IDBF4~7	← Rx	
MVU	Rx	0001 1110 0XXX XXXX	IDBF8~11	← Rx	
ADC	Rx	0010 0000 0XXX XXXX	AC	← Rx + AC + CF	CF
ADC	@HL	0010 0000 1000 0000	AC	← @HL + AC + CF	CF
ADC#	@HL	0010 0000 1100 0000	AC HL	← @HL + AC + CF ←HL+1	CF
ADC*	Rx	0010 0001 0XXX XXXX	AC,Rx	← Rx + AC + CF	CF
ADC*	@HL	0010 0001 1000 0000	AC,@HL	← @HL + AC + CF	CF
ADC*#	@HL	0010 0001 1100 0000	AC,@HL HL	← @HL + AC + CF ←HL+1	CF
SBC	Rx	0010 0010 0XXX XXXX	AC	← Rx + ACB + CF	CF
SBC	@HL	0010 0010 1000 0000	AC	← @HL + ACB + CF	CF
SBC#	@HL	0010 0010 1100 0000	AC	← @HL + ACB + CF	CF

Instruction		Machine Code	Function		Flag/Remark
			HL	←HL+1	
SBC*	Rx	0010 0011 0XXX XXXX	AC,Rx	← Rx + ACB + CF	CF
SBC*	@HL	0010 0011 1000 0000	AC,@HL	← @HL + ACB + CF	CF
SBC*#	@HL	0010 0011 1100 0000	AC,@HL HL	← @HL + ACB + CF ←HL+1	CF
ADD	Rx	0010 0100 0XXX XXXX	AC	← Rx + AC	CF
ADD	@HL	0010 0100 1000 0000	AC	← @HL + AC	CF
ADD#	@HL	0010 0100 1100 0000	AC HL	← @HL + AC ←HL+1	CF
ADD*	Rx	0010 0101 0XXX XXXX	AC,Rx	← Rx + AC	CF
ADD*	@HL	0010 0101 1000 0000	AC,@HL	← @HL + AC	CF
ADD*#	@HL	0010 0101 1100 0000	AC,@HL HL	← @HL + AC ←HL+1	CF
SUB	Rx	0010 0110 0XXX XXXX	AC	← Rx + ACB + 1	CF
SUB	@HL	0010 0110 1000 0000	AC	← @HL + ACB + 1	CF
SUB#	@HL	0010 0110 1100 0000	AC HL	← @HL + ACB + 1 ←HL+1	CF
SUB*	Rx	0010 0111 0XXX XXXX	AC,Rx	← Rx + ACB + 1	CF
SUB*	@HL	0010 0111 1000 0000	AC,@HL	← @HL + ACB + 1	CF
SUB*#	@HL	0010 0111 1100 0000	AC,@HL HL	← @HL + ACB + 1 ←HL+1	CF
ADN	Rx	0010 1000 0XXX XXXX	AC	← Rx + AC	
ADN	@HL	0010 1000 1000 0000	AC	← @HL + AC	
ADN#	@HL	0010 1000 1100 0000	AC HL	← @HL + AC ←HL+1	
ADN*	Rx	0010 1001 0XXX XXXX	AC,Rx	← Rx + AC	
ADN*	@HL	0010 1001 1000 0000	AC,@HL	← @HL + AC	
ADN*#	@HL	0010 1001 1100 0000	AC,@HL HL	← @HL + AC ←HL+1	
AND	Rx	0010 1010 0XXX XXXX	AC	← Rx AND AC	
AND	@HL	0010 1010 1000 0000	AC	← @HL AND AC	
AND#	@HL	0010 1010 1100 0000	AC HL	← @HL AND AC ←HL+1	
AND*	Rx	0010 1011 0XXX XXXX	AC,Rx	← Rx AND AC	
AND*	@HL	0010 1011 1000 0000	AC,@HL	← @HL AND AC	
AND*#	@HL	0010 1011 1100 0000	AC,@HL HL	← @HL AND AC ←HL+1	
EOR	Rx	0010 1100 0XXX XXXX	AC	← Rx EOR AC	
EOR	@HL	0010 1100 1000 0000	AC	← @HL EOR AC	
EOR#	@HL	0010 1100 1100 0000	AC HL	← @HL EOR AC ←HL+1	
EOR*	Rx	0010 1101 0XXX XXXX	AC,Rx	← Rx EOR AC	
EOR*	@HL	0010 1101 1000 0000	AC,@HL	← @HL EOR AC	
EOR*#	@HL	0010 1101 1100 0000	AC,@HL HL	← @HL EOR AC ←HL+1	

Instruction		Machine Code	Function		Flag/Remark
OR	Rx	0010 1110 0XXX XXXX	AC	← Rx OR AC	
OR	@HL	0010 1110 1000 0000	AC	← @HL OR AC	
OR#	@HL	0010 1110 1100 0000	AC HL	← @HL OR AC ←HL+1	
OR*	Rx	0010 1111 0XXX XXXX	AC,Rx	← Rx OR AC	
OR*	@HL	0010 1111 1000 0000	AC,@HL	← @HL OR AC	
OR*#	@HL	0010 1111 1100 0000	AC,@HL HL	← @HL OR AC ←HL+1	
ADCI	Ry,D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC,Ry	← Ry + D + CF	
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC,Ry	← Ry + DB + CF	
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	← Ry + D	
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC,Ry	← Ry + D	
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC,Ry	← Ry + DB + 1	
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC,Ry	← Ry + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC,Ry	← Ry AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC,Ry	← Ry EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC,Ry	← Ry OR D	
INC*	Rx	0100 0000 0XXX XXXX	AC,Rx	← Rx + 1	CF
INC*	@HL	0100 0000 1000 0000	AC,@HL	← @HL + 1	CF
INC*#	@HL	0100 0000 1100 0000	AC,@HL HL	← @HL + 1 ←HL+1	CF
DEC*	Rx	0100 0001 0XXX XXXX	AC,Rx	← Rx – 1	CF
DEC*	@HL	0100 0001 1000 0000	AC,@HL	← @HL - 1	CF
DEC*#	@HL	0100 0001 1100 0000	AC,@HL HL	← @HL - 1 ←HL+1	CF
IPA	Rx	0100 0010 0XXX XXXX	AC,Rx	← Port(A)	
IPB	Rx	0100 0100 0XXX XXXX	AC,Rx	← Port(B)	
IPC	Rx	0100 0111 0XXX XXXX	AC,Rx	← Port(C)	
IPD	Rx	0100 1000 0XXX XXXX	AC,Rx	← Port(D)	
MAF	Rx	0100 1010 0XXX XXXX	AC,Rx	← STS1	B3 : CF B2 : ZERO B1 : (No use) B0 : (No use)
MSB	Rx	0100 1011 0XXX XXXX	AC,Rx	← STS2	B3 : SCF3(DPT) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF

MSC	Rx	0100 1100 0XXX XXXX	AC,Rx	← STS3	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT)
MCX	Rx	0100 1101 0XXX XXXX	AC,Rx	← STS3X	B3 : SCF9(RFC) B2 : (unused) B1 : SCF6(TM2)
MSD	Rx	0100 1110 0XXX XXXX	AC,Rx	← STS4	B3 : (No use) B2 : FROVF B1 : WDF B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD(AC)	CF
DAA*	Rx	0101 0101 0XXX XXXX	AC,Rx	← BCD(AC)	CF
DAA*	@HL	0101 0101 1000 0000	AC,@HL	← BCD(AC)	CF
DAA*#	@HL	0101 0101 1100 0000	AC,@HL HL	← BCD(AC) ←HL+1	CF
DAS		0101 0110 0000 0000	AC	← BCD(AC)	CF
DAS*	Rx	0101 0111 0XXX XXXX	AC,Rx	← BCD(AC)	CF
DAS*	@HL	0101 0111 1000 0000	AC,@HL	← BCD(AC)	CF
DAS*#	@HL	0101 0111 1100 0000	AC,@HL HL	← BCD(AC) ←HL+1	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	AC,Rx	← D	
LDH	Rx,@HL	0110 0000 0XXX XXXX	AC,Rx	← H(T@HL)	
LDH*	Rx,@HL	0110 0001 0XXX XXXX	AC,Rx HL	← H(T@HL) ← HL + 1	
LDL	Rx,@HL	0110 0010 0XXX XXXX	AC,Rx	← L(T@HL)	
LDL*	Rx,@HL	0110 0011 0XXX XXXX	AC,Rx HL	← L(T@HL) ← HL + 1	
MRF1	Rx	0110 0100 0XXX XXXX	AC,Rx	← RFC3-0	
MRF2	Rx	0110 0101 0XXX XXXX	AC,Rx	← RFC7-4	
MRF3	Rx	0110 0110 0XXX XXXX	AC,Rx	← RFC11-8	
MRF4	Rx	0110 0111 0XXX XXXX	AC,Rx	← RFC15-12	
STA	Rx	0110 1000 0XXX XXXX	Rx	← AC	
STA	@HL	0110 1000 1000 0000	@HL	← AC	
STA#	@HL	0110 1000 1100 0000	@HL HL	← AC ←HL+1	
LDA	Rx	0110 1100 0XXX XXXX	AC	← Rx	

LDA	@HL	0110 1100 1000 0000	AC	← @HL	
LDA#	@HL	0110 1100 1100 0000	AC HL	← @HL ←HL+1	
MRA	Rx	0110 1101 0XXX XXXX	CF	← Rx3	
MRW	@HL,Rx	0110 1110 0XXX XXXX	AC,@HL	← Rx	
MRW#	@HL,Rx	0110 1110 1XXX XXXX	AC,@HL HL	← Rx ←HL+1	
MWR	Rx,@HL	0110 1111 0XXX XXXX	AC,Rx	← @HL	
MWR#	Rx,@HL	0110 1111 1XXX XXXX	AC,Rx HL	← @HL ←HL+1	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	AC,Ry	← Rx	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	AC,Rx	← Ry	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 PXXX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 PXXX XXXX XXXX	PC	← X	
TMS	Rx	1110 0000 0XXX XXXX	AC3,2 = 11 AC3,2 = 10 AC3,2 = 01 AC3,2 = 00 AC1,0,PB3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMS	@HL	1110 0001 0000 0000	TD7,6 = 11 TD7,6 = 10 TD7,6 = 01 TD7,6 = 00 TD5~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMSX	X	1110 001X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2	Rx	1110 0100 0XXX XXXX	Timer2	← Rx & AC	
TM2	@HL	1110 0101 0000 0000	Timer2	← T@HL	

TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0X0X XXX0	X6 X4 X3 X2 X1	: Enable HEF6 : Enable HEF4 : Enable HEF3 : Enable HEF2 : Enable HEF1	RFC TMR2 PDV INT TMR1
SIE*	X	1110 1001 0X0X XXXX	X6 X4 X3 X2 X1 X0	: Enable IEF6 : Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	RFC TMR2 PDV INT TMR1 C, DPT
PLC	X	1110 101X 0XXX XXXX	X8 X6-0	: Reset PH15~11 : Reset HRF6~0	
SRF	X	1110 1100 00XX XXXX	X5 X4 X3 X2 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RH Output : Enable RT Output : Enable RR Output	 ENX EHM ETP ERR
SRE	X	1110 1101 00XX X000	X5 X4 X3	: Enable SRF5(INT) : Enable SRF4(C port) : Enable SRF3(D port)	
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1110 1000 0000	SCLK	: Low Speed Clock	
CPHL	X	1110 1111 XXXX XXXX	(PC+1)	← force “NOP” if X7~0=IDBF7~0	
RTS		1111 0100 0000 0000	PC	← STACK (CALL Return)	
SCC	X	1111 0100 1X0X XXXX	X6 = 1 X6 = 0 X4 = 1 X3 = 1 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 : Set P(C) Cch : Set P(D) Cch : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1111 0101 000X X000	X4	: Enable SEF4(C1-4)	

			X3	: Enable SEF3(D1-4)	
SPA	X	1111 0101 100X XXXX	X4 X3~0	: Set A4-1 Pull-Low : Set A4-1 I/O	1:Pull low 1:Output, 0: Input
SPB	X	1111 0101 101X XX00	X4 X3~2	: Set B4-1 Pull-Low : Set B4-3 I/O	1:Pull low 1:Output, 0: Input
SPC	X	1111 0101 110X XXXX	X4 X3-0	: Set C4-1 Pull-Low : Set C4-1 I/O	1:Pull low, 1:Output, 0: Input
SPD	X	1111 0101 111X XXXX	X4 X3-0	: Set D4-1 Pull-Low : Set D4-1 I/O	1:Pull low 1:Output, 0: Input
SF	X	1111 0110 X00X 00XX	X7 X4 X1 X0	: Reload 1 Set : WDT Enable : BCF Set : CF Set	
RF	X	1111 0111 X00X 00XX	X7 X4 X1 X0	:Reload 1 Reset : WDT Reset : BCF Reset : CF Reset	
ALM	X	1111 110X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
SF2	X	1111 1110 0000 XXXX	X3 X2 X1 X0	: Enable INT powerful Pull-low : Close all Segments : Dis-ENX Set : Reload 2 Set	
RF2	X	1111 1110 1000 XXXX	X3 X2 X1 X0	: Disable INT powerful Pull-low : Release Segments : Dis-ENX Reset : Reload 2 Reset	
HALT		1111 1111 0000 0000	Halt Operation		
STOP		1111 1111 1000 0000	Stop Operation		

Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	D	Immediate Data
AC	Accumulator	(D)B	Complement of Immediate Data
(AC)n	Content of Accumulator (bit n)	PC	Program Counter
(AC)B	Complement of content of Accumulator	CF	Carry Flag
X	Address of program or control data	ZERO	Zero Flag
Rx	Address X of data RAM	WDF	Watch-Dog Timer Enable Flag
(Rx)n	Bit n content of Rx	7SEG	7 segment decoder for LCD
Ry	Address Y of working register	BCLK	System clock for instruction
R@HL	Address of data RAM specified by @HL	IEFn	Interrupt Enable Flag
BCF	Backup flag	HRFn	HALT Release Flag
@HL	Generic Index address register	HEFn	HALT Release Enable Flag
(@HL)	Content of generic Index address register	Lz	Address of LCD PLA Latch
(@L)	Content of lowest nibble Index register	SRFn	STOP Release Enable Flag
(@H)	Content of middle nibble Index register	SCFn	Start Condition Flag
(@U)	Content of highest nibble Index register	Cch	Clock Source of Chattering prevention ckt.
T@HL	Address of Table ROM	Cfq	Clock Source of Frequency Generator
H(T@HL)	High Nibble content of Table ROM	SEFn	Switch Enable Flag
L(T@HL)	Low Nibble content of Table ROM	FREQ	Frequency Generator setting Value
TMR	Timer Overflow Release Flag	CSF	Clock Source Flag
Ctm	Clock Source of Timer	P	Program Page
PDV	Pre-Divider	RFOVF	RFC Overflow Flag
STACK	Content of stack	RFC	Resistor to Frequency counter
TM1	Timer 1	(RFC)n	Bit data of Resistor to Frequency counter
TM2	Timer 2		