



十速科技股份有限公司
tenx technology inc.

**Advance
Information**

TMU3114MS

USB Full Speed Controller

Data Sheet

**Tenx reserves the right to change or
discontinue this product without notice.**

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Preliminary

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1. GENERAL DESCRIPTION

The TMU3114MS is an 8051-based embedded device tailored to general USB full speed application. TMU3114MS is designed for connecting PC. It support the one set of master SPI interface and built-in internal clock for fewest external components request.

2. FEATURES

(1). Operation Frequency

- Internal clock or PLL with 6MHz crystal oscillator.
- Internal clock accuracy within 0.2% for USB application
- 24MHz for CPU clock

(2). On-Chip Memory

- 16k x 8 internal program MASK-ROM
- Internal RAM 256 bytes and external XRAM up to 320 bytes

(3). USB interface

- Compliance with Universal Serial Bus specification v2.0 Full Speed
- Built-in USB Transceiver, 3.3V regulator
- Software Control USB pull-up resister
- Support USB Suspend /Resume and Remote Wakeup function
- Endpoint 0: Control SETUP transfer (8 bytes)
- Endpoint 0: Control IN/OUT transfer (64 bytes)
- Endpoint 1: BULK-IN transfer with Ping-Pong feature (2*64 bytes)
- Endpoint 2: BULK-OUT transfer with Ping-Pong feature (2*64 bytes)
- Endpoint 3: INTERRUPT IN transfer (8 bytes)

(4). SPI Interface

- Mode0, 1, 2, 3
- Master mode
- Clock Rate up to 12Mbps
- Read DMA (up to 64 bytes per time)
- Write DMA (up to 64 bytes per time)

(5). Reset Controller

- Power On Reset
- Watch-Dog Timer

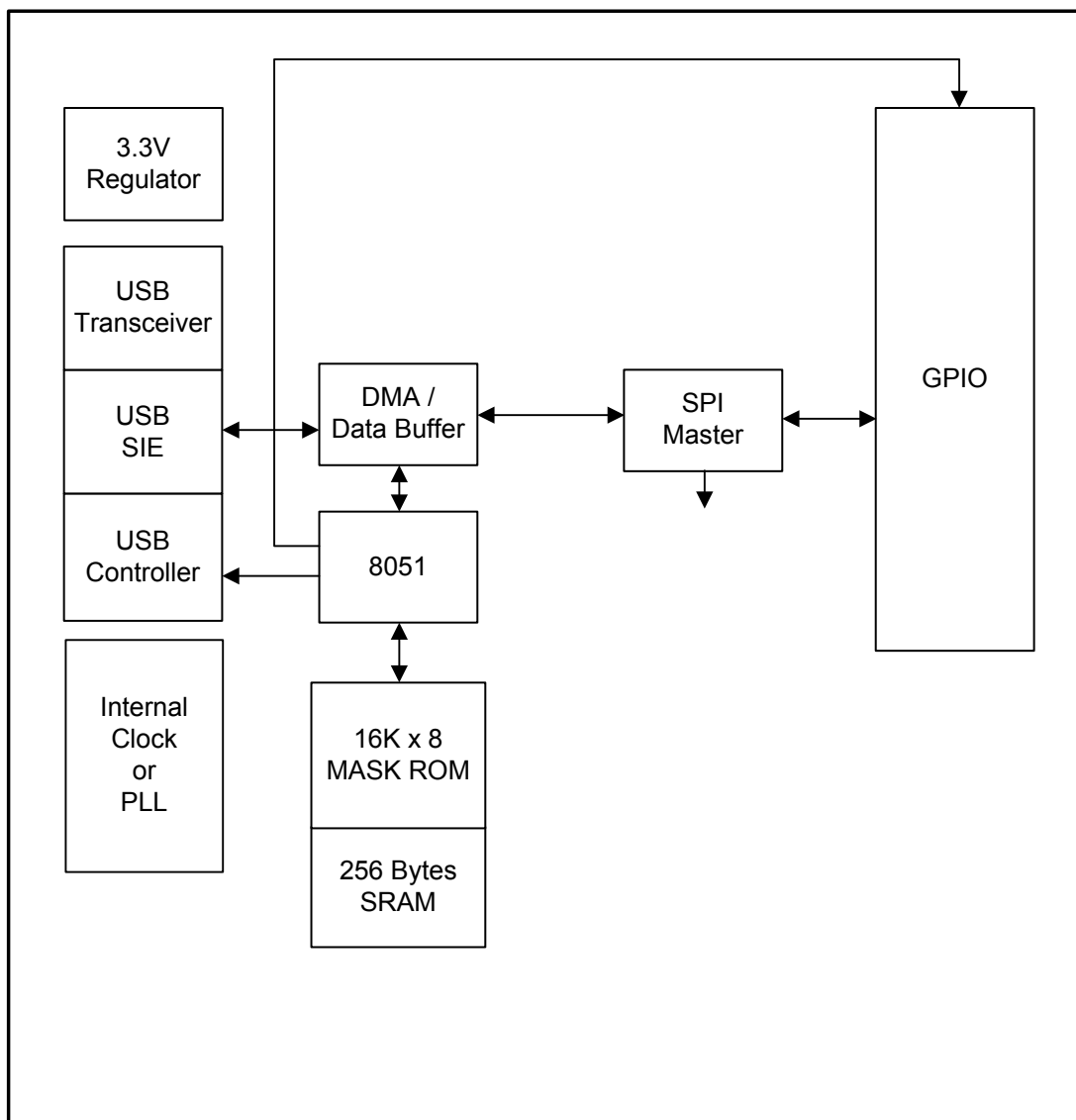
(6). I/O Ports

- Max. 8 GPIOs to flexible application
- 2 external Interrupts with wakeup function

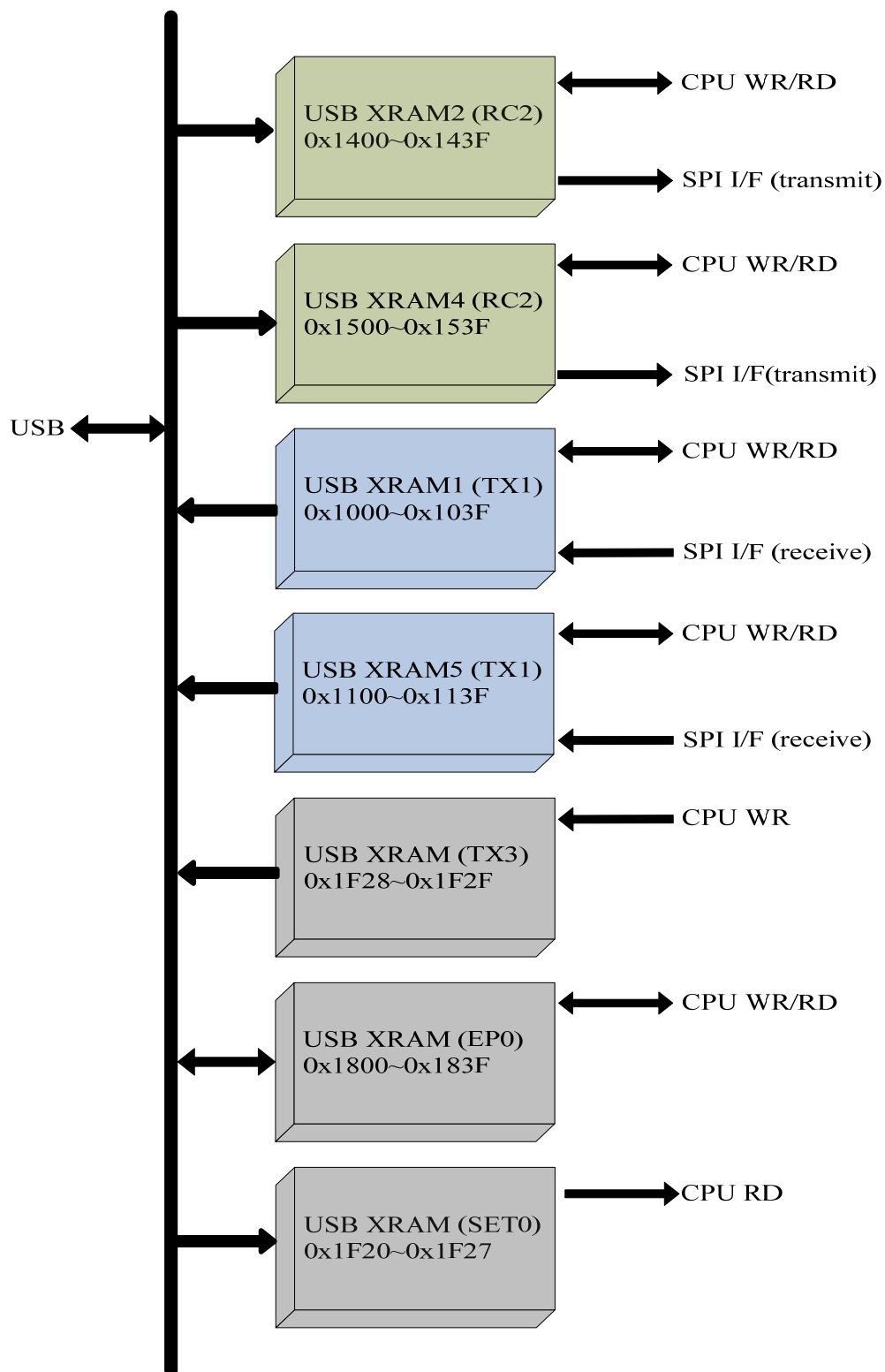
(7). Die Form / Customer Request**(8). Application**

- USB full speed general purpose
- USB to SPI bridge
- Web Key

3. Functional Block Diagram



4. XRAM Data Path



5. Pin Description

Name	I/O	Description				
VCC	P	5V Power from USB cable				
VSS	P	Ground				
V33	O	3.3V regulator output				
DP	I/O	USB positive data signal				
DM	I/O	USB negative data signal				
TESTn	I	Test Mode control (internal pull-up)				
FUSE4~0	I	Test Pins				
FX1	I	Crystal in 6MHz (optional)				
FX2	O	Crystal out (optional)				
VDDX	P	PLL power				
FLTC	I	PLL filter (optional)				
VSSX	P	PLL ground				
PC[2]	I/O	GPIO with wake-up interrupt				
PC[3]	I/O	GPIO with wake-up interrupt				
PC[4]	I/O	GPIO				
PC[5]	I/O	GPIO				
PC[6]		GPIO (b)				SPI CLK (o)
PC[7]		GPIO (b)				SPI DOUT (o)
PF[4]		GPIO (b)				SPI DIN (i)
PF[5]	I/O					

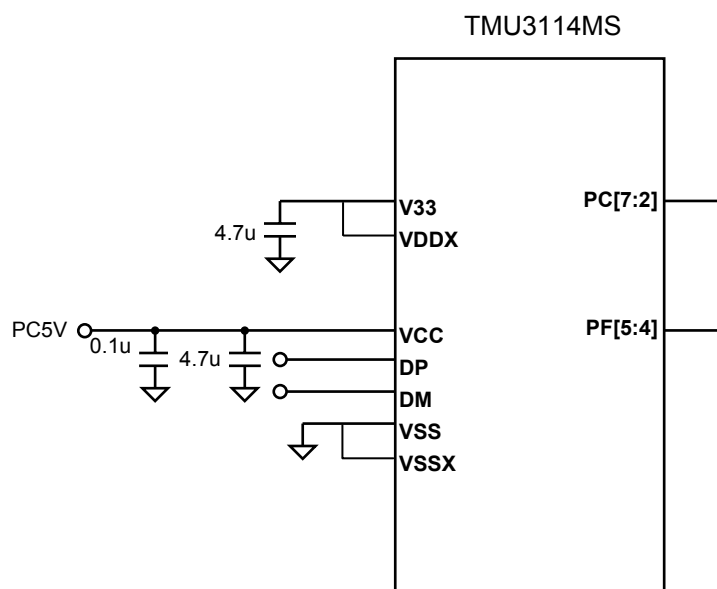
All I/O ports are pseudo-open drain types, unless otherwise specified function.

6. Memory Map

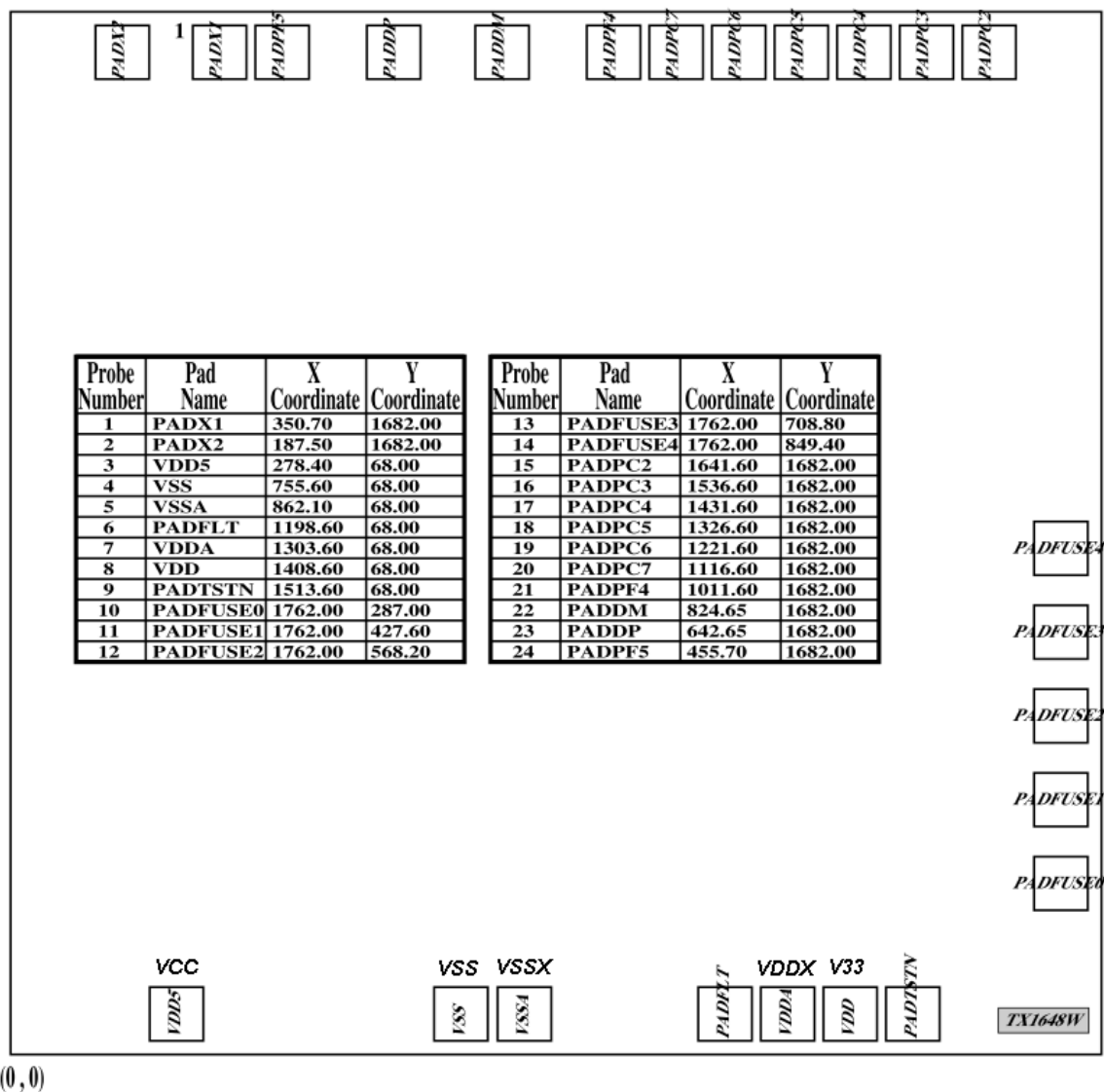
Name	Address	R/W	Rst	description
XRAM1	1000~103F	R/W	u	External RAM TX1 Buffer 1 (64 Bytes)
XRAM5	1100~113F	R/W	u	External RAM TX1 Buffer 5 (64 Bytes)
XRAM2	1400~143F	R/W	u	External RAM RC2 Buffer 2 (64 Bytes)
XRAM4	1500~153F	R/W	u	External RAM RC2 Buffer 4 (64 Bytes)
EP0RAM	1800~183F	R/W	u	EP0 OUT/TX Receive Buffer (64 Bytes)
SET0FIFO	1F20~1F27	R	u	EP0 SETUP Receive Buffer (8 Bytes)
TX3FIFO	1F28~1F2F	W	u	EP3 Transmit Buffer (8 Bytes)
DEVICE_R	1F00.7	R/W	1	USB DP pull-up R enable
USBADR	1F00.6~0	R/W	0	USB device address, clear while chip reset
OUTI0	1F01.7	R/W	0	EP0 OUT Receive Interrupt flag, write 0 to clear flag.
TX0I	1F01.6	R/W	0	EP0 Transmit Interrupt flag, write 0 to clear flag.
TX1I	1F01.5	R/W	0	EP1 Transmit Interrupt flag, write 0 to clear flag.
RC2I	1F01.4	R/W	0	EP2 Receive Interrupt flag, write 0 to clear flag.
RSTI	1F01.3	R/W	0	USB Bus Reset Interrupt flag, write 0 to clear flag.
RSMI	1F01.2	R/W	0	USB Resume Interrupt flag, write 0 to clear flag.
SUSPI	1F01.1	R/W	0	USB Suspend Interrupt flag, write 0 to clear flag.
SETI0	1F01.0	R/W	0	EP0 SETUP Receive Interrupt flag, write 0 to clear flag.
OUT0IE	1F02.7	W	0	OUT0I Interrupt enable (INT0)
TX0IE	1F02.6	W	0	TX0I Interrupt enable (INT0)
TX1IE	1F02.5	W	0	TX1I Interrupt enable (INT0)
RC2IE	1F02.4	W	0	RC2I Interrupt enable (INT0)
RSTIE	1F02.3	W	0	RSTI Interrupt enable (INT0)
RSMIE	1F02.2	W	0	RSMI Interrupt enable (INT0)
SUSPIE	1F02.1	W	0	SUSPI Interrupt enable (INT0)
SETIE	1F02.0	W	0	SET0I Interrupt enable (INT0)
SUSPND	1F03.7	R/W	0	S/W force USB interface into suspend mode.
RSMO	1F03.6	R/W	0	S/W force USB interface send RESUME signal in suspend mode.
OUT0RDY	1F03.0	R/W	0	EP0 ready for receive an OUT, clear by H/W while OUT0I/SET0I occurs.
OUT0TGL	1F04.7	R	0	1: received DATA1 packet; 0: received DATA0 Packet.
OUT0CNT	1F04.6~0	R	0	OUT0 Received data byte count.
TX0RDY	1F05.6	R/W	0	EP0 ready for transmit, clear by H/W while TX0I/SET0I occurs.
TX0TGL	1F05.5	R/W	0	EP0 transmit DATA1/DATA0 packet.
EP0STALL	1F05.4	R/W	0	EP0 will stall OUT/IN packet, clear by H/W while SET0I occurs.
RC0ERR	1F05.3	R	0	EP0 received data error.
TX0CNT	1F0B.6~0	W	0	EP0 transmit byte count
EP1STALL	1F06.7	R/W	0	EP1 stall.
EP1CFG	1F06.6	R/W	0	Set EP1 configuration
TX1RDY	1F06.5	R/W	0	EP1 ready for transmit, clear by H/W while TX1I occurs.
TX1TGL	1F06.4	R/W	0	EP1 transmit DATA1/DATA0 packet.
EP2STALL	1F07.7	R/W	0	EP2 stall.
EP2CFG	1F07.6	R/W	0	Set EP2 configuration.
RC2RDY	1F07.5	R/W	0	EP2 ready for receive, clear by H/W while RC2I occurs.
RC2TGL	1F07.4	R	0	1: received DATA1 packet; 0: received DATA0 Packet.
RC2ERR	1F07.3	R	0	EP2 received data error.
TX3IE	1F08.7	W	0	TX3I Interrupt enable (INT0)
TX1CNT	1F08.6~0	W	0	EP1 transmit byte count.
TX3I	1F09.7	R/W	0	EP3 transmit Interrupt flag, write 0 to clear flag.
RC2CNT	1F09.6~0	R	0	EP2 received data byte count.
EP3STALL	1F0A.7	R/W	0	EP3 stall.
EP3CFG	1F0A.6	R/W	0	Set EP3 configuration.
TX3RDY	1F0A.5	R/W	0	EP3 ready for transmit, clear by H/W while TX3I occurs.
TX3TGL	1F0A.4	R/W	0	EP3 transmit DATA1/DATA0 packet.
TX3CNT	1F0A.3~0	W	0	EP3 transmit byte count.

XRAM1USB	1F0C.7~5	R/W	0	111:USB TX1 Bulk-IN	010:SPI-RCFIFO to XRAM1	000:CPU W/R
XRAM2USB	1F0C.4~2	R/W	0	111:USB RC2 Bulk-OUT	010:DMA to SPI-TXFIFO	000:CPU W/R
XRAM5USB	1F1B.7~5	R/W	0	111:USB TX1 Bulk-IN	010:SPI-RCFIFO to XRAM5	000:CPU W/R
XRAM4USB	1F1B.4~2	R/W	0	111:USB RC2 Bulk-OUT	010:DMA to SPI-TXFIFO	000:CPU W/R
EP0RAMUSB	1F0D.7	R/W	0	Assign EP0RAM as USB OUT0/TX0 transfer buffer		
DMASPI_BUSY	1F0D.0	R	0	SPIFIFO DMA write/read busy flag		
DMASPI_S	1F0E.7	R/W	1	Low to high to start DMA XRAM2/XRAM4 to SPI FLASH		
DMASPI_LEN	1F0E.6~0	R/W	1	DMASPI data length		
SPI MASTER						
CPOL	1F52.6	W	0	SPIMCLK idle state, (1:High 0:Low)		
CPHA	1F52.5	W	0	SPIMCLK phase		
BSL[3:0]	1F52.4~1	W	7	Buffer shift bit counter(0111:8bit)		
SPI_EN	1F53.7	R/W	0	Enable SPI Master function		
CRS[6:0]	1F53.6~0	R/W	0	Clock rate select {CPUCLK/2*(CRS+1)}		
I/O INT						
EXINT2I	1F81.2	R/W	0	PC2 interrupt flag, write 0 to clear flag		
EXINT3I	1F81.3	R/W	0	PC3 interrupt flag, write 0 to clear flag		
EXINT2IE	1F82.2	W	0	PC2 external interrupt enable (INT1)		
EXINT3IE	1F82.3	W	0	PC3 external interrupt enable (INT1)		
MISC						
PWR_DN	1F8B	W	0	Power Down Mode		
WDT_FLG	1F8C.5	R/W	0	WatchDog overflow flag(CPUCLK*2^15), write 0 or RST_P=1 to clear flag		
WDTe	1F8E	W	0	Clear WDT and enable WDT (clock source form CPU clock)		
TESTreg	1F8F.7~0	W	0	Test Mode option, keep 0 in normal mode		
I/O						
PC7	1F9C.7	R/W	1	PC7 as GPIO or SPIA serial data output(SDO), depend on PC7CON		
PC6	1F9C.6	R/W	1	PC6 as GPIO or SPIA SCK0(master), depend on PC6CON		
PC5	1F9C.5	R/W	1	PC5 as GPIO		
PC4	1F9C.4	R/W	1	PC4 as GPIO		
PC3	1F9C.3	R/W	1	PC3 as GPIO with interrupt wakeup-up function		
PC2	1F9C.3	R/W	1	PC2 as GPIO with interrupt wakeup-up function		
PC7CON	1FAC.7	R/W	1	1:PC7 as GPIO, 0:PC7 as SPIA serial data output for master		
PC6CON	1FAC.6	R/W	1	1:PC6 as GPIO, 0:PC6 as SPIA clock output(master)		
PF5	1F9F.5	R/W	1	GPIO		
PF4	1F9F.4	R/W	1	GPIO or SPIA serial data input (SDI), depend on PF4CON		
PF4CON	1FAF.4	R/W	1	1:PF4 as GPIO, 0:PF4 as SPIA serial data input(SDI) for master		

7. Application Circuit



8. PAD list



9. Electrical Characteristics

(1). ABSOLOUTE MAXIMUM RATINGS (VSS = 0V)

Name	Symbol	Range	Unit
Maximum Supply Voltage	VCC	-0.3 to 5.5	V
Maximum Input Voltage	Vin	-0.3 to VCC + 0.3	V
Maximum output Voltage	Vout	-0.3 to VCC + 0.3	V
Maximum Operating Temperature	Topg	-10 to + 70	°C
Maximum Storage Temperature	Tstg	-25 to + 125	°C

(2). RECOMMEND OPERATING CONDITION (at Ta = -10°C to 70°C, VSS = 0V)

Name	Symb.	Min.	Max.	Unit
Supply Voltage	VCC	4.5	5.5	V
Input "H" Voltage	Vih	0.9 x VCC	VCC	V
Input "L" Voltage	Vil	0	0.1 x VCC	V

(3). DC CHARACTERISTICS (at Ta = 25°C, VCC = 5.0V, VSS = 0V, unless otherwise specify)

Name	Symb.	Min.	Typ.	Max.	Unit	Condition	Note
CPU Clock	fclk1	-2%	24	+2%	MHz	Internal Clock enable	
	fclk2	+2%	24	+2%	MHz	Crystal 6MHz, PLL enable	
Internal Clock	Firc	-0.2%	48	0.2%	MHz	Internal Clock enable	
Operating current	Icc1		6		mA	Internal clock	No load
	Icc2		5		mA	PLL clock	No load
Suspend current	Isus		380	500	uA	USB mode	No load
Output high current	Ioh1	5	7	-	mA	Voh=3.0V, V33=3.3V	One clk time
	Ioh2	3	8	-	uA		
Output low current	Iol1	17	24	-	mA	Vol = VSS + 0.4v,	
Input high voltage	Vih1	2		VCC	V	V33 = 3.3V	
Input low voltage	Vil1			1.2	V	V33 = 3.3V	
Pull up resistance	Rup1	80	100	120	KΩ	V33 = 3.3V	
V33 pin voltage	V33	3.0	3.3	3.6	V		
V33 output current	I33		100		mA	V33=3.0V, average current	

(4). USB AC CHARACTERISTICS (at Ta = 25°C, VCC = VDDX = 5.0V, VSS = VSSX = 0V)

Name	Symb.	Min.	Typ.	Max.	Unit	Note
DP/DM rising time	Trise	4		20	ns	
DP/DM falling time	Tfall	4		20	ns	
DP,DM cross point	Vx	1.3		2.0	V	
V33 output voltage	Vreg	3.0	3.3	3.6	V	

Note: All the USB transceiver characteristics meet USB1.1 spec.