TM87R04

4-Bit Microcontroller with LCD Driver

Data Sheet

AMENDMENT HISTORY

Version	Date	Description
V1.0	May, 2011	New release
V1.1	Dec, 2011	Add Ordering Information table.

CONTENTS

GENERAL DESCRIPTION

TM87R04 is a Mask ROM embedded high-performance 4-bit micro controller with LCD driver.

FEATURE

1. Powerful instruction set (100 instructions)
- Binary addition, subtraction, BCD adjusts, logical operation in direct and index addressing mode
- Single-bit manipulation (set, reset, decision for branch)
- Various conditional branches
- 16 working registers and manipulation
- LCD driver data transfer

2. Memory capacity
- Program ROM capacity 8186 x 8 bits
- Data RAM capacity 128 x 4 bits

3. Input/output ports
- Port IOA 4 pins (with internal pull-low)
- Port IOB 2 pins (with internal pull-low)
- Port IOC 4 pins (with internal pull-low, chattering prevention clock)
- Port IOD 4 pins (with internal pull-low)

4. 8 level subroutine nesting

5. Interrupt function
- External factor 2 (INT pin, Port IOC)
- Internal factor 3 (Pre-Divider, Timer1, Timer2)

6. Built in Alarm, Frequency or Melody generator

7. BZB, BZ [Mux*(Multiplex System)* with IOB3, IOB4]

8. Two 6-bit programmable timers with programmable clock source

9. LCD driver output
- 32 LCD driver outputs (up to 128 LCD segment drivable)
- 1/4 Duty for LCD
- 1/2 Bias or 1/3 Bias (1V or 1.5V step) for LCD selected by option
- Single instruction to turn off all segments
- 16 LCD address

10. Built-in Voltage doublers, and halve charge pump circuit.

11. Dual clock operation, X'tal type slow oscillation, and fast oscillation can set 3.58MHz ceramic resonator or external R by switch option.

12. Watch dog timer

13. HALT function

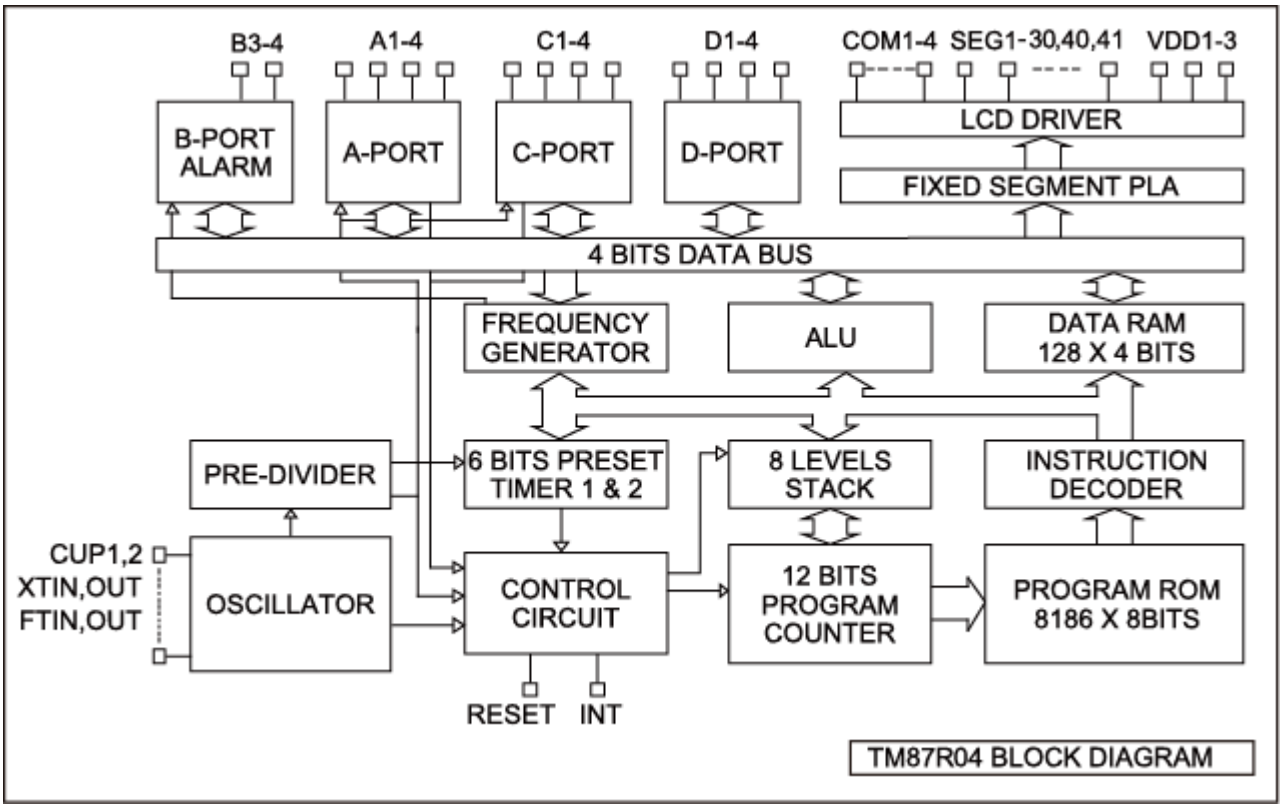
14. STOP function

15. Fixed LCD PLA configuration

APPLICATION

- Timer / Calendar / Calculator

BLOCK DIAGRAM



PIN ASSIGNMENT

No	Name	No	Name
1	XIN	30	SEG15
2	XOUT	31	SEG16
3	FTIN	32	SEG17
4	FTOUT	33	SEG18
5	GND	34	SEG19
6	VDD1	35	SEG20
7	VDD(2)	36	SEG21
8	TEST	37	SEG22
9	VDD3	38	SEG23
10	CUP1	39	SEG24/IOA1
11	CUP2	40	SEG25/IOA2
12	COM1	41	SEG26/IOA3
13	COM2	42	SEG27/IOA4
14	COM3	43	SEG28
15	COM4	44	SEG29
16	SEG1	45	SEG30/IOB3/BZB
17	SEG2	46	IOB4/BZ
18	SEG3	47	IOC1
19	SEG4	48	IOC2
20	SEG5	49	IOC3
21	SEG6	50	IOC4
22	SEG7	51	IOD1
23	SEG8	52	IOD2
24	SEG9	53	IOD3
25	SEG10	54	IOD4
26	SEG11	55	SEG40
27	SEG12	56	SEG41
28	SEG13	57	RESET
29	SEG14	58	INT

PIN DESCRIPTION

Name	I/O	Description
VDD1, 2, 3	P	✧ LCD supply voltage, and positive supply voltage. ✧ Connect +3.0V battery positive pin to VDD2 (for 1/3 bias 1.5V step) or VDD3 (for 1/3 bias 1V step).
RESET	I	✧ Input pin from LSI reset request signal, with internal pull-down resistor.
INT	I I/O	✧ Input pin for external INT request signal. ✧ Falling edge or rising edge triggered by option. ✧ Internal pull-down or pull-up resistor is selected by option. ✧ Serial Data for Serial Program/Read Mode.
TEST	I	✧ Test signal input pin.
CUP1, 2	O	✧ Switching pins for supply the LCD driving voltage to the VDD1, 2, 3 pins. ✧ Connect the CUP1 and CUP2 pins with non-polarized electrolytic capacitor if 1/2 or 1/3 bias mode has been selected. In no BIAS mode, these pins should be open.
XIN XOUT	I O	✧ 32KHz Crystal oscillator for Slow Clock. If XIN pin is unused, it must be connected to VDD2.
FTIN FTOUT	I O	✧ 3.58MHz ceramic resonator oscillator for Fast Clock. External R oscillation for Fast Clock. If FTIN pin is unused, it must be connected to GND.
COM1~4	O	✧ Output pins for driving the common pins of the LCD panel.
SEG1-29, 30,40, 41	O	✧ Output pins for driving the LCD panel segment.
IOA1-4	I/O	✧ Input / Output port-A, can use software to define internal pull-low Resistor. ✧ This port is multiplexed with SEG24~27, and set by option.
IOB3-4	I/O	✧ Input / Output port-B, can use software to define internal pull-low Resistor. ✧ This port is multiplexed with BZB, BZ, and set by option.
IOC1-4	I/O	✧ Input / Output port-C, can use software to define internal pull-low and chattering clock to reduce input bounce.
IOD1-4	I/O	✧ Input / Output port-D, can use software to define internal pull-low Resistor, and Chattering clock to reduce input bounce.
(ALM) BZB/BZ	O	✧ Output port for alarm, frequency or melody generator. ✧ This port is multiplexed with IOB3, 4, and set by option.
GND	P	✧ Negative supply voltage.

Fixed PLA Table

SEGn	Lz	COM1	COM2	COM3	COM4
SEG1	00H	DBUSA	DBUSB	DBUSC	DBUSD
SEG2		DBUSE	DBUSF	DBUSG	DBUSH
SEG3	01H	DBUSA	DBUSB	DBUSC	DBUSD
SEG4		DBUSE	DBUSF	DBUSG	DBUSH
SEG5	02H	DBUSA	DBUSB	DBUSC	DBUSD
SEG6		DBUSE	DBUSF	DBUSG	DBUSH
SEG7	03H	DBUSA	DBUSB	DBUSC	DBUSD
SEG8		DBUSE	DBUSF	DBUSG	DBUSH
SEG9	04H	DBUSA	DBUSB	DBUSC	DBUSD
SEG10		DBUSE	DBUSF	DBUSG	DBUSH
SEG11	05H	DBUSA	DBUSB	DBUSC	DBUSD
SEG12		DBUSE	DBUSF	DBUSG	DBUSH
SEG13	06H	DBUSA	DBUSB	DBUSC	DBUSD
SEG14		DBUSE	DBUSF	DBUSG	DBUSH
SEG15	07H	DBUSA	DBUSB	DBUSC	DBUSD
SEG16		DBUSE	DBUSF	DBUSG	DBUSH
SEG17	08H	DBUSA	DBUSB	DBUSC	DBUSD
SEG18		DBUSE	DBUSF	DBUSG	DBUSH
SEG19	09H	DBUSA	DBUSB	DBUSC	DBUSD
SEG20		DBUSE	DBUSF	DBUSG	DBUSH
SEG21	0AH	DBUSA	DBUSB	DBUSC	DBUSD
SEG22		DBUSE	DBUSF	DBUSG	DBUSH
SEG23	0BH	DBUSA	DBUSB	DBUSC	DBUSD
SEG24		DBUSE	DBUSF	DBUSG	DBUSH
SEG25	0CH	DBUSA	DBUSB	DBUSC	DBUSD
SEG26		DBUSE	DBUSF	DBUSG	DBUSH
SEG27	0DH	DBUSA	DBUSB	DBUSC	DBUSD
SEG28		DBUSE	DBUSF	DBUSG	DBUSH
SEG29	0EH	DBUSA	DBUSB	DBUSC	DBUSD
SEG30		DBUSE	DBUSF	DBUSG	DBUSH
SEG40	0FH	DBUSA	DBUSB	DBUSC	DBUSD
SEG41		DBUSE	DBUSF	DBUSG	DBUSH

ABSOLOUTE MAXIMUM RATINGS

(GND= 0V)

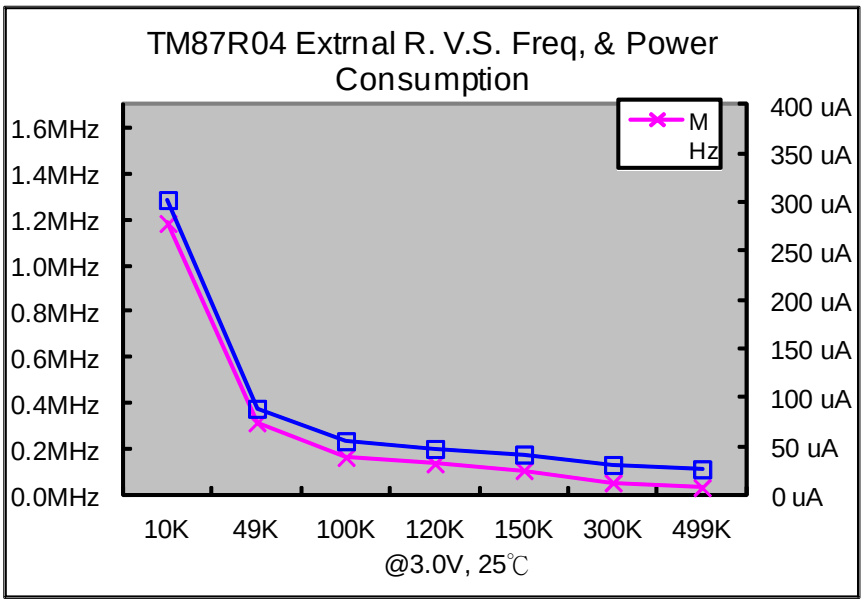
Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 3.6	V
	VDD2		
	VDD3		
Maximum Input Voltage	Vin	-0.3 to VDD1/2+0.3	
Maximum output Voltage	Vout1	-0.3 to VDD1/2+0.3	
	Vout2	-0.3 to VDD3+0.3	
Maximum Operating Temperature	Topg	-20 to +70	℃
Maximum Storage Temperature	Tstg	-25 to +125	

POWER CONSUMPTION

at VDD2= 3.0V, Ta=-20℃ to 70℃, GND= 0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT	Only 32.768KHz Crystal oscillator operating, without loading. BCF = 0, PH0=BCLK		3	6	uA
STOP mode	ISTOP				1	
Normal Mode	I_{32K}	Only 32.768KHz Crystal oscillator operating, without loading. BCF = 0, PH0=BCLK	7.5			
External R	$I_{Ext.\ R}$	R = 150KΩ oscillator operating, without loading. BCF = 0, PH0=BCLK	36			
3.58MHz ceramic resonator	$I_{3.58Mcr}$	Only 3.58MHz ceramic resonator operating, without loading. BCF = 0, PH0=BCLK	480			

Note: When External R oscillator mode is operating, the current consumption will depend on the frequency of oscillation.



ALLOWABLE OPERATING CONDITIONS

(@ VDD=3.0V Ta=-20℃ to 70℃,GND= 0V)

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD2	1/2, 1/3 Bias (1.5V step)	2.4	3.6	V
	VDD3	1/3 Bias (1V step)			
Oscillator Start-Up Voltage	VDD_{stup}	32.768KHz Crystal Mode	1.4		
		3.58MHz ceramic resonator Mode	1.8		
Oscillator Sustain Voltage	VDD_{sut}	32.768KHz Crystal Mode	1.3		
		3.58MHz ceramic resonator Mode	1.55		
Input “H” Voltage	Vih1	Li Battery Mode	VDD2-0.7	VDD2+0.7	
Input “L” Voltage	Vil1		-0.7	0.7	
Input “H” Voltage	Vih2	1/3 Bias (1V step)	VDD3-0.7	VDD3+0.7	
Input “L” Voltage	Vil2		-0.7	0.7	
Input “H” Voltage	Vih3	XTIN/FTIN at 3V Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil3		0	0.2xVDD2	
Operating Freq	Fopg1	32.768KHz Crystal Mode	32		KHZ
	Fopg2	External R mode	10	1000	
	Fopg3	3.58MHz ceramic resonator	455	4000	

ELECTRICAL CHARACTERISTICS

at#1:VDD2=2.4V(Li)

- **Input Resistance**

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
“L” Level Hold Tr(IOC)	Rllh1	Vi=0.2VDD2	10	40	100	KΩ
IOA,B,C Pull-Down Tr	Rmad1	Vi=VDD2	200	500	1000	
INT Pull-up Tr	Rintu1	Vi=VDD2	200	500	1000	
INT Pull-Down Tr	Rintd1	Vi=GND	200	500	1000	
RES Pull-Down R	Rres1	Vi=GND or VDD2	9	35	90	

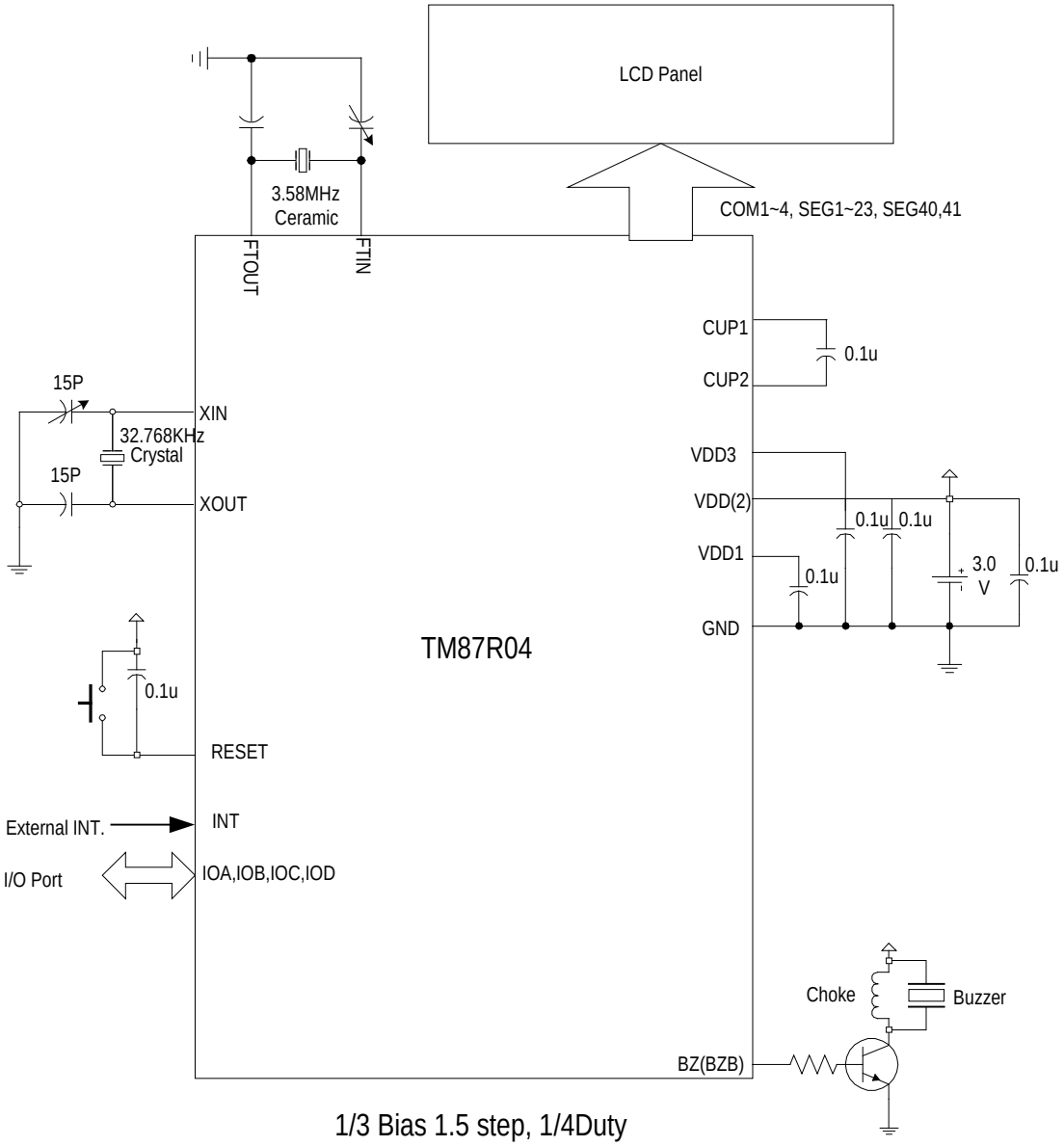
- **Segment Driver Output Characteristics**

  VDD2(1.5V step) or VDD3(1V step) =2.4V(Li)

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias (1.5V step) Display Mode							
Output ”H” Voltage	Voh3f	Ioh=-1uA	SEG-n	2.2			V
Output ”L” Voltage	Vol3f	Iol=1uA				0.2	
Output ”H” Voltage	Voh3g	Ioh=-10uA	COM-n	2.2			
Output ”M” Voltage	Vom3g	Iol/h=+/-10uA		1.0		1.4	
Output ”L” Voltage	Vol3g	Iol=10uA				0.2	
1/3 Bias (1.5V step) Display Mode							
Output ”H” Voltage	Voh3i	Ioh=-1uA	SEG-n	3.4			V
Output ”M1” Voltage	Vom13i	Iol/h=+/-10uA		1.0		1.4	
Output ”M2” Voltage	Vom23i	Iol/h=+/-10uA		2.2		2.6	
Output ”L” Voltage	Vol3i	Iol=1uA				0.2	
Output ”H” Voltage	Voh3j	Ioh=-10uA	COM-n	3.4			
Output ”M1” Voltage	Vom13j	Iol/h=+/-10uA		1.0		1.4	
Output ”M2” Voltage	Vom23j	Iol/h=+/-10uA		2.2		2.6	
Output ”L” Voltage	Vol3j	Iol=10uA				0.2	
1/3 Bias (1V step) Display Mode							
Output ”H” Voltage	Voh5i	Ioh=-1uA	SEG-n	2.2			V
Output ”M1” Voltage	Vom15i	Iol/h=+/-10uA		0.6		1.0	
Output ”M2” Voltage	Vom25i	Iol/h=+/-10uA		1.4		2.8	
Output ”L” Voltage	Vol5i	Iol=1uA				0.2	
Output ”H” Voltage	Voh5j	Ioh=-10uA	COM-n	2.2			
Output ”M1” Voltage	Vom15j	Iol/h=+/-10uA		0.6		1.0	
Output ”M2” Voltage	Vom25j	Iol/h=+/-10uA		1.4		2.8	
Output ”L” Voltage	Vol5j	Iol=10uA				0.2	

TYPICAL APPLICATION CIRCUIT

This application circuit is simply an example, and is not guaranteed to work.



1/3 Bias 1.5 step, 1/4Duty

INSTRUCTION TABLE

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 0010 ZZZZ YYYY	Lz	← (7SEG ← Ry)	(Ry=70H~7FH)
LCB	Lz,Ry	0000 0100 ZZZZ YYYY	Lz	← (7SEG ← Ry) Blank Zero	(Ry=70H~7FH)
LCP	Lz,Ry	0000 0110 ZZZZ YYYY	Lz	← Ry & AC	(Ry=70H~7FH)
OPA	Rx	0000 1010 0XXX XXXX	Port(A)	← Rx	
OPAS	Rx,D	0000 1011 DXXX XXXX	A1,2,3,4	← Rx0,Rx1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	Port(B)	← Rx	
OPC	Rx	0000 1101 0XXX XXXX	Port(C)	← Rx	
OPD	Rx	0000 1110 0XXX XXXX	Port(D)	← Rx	
FRQ	D,Rx	0001 00DD 0XXX XXXX	FREQ D=00 D=01 D=10 D=11	← Rx & AC : 1/4 Duty : 1/3 Duty : 1/2 Duty : 1/1 Duty	
FRQX	D,X	0001 10DD XXXX XXXX	FREQ	← X	
ADC	Rx	0010 0000 0XXX XXXX	AC	← Rx + AC + CF	CF
ADC*	Rx	0010 0001 0XXX XXXX	AC,Rx	← Rx + AC + CF	CF
SBC	Rx	0010 0010 0XXX XXXX	AC	← Rx + ACB + CF	CF
SBC*	Rx	0010 0011 0XXX XXXX	AC,Rx	← Rx + ACB + CF	CF
ADD	Rx	0010 0100 0XXX XXXX	AC	← Rx + AC	CF
ADD*	Rx	0010 0101 0XXX XXXX	AC,Rx	← Rx + AC	CF
SUB	Rx	0010 0110 0XXX XXXX	AC	← Rx + ACB + 1	CF
SUB*	Rx	0010 0111 0XXX XXXX	AC, Rx	← Rx + ACB + 1	CF
ADN	Rx	0010 1000 0XXX XXXX	AC	← Rx + AC	
ADN*	Rx	0010 1001 0XXX XXXX	AC, Rx	← Rx + AC	
AND	Rx	0010 1010 0XXX XXXX	AC	← Rx AND AC	
AND*	Rx	0010 1011 0XXX XXXX	AC, Rx	← Rx AND AC	
EOR	Rx	0010 1100 0XXX XXXX	AC	← Rx EOR AC	
EOR*	Rx	0010 1101 0XXX XXXX	AC, Rx	← Rx EOR AC	
OR	Rx	0010 1110 0XXX XXXX	AC	← Rx OR AC	
OR*	Rx	0010 1111 0XXX XXXX	AC, Rx	← Rx OR AC	
ADCI	Ry,D	0011 0000 DDDD YYYY	AC	← Ry + D + CF	
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC, Ry	← Ry + D + CF	
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	← Ry + DB + CF	
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC, Ry	← Ry + DB + CF	
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	← Ry + D	
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC, Ry	← Ry + D	
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	← Ry + DB + 1	
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC, Ry	← Ry + DB + 1	

Instruction		Machine Code	Function		Flag/Remark
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	← Ry + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC, Ry	← Ry + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	← Ry AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC, Ry	← Ry AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	← Ry EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC, Ry	← Ry EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	← Ry OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC, Ry	← Ry OR D	
INC*	Rx	0100 0000 0XXX XXXX	AC, Rx	← Rx + 1	CF
DEC*	Rx	0100 0001 0XXX XXXX	AC,Rx	← Rx – 1	CF
IPA	Rx	0100 0010 0XXX XXXX	AC, Rx	← Port(A)	
IPB	Rx	0100 0100 0XXX XXXX	AC, Rx	← Port(B)	
IPC	Rx	0100 0111 0XXX XXXX	AC, Rx	← Port(C)	
IPD	Rx	0100 1000 0XXX XXXX	AC, Rx	← Port(D)	
MAF	Rx	0100 1010 0XXX XXXX	AC, Rx	← STS1	B3 : CF B2 : ZERO B1 : (unused) B0 : (unused)
MSB	Rx	0100 1011 0XXX XXXX	AC, Rx	← STS2	B3 : (unused) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF
MSC	Rx	0100 1100 0XXX XXXX	AC, Rx	← STS3	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT)
MCX	Rx	0100 1101 0XXX XXXX	AC, Rx	← STS3X	B3 : (unused) B2 : (unused) B1 : SCF6(TM2) B0 : (unused)
MSD	Rx	0100 1110 0XXX XXXX	AC, Rx	← STS4	B3 : (unused) B2 : (unused) B1 : WDF B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	ACn, Rxn AC3, Rx3	← Rx(n+1) ← 1	
SL0	Rx	0101 0010 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	ACn, Rxn AC0, Rx0	← Rx(n-1) ← 1	
DAA		0101 0100 0000 0000	AC	← BCD(AC)	CF
DAA*	Rx	0101 0101 0XXX XXXX	AC,Rx	← BCD(AC)	CF
DAS		0101 0110 0000 0000	AC	← BCD(AC)	CF

Instruction		Machine Code	Function		Flag/Remark
DAS*	Rx	0101 0111 0XXX XXXX	AC,Rx	← BCD(AC)	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	AC,Rx	← D	
STA	Rx	0110 1000 0XXX XXXX	Rx	← AC	
LDA	Rx	0110 1100 0XXX XXXX	AC	← Rx	
MRA	Rx	0110 1101 0XXX XXXX	CF	← Rx3	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	AC, Ry	← Rx	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	AC, Rx	← Ry	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 PXXX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 PXXX XXXX XXXX	PC	← X	
TMS	Rx	1110 0000 0XXX XXXX	AC3,2 = 11 AC3,2 = 10 AC3,2 = 01 AC3,2 = 00 AC1,0,PB3~0	: Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TMSX	X	1110 001X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100X 8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
TM2	Rx	1110 0100 0XXX XXXX	Timer2	← Rx & AC	
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111 X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH13 : Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 000X XXX0	X4 X3 X2	: Enable HEF4 : Enable HEF3 : Enable HEF2	TMR2 PDV INT

Instruction		Machine Code	Function		Flag/Remark
			X1	: Enable HEF1	TMR1
SIE*	X	1110 1001 000X XXXX	X4 X3 X2 X1 X0	: Enable IEF4 : Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	TMR2 PDV INT TMR1 CPT
PLC	X	1110 101X 000X XXXX	X8 X4 X3 X2 X1 X0	: Reset PH15~11 : Reset HRF4 : Reset HRF3 : Reset HRF2 : Reset HRF1 : Reset HRF0	 TMR2 PDV INT TMR1 CPT
SRE	X	1110 1101 00XX 0000	X5 X4	: Enable SRF5(INT) : Enable SRF4(C port)	
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1110 1000 0000	SCLK	: Low Speed Clock	
RTS		1111 0100 0000 0000	PC	←STACK (CALL Return)	
SCC	X	1111 0100 1X0X 0XXX	X6 = 1 X6 = 0 X4 = 1 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 : Set P(C) Cch : Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1111 0101 000X 0000	X4	: Enable SEF4(C1-4)	
SPA	X	1111 0101 100X XXXX	X4 X3~0	: Set A4-1 Pull-Low : Set A4-1 I/O	1:Pull low 1:Output, 0: Input
SPB	X	1111 0101 101X XX00	X4 X3,2	: Set B4-1 Pull-Low : Set B4,3 I/O	1:Pull low 1:Output, 0: Input
SPC	X	1111 0101 110X XXXX	X4 X3-0	: Set C4-1 Pull-Low : Set C4-1 I/O	1:Pull low 1:Output, 0: Input
SPD	X	1111 0101 111X XXXX	X4 X3-0	: Set D4-1 Pull-Low : Set D4-1 I/O	1:Pull low 1:Output, 0: Input
SF	X	1111 0110 X00X 00XX	X7 X4 X1 X0	: Reload 1 Set : WDT Enable : BCF Set : CF Set	
RF	X	1111 0111 X00X 00XX	X7 X4 X1 X0	: Reload 1 Reset : WDT Reset : BCF Reset : CF Reset	
ALM	X	1111 110X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	

Instruction		Machine Code	Function		Flag/Remark
SF2	X	1111 1110 0000 XX0X	X3 X2 X0	: Enable INT powerful Pull low : Close all Segments : Reload 2 Set	
RF2	X	1111 1110 1000 XX0X	X3 X2 X0	: Disable INT powerful Pull low : Release Segments : Reload 2 Reset	
HALT		1111 1111 0000 0000	Halt Operation		
STOP		1111 1111 1000 0000	Stop Operation		

Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	D	Immediate Data
AC	Accumulator	(D)B	Complement of Immediate Data
(AC)n	Content of Accumulator (bit n)	PC	Program Counter
(AC)B	Complement of content of Accumulator	CF	Carry Flag
X	Address of program or control data	ZERO	Zero Flag
Rx	Address X of data RAM	WDF	Watch-Dog Timer Enable Flag
(Rx)n	Bit n content of Rx	7SEG	7 segment decoder for LCD
Ry	Address Y of working register	BCLK	System clock for instruction
BCF	Backup flag	IEFn	Interrupt Enable Flag
TMR	Timer Overflow Release Flag	HRFn	HALT Release Flag
Ctm	Clock Source of Timer	HEFn	HALT Release Enable Flag
PDV	Pre-Divider	Lz	Address of LCD PLA Latch
STACK	Content of stack	SRFn	STOP Release Enable Flag
TM1	Timer 1	SCFn	Start Condition Flag
TM2	Timer 2	Cch	Clock Source of Chattering prevention ckt.
FREQ	Frequency Generator setting Value	Cfq	Clock Source of Frequency Generator
CSF	Clock Source Flag	SEFn	Switch Enable Flag
P	Program Page		

ORDERING INFORMATION

The ordering information:

Ordering number	Package
TM87R04-COD	Wafer / Dice with code