十速科技股份有限公司
tenx technology inc.

Advance Information

TM57PR40

8-Bit Microcontroller

Data Sheet

Tenx reserves the right to change or discontinue this product without notice.

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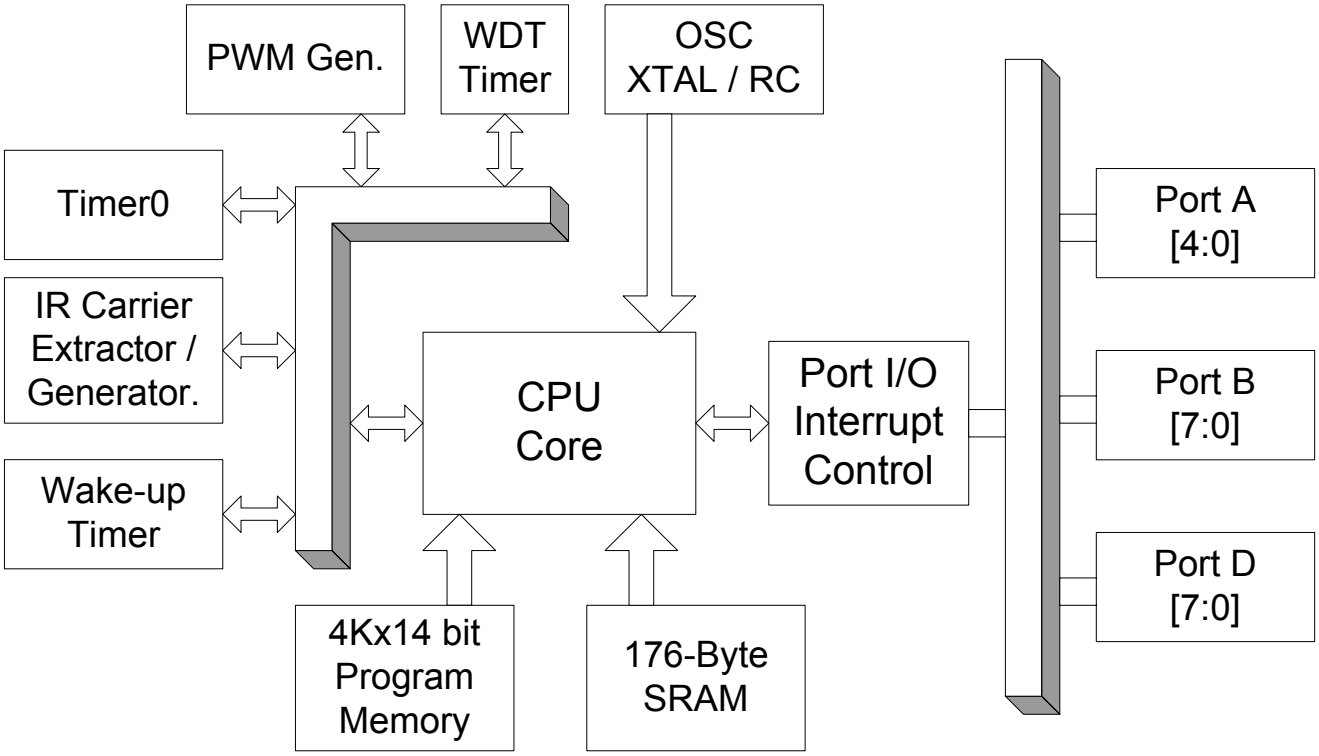
FEATURE

1. ROM: 4K x 14 bits
2. RAM: 176 x 8 bits
3. STACK: 5 Levels
4. I/O ports: Three I/O ports (Max 21 pins)
5. Timer: One 8-bit timer with reload/prescale
6. Built-in 11-bit IR carrier extractor (covering 10KHz to 100KHz carrier)
7. IR Carrier output with 11-bit resolution
8. Watchdog Timer: On chip WDT based on system clock
9. Power-On Reset & Watchdog timer overflow Reset & Low Voltage reset (Note-1)
10. On chip wake-up timer can wake CPU up every 64ms by interrupt and can be turned off.
11. Oscillation Frequency:
    - 1MHz to 20 MHz external crystal oscillator
      Maximum operating frequency are 12MHz @ VDD=3V and 16MHz @ VDD=5V
    - RC (External C)
12. Operation Voltage: 2.2V to 5.5V
13. Instruction set: 36 Instructions
14. Execution Time: 200 ns at 10 MHz f_{OSC} (minimum)
15. Interrupts: 4 interrupt sources with one vector and interrupt level
    - Timer0 Overflow
    - PA0 interrupt
    - Wake-up timer interrupt
    - Port B interrupt
16. System Configure Option: Protection(SBT[0]), OSC Mode(SBT[1]) and LVREN(SBT[2])
17. Reset vector: 000H
18. Interrupt vector: 001H
19. Power Down mode
20. Package Types:
    - SOP 28L – 300mil
    - SOP 24L – 300mil
    - Die form

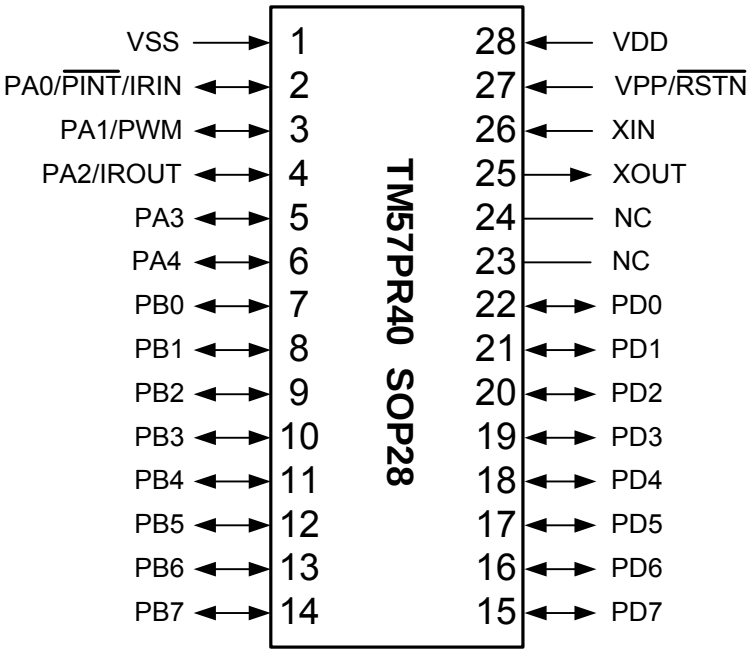
Note-1: Power-On-Reset (POR) and Low-Voltage-Reset (LVR) are controlled by FUSE bit. They are built in the same circuit, and on or off simultaneously. If POR or LVR is disabled, please use an external reset circuit to reset the CPU.

System Block Diagram

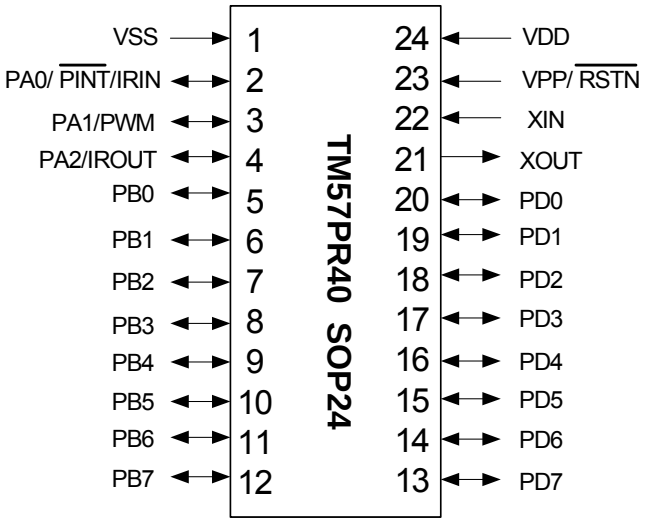


<Figure-1: System Block Diagram>

Pin Order Diagram



<Figure-2: SOP-28 Pin assignment diagrams>



Note: PA3 and PA4 are removed for SOP-24 package.

<Figure-3: SOP-24 Pin assignment diagrams>

PIN Description

Name	In/Out	Pin Description	Shared Function
PA.0–PA.4	I/O	Bit-programmable I/O port for Schmitt-trigger input or push-pull output and pseudo-open-drain selectable.	INT / PWM / IR Carrier IN/OUT
PB.0–PB.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or push-pull output.	INT
PD.0–PD.7	I/O	Bit-programmable I/O port for Schmitt-trigger input or pseudo-open-drain output.	
X_{IN}, X_{OUT}	–	Crystal / Ceramic, or RC oscillator signal for system clock.	
V_{DD}, V_{SS}	P	Voltage input pin and ground	–
VPP / RSTn	I	Reset pin or OTP program power	

< I: Input; O: Output; I/O: Bi-direction; P: Power >

Instruction Set

Field	Description
f	Register File Address
b	Bit address
k	Literal. Constant data or label
d	Destination selection field. 0: Working register; 1: Register file
W	Working Register
Z	Zero Flag
C	Carry Flag
DC	Decimal Carry Flag
PC	Program Counter
TOS	Top Of Stack
GIE	Global Interrupt Enable Flag (i-Flag)
( )	Contents
.	Bit Field
←	Assign direction

Mnemonic		Op Code	Cycles	Flag Affect	Description
Byte-Oriented File Register Instruction					
ADDWF	f,d	00 0111 dfff ffff	1	C,DC,Z	Add W and "f"
ANDWF	f,d	00 0101 dfff ffff	1	Z	AND W with "f"
CLRF	f	00 0001 1fff ffff	1	Z	Clear "f"
CLRW		00 0001 0100 0000	1	Z	Clear W
COMF	f,d	00 1001 dfff ffff	1	Z	Complement "f"
DECF	f,d	00 0011 dfff ffff	1	Z	Decrement "f"
DECFSZ	f,d	00 1011 dfff ffff	1 or 2	-	Decrement "f", skip if zero
INCF	f,d	00 1010 dfff ffff	1	Z	Increment "f"
INCFSZ	f,d	00 1111 dfff ffff	1 or 2	-	Increment "f", skip if zero
IORWF	f,d	00 0100 dfff ffff	1	Z	OR W with "f"
MOVFW	f	00 1000 0fff ffff	1	-	Move "f" to "w"
MOVWF	f	00 0000 1fff ffff	1	-	Move W to "f"
MOVWR	r	00 0000 00rr rrrr	1	-	Move W to "r"
RLF	f,d	00 1101 dfff ffff	1	C	Rotate left "f" through carry
RRF	f,d	00 1100 dfff ffff	1	C	Rotate right "f" through carry
SUBWF	f,d	00 0010 dfff ffff	1	C,DC,Z	Subtract W from "f"
SWAPF	f,d	00 1110 dfff ffff	1	-	Swap high/low nibble of "f"
TESTZ	f	00 1000 1fff ffff	1	Z	Test if "f" is zero
XORWF	f,d	00 0110 dfff ffff	1	Z	XOR W with "f"
Bit-Oriented File Register Instruction					
BCF	f,b	01 000b bbff ffff	1	-	Clear "b" bit of "f"
BSF	f,b	01 001b bbff ffff	1	-	Set "b" bit of "f"
BTFSC	f,b	01 010b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTFSS	f,b	01 011b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if set
Literal and Control Instruction					
ADDLW	k	01 1100 kkkk kkkk	1	C,DC,Z	Add Literal "k" to W
ANDLW	k	01 1011 kkkk kkkk	1	Z	AND Literal "k" with W
CALL	k	10 kkkk kkkk kkkk	2	-	Call subroutine "k"
CLRWDT		00 0000 0000 0100	1	-	Clear and enable Watch Dog Timer
GOTO	k	11 kkkk kkkk kkkk	2	-	Jump to branch "k"
IORLW	k	01 1010 kkkk kkkk	1	Z	OR Literal "k" with W
MOVLW	k	01 1001 kkkk kkkk	1	-	Move Literal "k" to W
NOP		00 0000 0000 0000	1	-	No operation
RET		00 0000 0100 0000	2	-	Return
RETI		00 0000 0110 0000	2	-	Return from interrupt
RETLW	k	01 1000 kkkk kkkk	2	-	Return, place Literal "k" in W
SLEEP		00 0000 0000 0011	1	-	Go into standby mode, Clock oscillation stops
XORLW	k	01 1111 kkkk kkkk	1	Z	XOR Literal "k" with W

Memory MAP

F-Plane

Name	Address	R/W	Reset	Description
INDF	00.7~0	R/W	0	Indirect Register (1)
TIMER0	01.7~0	R/W	0	Timer 0
PC	02.7~0	R/W	0	Program Counter [7~0]
RAMBANK	03.4	R/W	0	SRAM Bank Select
ZFLAG	03.2	R/W	0	Zero Flag
DCFLAG	03.1	R/W	0	Decimal Carry Flag
CFLAG	03.0	R/W	0	Carry Flag
FSR	04.6~0	R/W	0	File Select Register
PAD	05.2~0	R/W	ff	Port A output data latch / pin
PBD	06.7~0	R/W	ff	Port B output data latch / pin
PDD	07.7~0	R/W	ff	Port D output data latch / pin
WKTI	0A.2	R/W	0	Wake-up timer (64ms) Interrupt flag, write 0 to clear flag.
PA0I	0A.1	R/W	0	PA[0] falling edge interrupt, write 0 to clear flag.
TM0I	0A.0	R/W	0	Timer0 Interrupt flag, write 0 to clear flag.
PBINT	0B.7~0	R/W	0	Port B falling edge interrupt flag, write "0" to clear.
PWMCON	0C.7~0	R/W	0	PWM Control Register. “Bit 0=” 1: Enable; 0: Disable
PWMDTY	0D.7~0	R/W	0	PWM Duty.
IRCON.IREN	0E.0	R/W	0	1: IR Carrier output; 0: IR Carrier not output
IRCON.START	0E.1	R/W	0	1: Start IR Learn Mode; 0: Turn-off IR Learn Mode and clear PRDREGH, PRDREGL, DUTYREGH, and DUTYREGL.
IRCON.AMS	0E.2	R/W	0	IR Auto/Manual Select. 1: IR Auto Mode; 0: IR Manual Mode
IRPRDH	0F.2~0	R/W	0	IR Carrier Period High (manual setting)
IRPRDL	10.7~0	R/W	0	IR Carrier Period Low (manual setting)
IRDUTYH	11.2~0	R/W	0	IR Carrier Duty (manual setting)
IRDUTYL	12.7~0	R/W	0	IR Carrier Duty (manual setting)
PRDREGH	13.2~0	R	0	IR Carrier Period High (automatically setting)
PRDREGL	14.7~0	R	fa	IR Carrier Period Low (automatically setting)
DUTYREGH	15.2~0	R	0	IR Carrier Duty (automatically setting)
DUTYREGL	16.7~0	R	7d	IR Carrier Duty (automatically setting)
	17 ~ 1F	-	-	Reserved. DO NOT use this area.
SRAM	30~7F	R/W	-	Internal RAM (176 Bytes), (7Fh-30h+1)*2 + 10h

Note-1: The INDF Register is not a physical register. Addressing INDF actually addresses the register whose address is contained in the FSR register. This is so called indirect addressing.

WARNING: The register addresses not in the table are all reserved. Writing or reading these undefined registers may cause the system to be unstable.

R-Plane

Name	Address	R/W	Reset	Description
RELOAD	01.7~0	W	0	Timer0 overflow reload value
PSCL	02.3~0	W	0	Timer0 Pre-Scale, 0: div1, 7: div128, 8: div256 instruction cycle
PWRDOWN	03	W	0	write this register to enter Power-Down Mode
WDTE	04	W	0	write this register to clear WDT and enable WDT
PAPPE	05.2~0	W	0	Port A Push-Pull Enable
PBE	06.7~0	W	0	Port B output enable
WKTIE	0A.2	W	0	WKTI Interrupt enable
PA0IE	0A.1	W	0	PA[0] Interrupt enable
TM0IE	0A.0	W	0	Timer0 Interrupt enable
PBINTE	0B.7~0	W	0	Port B falling interrupt enable
PBPUE	0D.7~0	W	0	Port B pull-high enable. 1: Enable; 0: Disable
	0E ~ 3F	-	-	Reserved. DO NOT use this area.

Electrical Characteristics

- **Absolute Maximum Ratings (T_A = 25°C)**

Parameter	Rating	Unit
Supply voltage	–0.3 to +5.5	V
Input voltage	–0.3 to V_{DD} +0.3	
Output voltage	–0.3 to V_{DD} +0.3	
Maximum Operating Voltage	5.5	V
Operating temperature	–20 to +70	°C
Storage temperature	–25 to +125	

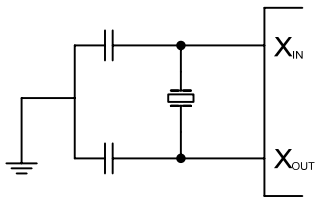
- **DC Characteristics (T_A = 25°C, V_{DD} = 2.2V to 5.5V)**

Parameter	Symbol	Conditions		Min	Type	Max	Unit
Input High Voltage	V_{IH1}	Except X_{IN} , X_{OUT}	V_{DD} = 2.2 to 5.5 V	0.8 V_{DD}	–	V_{DD}	V
	V_{IH2}	X_{IN} , X_{OUT}		V_{DD} - 0.1			
Input Low Voltage	V_{IL1}	Except X_{IN} , X_{OUT}	V_{DD} = 2.2 to 5.5 V	–	–	0.2 V_{DD}	V
	V_{IL2}	X_{IN} , X_{OUT}				0.1	
Output High Voltage	V_{OH1}	Push-Pull when I_{OH}= -6.0 mA	V_{DD} = 4.5 to 5.5 V	–	V_{DD} - 0.4	–	V
	V_{OH2}	Pseudo-open-drain when I_{OH}= -15uA	V_{DD} = 4.5 to 5.5 V	–	V_{DD} - 0.4	–	V
Output Low Voltage	V_{OL}	I_{OL}=15mA	V_{DD} = 4.5 to 5.5 V		0.4		V
Input Leakage Current (pin high)	I_{ILH}	Except X_{IN} , X_{OUT}	V_{IN} = V_{DD}	–	–	1	uA
		X_{IN} , X_{OUT}	V_{IN} = V_{DD}				
Input Leakage Current (pin low)	I_{ILL}	Except X_{IN} , X_{OUT}	V_{IN} = 0 V	–	–	–1	uA
		X_{IN} , X_{OUT}	V_{IN} = 0 V				
Standby Current	I_{SB}		V_{DD} = 5V			<1	uA
Power Supply Current	I_{DD}	Run 10 MHz	V_{DD} = 4.5 to 5.5 V	–		7	mA
		Run 4 MHz	V_{DD} = 2.2 V			1	

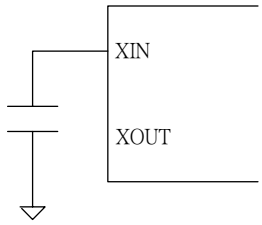
- **Clock Timing Constants (T_A = –20°C to +70°C)**

Oscillator	Condition	Min	Type	Max	Unit
XTAL	VDD = 2.5 to 5.5 V	1		16	MHz
RC(note-1)	VDD = 4.75 to 5.25 V		4		

Note:
1. Tolerance: ±20 % at TA = 25°C



External Oscillator Circuit (Crystal or Ceramic)



External C Oscillator

External C Reference Frequency Table: **Unit: Hz**

	VDD=3V	VDD=5V
22pF	962K	1.23M
12pF	1.43M	1.77M
4pF	2.53M	3.09M
1pF	3.53M	4.27M

System Configuration Fuse Definition:

- Bit[3] : Not used.

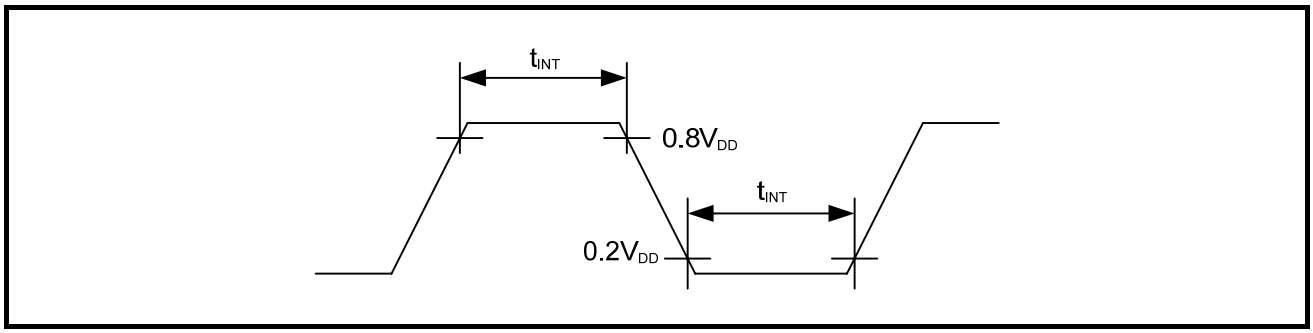
- Bit[2] : LVREN. (Low Voltage Reset Enable)
  1: Enable; 0: Disable
  Note: Disable LVREN and also disable Power-On Reset.

- Bit[1] : OSC Mode
  1: XTAL; 0: External C

- Bit[0] : Protection
  1: Not protect; 0: Protect

- **External Interrupt Characteristics (T_A = –20°C to +70°C, V_{DD} = 2.2V to 5.5V)**

Parameter	Conditions	Min	Typ	Max	Unit
Input High Voltage	–	0.8 V_{DD}	–	V_{DD}	V
Input Low Voltage	–	–	–	0.2 V_{DD}	V
External Interrupt Input Width(t_{INT})	V_{DD} = 5 V ± 10 %	–	200	–	ns



- **Reset Timing Characteristics (T_A = –20°C to +70°C, V_{DD} = 2.2V to 5.5V)**

Parameter	Conditions	Min.	Type	Max.	Unit
Input High Voltage	–	0.8 V_{DD}	–	V_{DD}	V
Input Low Voltage	–	–	–	0.2 V_{DD}	V
RESET Input Low Width	Input V_{DD} = 5 V ± 10 %	–	1	–	μs
Oscillation stabilization time	f_{OSC} = 1 ~ 12 MHz	2.4	–	6.1	ms

- **LVR Circuit Characteristics (T_A = 25°C, V_{DD} = 2.2V to 5.5V)**

Parameter	Symbol	Min.	Type	Max.	Unit
LVR reference Voltage	V_{LVR}	–	-	2.2	V

Package Information: The order information is “IC Type” “XX” “YY” “C” “Z”

1. “IC TYPE”: TM57PR40

2. “XX”: Package Type

- SOP Code: S

3. “YY”: IC Pin Number

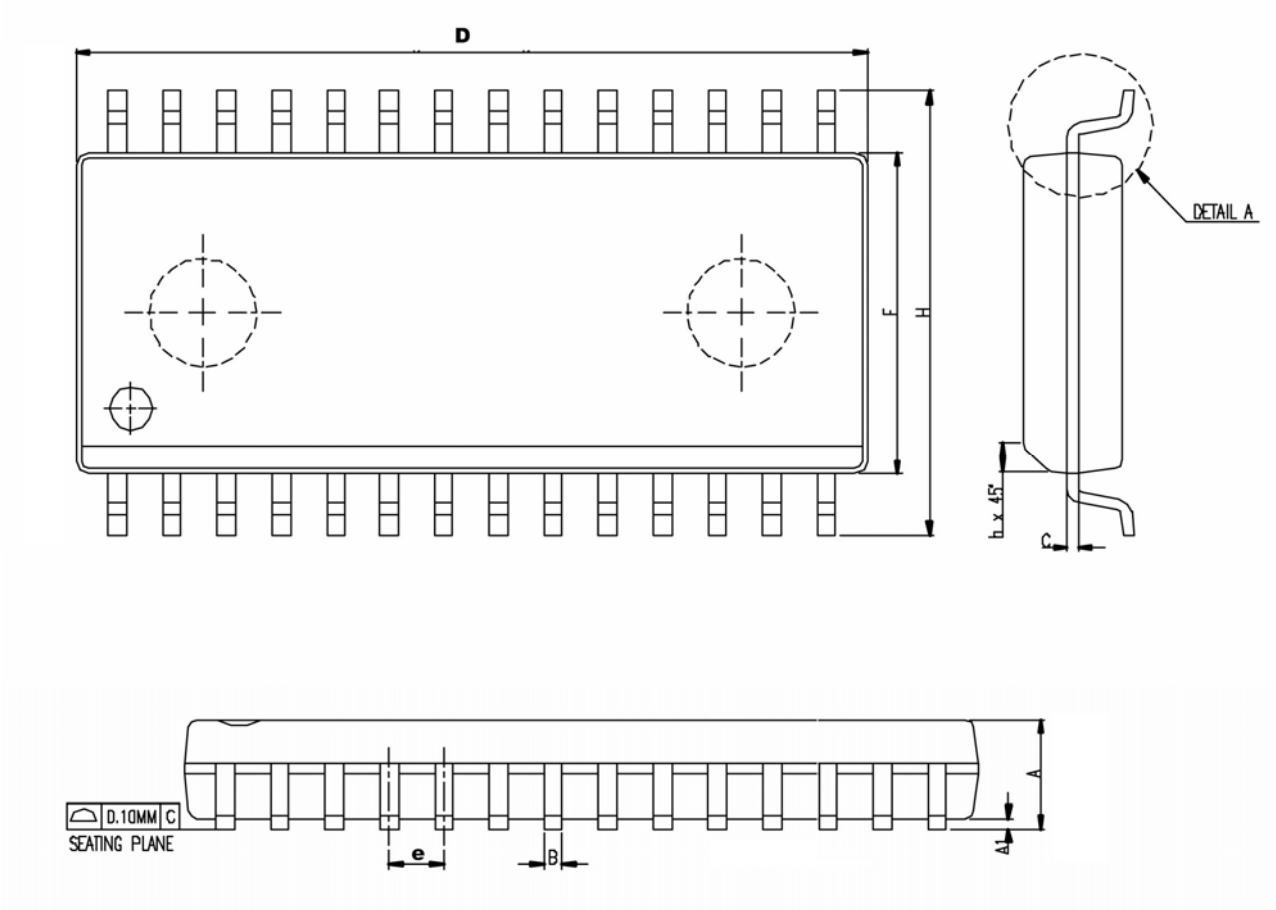
- Pin Number: 28 Code: 28
- Pin Number: 24 Code: 24

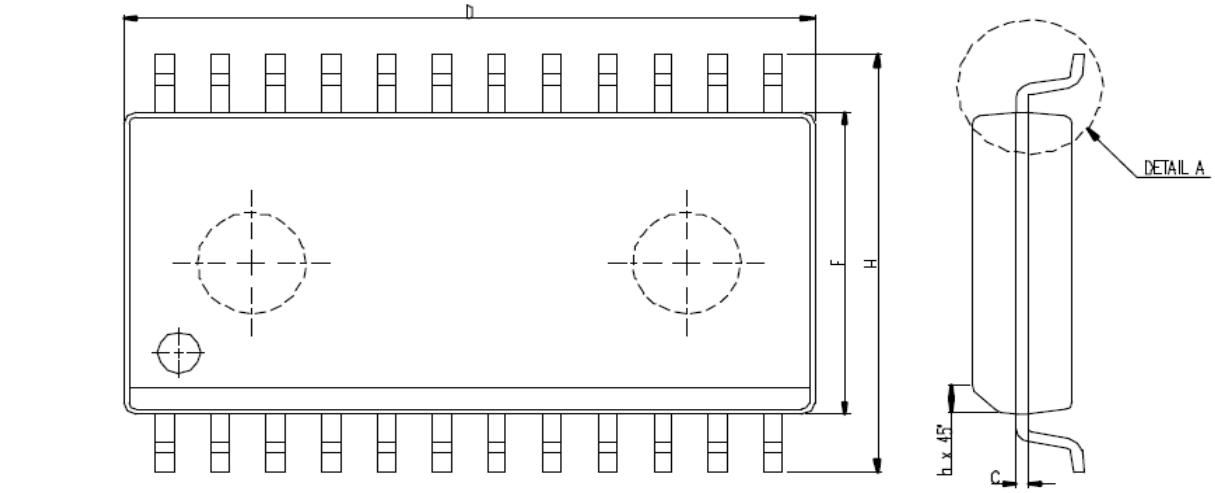
4. “C”: Reserve (Must write be “C”)

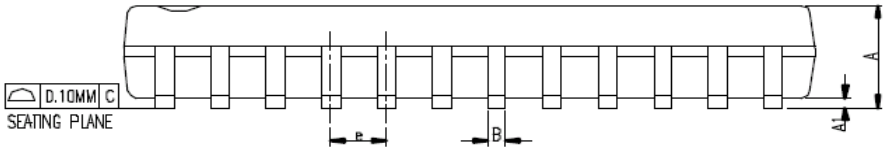
5. “Z”: Package material

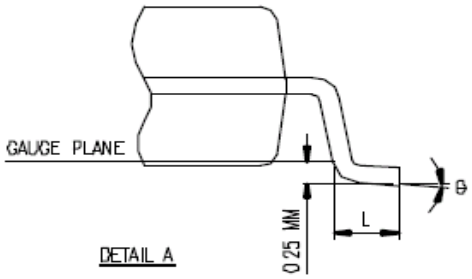
- Package material: Pb-free Code: W
- Package material: Green Package Code: G

Package Dimension









DETAIL A

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.0926	0.1043
A1	0.10	0.30	0.0040	0.0118
B	0.33	0.51	0.013	0.020
C	0.23	0.32	0.0091	0.0125
e	1.27 BSC		0.050 BSC	
E	7.40	7.60	0.2914	0.2992
H	10.00	10.65	0.394	0.419
L	0.40	1.27	0.016	0.050
h	0.25	0.75	0.010	0.029
θ	0°	8°	0°	8°

	D DIMENSION (IN MM)		D DIMENSION (IN INCH)		
N	MIN.	MAX.	MIN.	MAX.	JEDEC
20	12.60	13.00	0.4961	0.5118	MS-013 (AC)
24	15.20	15.60	0.5985	0.6141	MS-013 (AD)
28	17.70	18.10	0.6969	0.7125	MS-013 (AE)