



十速科技股份有限公司  
tenx technology inc.

**Advance  
Information**

---

# TM8721

# Data Sheet

**Tenx reserves the right to change or  
discontinue this product without notice.**

**tenx technology inc.**

---

**FUNCTION****1. Powerful instruction set (137 instructions)**

- Binary addition, subtraction, BCD adjust, logical operation in direct and index addressing mode.
- Single-bit manipulation. (set, reset, decision for branch)
- Various conditional branch.
- 16 working registers and manipulation.
- Look-up table.
- LCD driver data transfer.

**2. Memory capacity**

- ROM capacity                   1024 x 16 bits.
- RAM capacity                    64 x 4 bits.

**3. Input/output ports**

- Port IOA4                   1 pin (with internal pull-low).  
IOA4 port had built in the input signal chattering prevention circuitry.
- Port IOC                    4 pins (with internal pull-low, low-level-hold).
- Port IOB3,4                2 pins (with internal pull-low), & mask option with BZB, BZ.

**4. 8 level subroutine nesting.****5. Interrupt function**

- External factor    1       (Pin IOA4 port).
- Internal factors    3       (Pre-Divider, Timer2 & RFC).

**6. Built in Alarm, clock or single tone melody generator (BZB, BZ), & mask option with IOB3, 4.****7. Built-in R to F Converter circuit**

- CX, RR, RT.

**8. One 6-bit programmable timer (Timer 2) with programmable clock source.****9. LCD driver output**

- 9 LCD driver outputs. (Up to drive 36 LCD segments)
- 1/4 Duty and 1/2 Bias for LCD display.
- Single instruction to turn off all segments.
- 9 DC/Open Drain outputs for LED mask option.
- 16 LCD Address.

**10. Built-in Voltage double charge pump circuit.****11. Clock oscillation can be defined as X'tal, external-R or internal-R 2 type oscillator by mask option.****12. HALT function.****13. STOP function.**

## APPLICATION

- Thermometer, Timer

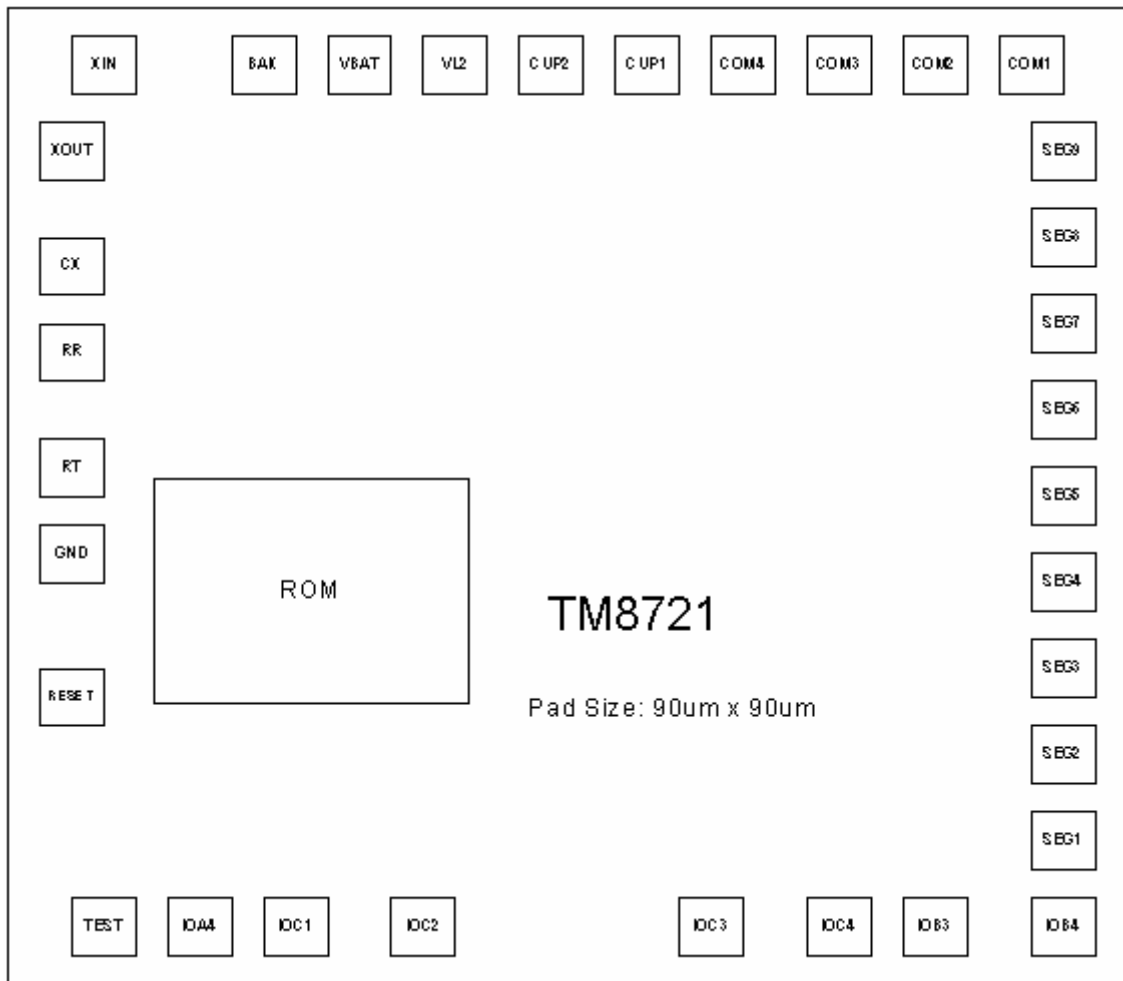
## PIN DESCRIPTION

Name	I/O	Description
VBAT	P	Positive power supply. Connect a 0.1uF capacitor to GND.
BAK(VL1)	P	Internal logic, RFC & LCD mode level1 supply voltage Connected to VBAT.
VL2	P	LCD mode level2 supply voltage. Connect a 0.1uF capacitor to GND for LCD mode. Short to VBAT for LED Mode.
RESET	I	Input pin for chip reset request signal, with internal pull-down resistor.
TEST	I	Test signal input pin.
CUP1,2	O	Switching pins for supply the LCD driving voltage. Connect the CUP1 and CUP2 pins with a 0.1uf non-polarized electrolytic capacitor for LCD mode.
COM1~4	O	Output pins for driving the common pins of the LCD panel.
SEG1~9	O	Output pins for driving the LCD panel segment.
IOA4	I/O	I/O port pin.
IOB3,4	I/O	I/O port pins, & mask option with BZB, BZ
IOC1~4	I/O	I/O port pins
CX RR, RT	I O	1 input pin and 2 output pins for RFC application.
BZB, BZ	O	Output port for alarm, frequency or melody generator
XIN XOUT	I O	System clock oscillation. Connected with 32KHz crystal oscillator or internal R or external R by mask option.
GND	P	Negative supply voltage.

## PAD COORDINATE

No	Name	X	Y	No	Name	X	Y
1	VL2	563.50	1267.50	18	IOB4/BZ	1317.40	87.25
2	VBAT	438.50	1267.50	19	SEG1	1327.50	222.50
3	BAK (VL1)	323.50	1267.50	20	SEG2	1327.50	337.50
4	XIN	120.40	1267.50	21	SEG3	1327.50	452.50
5	XOUT	87.50	1119.20	22	SEG4	1327.50	567.50
6	CX	87.50	979.00	23	SEG5	1327.50	682.50
7	RR	87.50	864.00	24	SEG8	1327.50	797.50
8	RT	87.50	700.50	25	SEG7	1327.50	912.50
9	GND	87.50	585.50	26	SEG8	1327.50	1027.50
10	RESET	87.50	330.05	27	SEG9	1327.50	1142.50
11	TEST	115.00	87.25	28	COM1	1253.50	1267.50
12	IOA4	260.00	87.25	29	COM2	1138.50	1267.50
13	IOC1	375.00	87.25	30	COM3	1023.50	1267.50
14	IOC2	530.90	87.25	31	COM4	908.50	1267.50
15	IOC3	890.60	87.25	32	CUP1	793.50	1267.50
16	IOC4	1046.50	87.25	33	CUP2	678.50	1267.50
17	IOB3/BZB	1161.50	87.25				

**PAD DIAGRAM**



The substrate of chip should be connected to GND.

**FUNCTION DESCRIPTION**

**SRAM**

There are 64 X 4 bits data SRAM(40h ~ 7Fh), can be used by direct addressing mode or index addressing mode; the last 16 address(70h ~ 7Fh) can be used as Working Register.

**ROM**

There are 1024 X 16 bits ROM, can be used to divide it for Instruction ROM and Index ROM by mask option. The capacity of Instruction ROM is 128N x 16bits, and the capacity of Index ROM is 256(8-N) x 8bits (N=1 to 8).

The Index ROM can be used as 4-bits or 8-bits mode.

**I/O Ports**

The IOC port can be selected by software separately as input or output and with/without internal pull-low.

The IOB3,4 port can be selected by software separately as input or output and with/without internal pull-low.

The IOA4 port can be selected by software as input or output and with/without internal pull-low and different chattering clock for HALT release /Interrupt trigger to reduce the bounce of key scan:

PH6 : 512Hz PH8 : 128Hz PH10 : 32Hz

The pull-low of IOA4 will be masked off for those pins that were defined as output pins. During developing, the IOA3~1 must be set to output. The initial state of all I/O Ports are all standard Input state and with internal pull-low resistor. Before set some pins from input to output, you can execute output function to ensure their output value.

**Reset**

Reset Pin Reset function. There is no individual “Power On Reset” option because “RESET pin reset” is the only way to start up the program. When the ‘H’ level signal applied on the RESET pin, the reset cycle will finished after 64ms automatically, even though the reset signal is longer than 64ms.

**Pre-Divider**

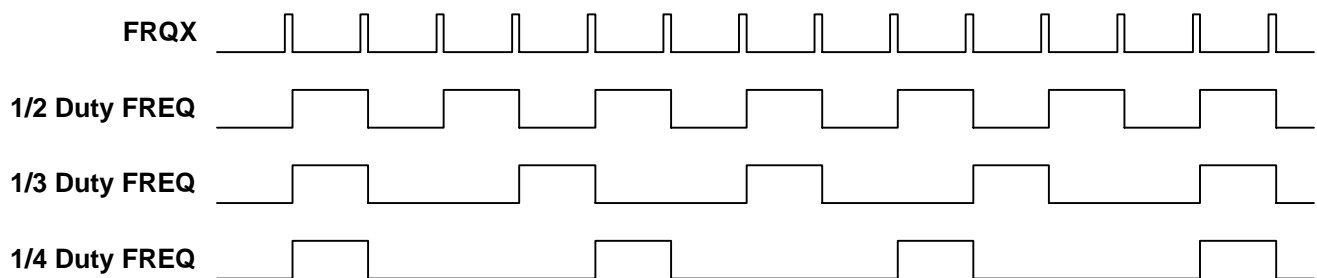
The pre-divider contains a 15-stage counter using PH0 as clock source; the output of T-Flip-Flop is changed when input clock changes from H to L. PH11~15 will be reset to L state when power on reset or external reset pin reset or PLC 100 instruction is executed. When PH14 changed from H to L, the HALT release signal HRF3 is generated.

**TIMER 2**

This 6 bits programmable timer can select PH3 / PH9 / PH15 / FREQ (Timer 2 can also select PH5 / PH7 / PH11 / PH13 by TM2X instruction) as clock source; when it is underflow, the HALT release signal HRF1/4 is generated.

**Alarm / Frequency / Melody**

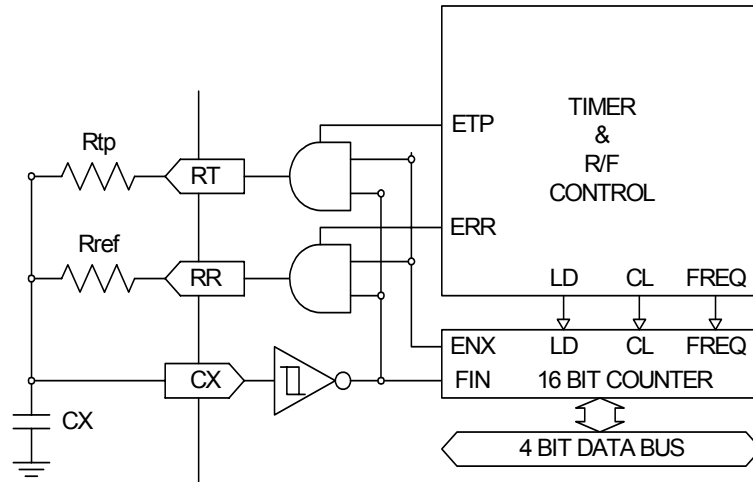
There is an 8 bits programmable counter used as Frequency generator, and a 2-bit control for 1/1, 1/2, 1/3 or 1/4 duty selection.



There is another 8 bits envelope control for Alarm, Frequency or Melody output from BZ/BZB.

**Resistor to Frequency Converter**

There is a Resistor to Frequency Converter; it contains a RC oscillation circuit and a 16 bits counter to calculate relative resistance of temperature or humidity sensor with the reference resister.



There are two kinds of methodology for measuring the input frequency; first, set CX as clock input and using Timer 2 as interval control, or use software direct control the time interval; second, if the CX frequency is too low, either a poor resolution for a fixed interval, or a long period for better resolution but a longer read-out rate, for example, 10 seconds per read-out, in such condition, you can switch the measuring mode to be setting the CX as interval control, it will enable the counter from the first CX rising edge till next rising edge, then generate a HALT release signal HRF6, and using FREQ (internal frequency generator output) as clock input, hence you can count the interval of CX.

For measuring the resistance of Temperature or Humidity sensor, first we measure the frequency of There is a Resistor to Frequency Converter, it contains a RC oscillation circuit and a 16 bits counter to calculate relative resistance of temperature and humidity sensor with the reference resister.

**HALT Function**

The HALT instruction will disable the system clock and leave only pre-divider, frequency generator, timer and chattering clock for HALT release generation.

**STOP Function**

The STOP instruction will disable all clocks to minimize the stand-by current ( < 1uA ).

**ABSOLUTE MAXIMUM RATINGS**

at Ta = -20°C to 70°C, GND = 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VBAT	-0.3 to 3.6	V
	BAK	-0.3 to 3.6	V
	VL2	-0.3 to 3.6	V
Maximum Input Voltage	Vin	-0.3 to VBAT+0.3	V
Maximum output Voltage	Vout1	-0.3 to BAK+0.3	V
	Vout2	-0.3 to VL2 +0.3	V
Maximum Operating Temperature	Topg	-20 to +70	°C
Maximum Storage Temperature	Tstg	-25 to +125	°C

**ALLOWABLE OPERATING CONDITIONS**

at Ta = -20°C to 70°C, GND = 0V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VBAT	Connected BAK to VBAT	1.2	1.5	1.8	V
	VL2		2xBAKx0.9		2xBAK + 0.1	V
Input "H" Voltage	Vih1	IOC and IOD port in input mode	VBAT-0.7	-	VBAT+0.7	V
Input "L" Voltage	Vil1		-0.7	-	0.7	V

**ALLOWABLE OPERATING FREQUENCY**

at Ta = -20°C to 70°C, GND = 0V

Condition	Max, Operating Frequency
BAK=1.5V	800KHz

**ELECTRICAL CHARACTERISTICS INTERNAL RC FREQUENCY RANGE**

Option Mode	BAK	Min.	Typical	Max.
350KHz	1.5V		350KHz	
650KHz			650KHz	

**Input Resistance**

VBAT = 1.5V

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
"L" Level Hold Tr.(IOC1~4)	Rllh1	Vi = 0.2VBAT	10	40	70	Kohm
IOA4, IOB3~4, IOC1~4 Pull-Down Tr.	Rmad1	Vi = VBAT	200	500	1100	Kohm
RES Pull-Down R	Rres1	Vi = GND or VBAT	50	70	100	Kohm

**DC Output Characteristics**

(VL2 = 1.2V)

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1c	For LED option, loh = -1mA	SEG1~9	0.75	0.9	-	V
Output "L" Voltage	Vol1c	For LED option, lol = 5mA		-	0.3	0.45	V
Output "H" Voltage	Voh2c	loh = -1mA	IOA4, IOC1~4, IOB3,4/ BZB, BZ	0.75	0.9		V
Output "L" Voltage	Vol2c	lol = 2mA			0.3	0.45	V

**(VBAK = 1.5V)**

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh3c	Ioh = -200uA	RR, RT		1.125		V
Output "L" Voltage	Vol3c	Iol = 400uA			0.375		V

**Segment Driver Output Characteristics**

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
1/2 Bias Display Mode							
Output "H" Voltage	Voh12f	Ioh = -1uA	SEG-n	2.5			V
Output "L" Voltage	Vol12f	Iol = 1uA				0.2	V
Output "H" Voltage	Voh12g	Ioh = -10uA	COM-n	2.5			V
Output "M" Voltage	Vom12g	Iol/h = +/-10uA	COM-n	1.05		1.55	V
Output "L" Voltage	Vol12g	Iol = 10uA				0.2	V

**POWER CONSUMPTION****@ Ta = -20°C to 70°C, GND = 0V, VBAT = 1.5V**

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT	Only 32.768KHz Crystal oscillator operating, without loading.		2		uA
STOP mode	ISTOP				1	uA
Operating current	Iop1	RFC operating *	20	45	60	uA

\* Rtp and Rref = 30KΩ, Cx = 0.001uF

**Note:** When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

## INSTRUCTION TABLE

Instruction	Machine Code	Function	Flag/Remark
NOP	0000 0000 0000 0000	No Operation	
LCT	Lz,Ry 0000 0010 ZZZZ YYYY	Lz ← (7SEG ← Ry)	
LCB	Lz,Ry 0000 0100 ZZZZ YYYY	Lz ← (7SEG ← Ry)	Blank Zero
LCP	Lz,Ry 0000 0110 ZZZZ YYYY	Lz ← Ry & AC	
LCD	Lz,@HL 0000 1000 ZZZZ 0000	Lz ← T@HL	
LCT	Lz,@HL 0000 1000 ZZZZ 0001	Lz ← (7SEG ← @HL)	
LCB	Lz,@HL 0000 1000 ZZZZ 0010	Lz ← (7SEG ← @HL)	Blank Zero
LCP	Lz,@HL 0000 1000 ZZZZ 0011	Lz ← @HL & AC	
OPA	Rx 0000 1010 01XX XXXX	PortA(IOA4) ← Rx	Rx: 40~7Fh
OPB	Rx 0000 1100 01XX XXXX	PortB(IOB) ← Rx	Rx: 40~7Fh
OPC	Rx 0000 1101 01XX XXXX	PortC(IOC) ← Rx	Rx: 40~7Fh
FRQ	D,Rx 0001 00DD 01XX XXXX	FREQ ← Rx & AC D=00 : 1/4 Duty D=01 : 1/3 Duty D=10 : 1/2 Duty D=11 : 1/1 Duty	Rx: 40~7Fh
FRQ	D,@HL 0001 01DD 0000 0000	FREQ ← T@HL	
FRQX	D,X 0001 10DD XXXX XXXX	FREQ ← X	
MVL	Rx 0001 1100 01XX XXXX	@L ← Rx	Rx: 40~7Fh
MVH	Rx 0001 1101 01XX XXXX	@H ← Rx & AC	Rx: 40~7Fh
ADC	Rx 0010 0000 01XX XXXX	AC ← Rx + AC + CF	CF, Rx: 40~7Fh
ADC	@HL 0010 0000 1000 0000	AC ← @HL + AC + CF	CF
ADC*	Rx 0010 0001 01XX XXXX	AC,Rx ← Rx + AC + CF	CF, Rx: 40~7Fh
ADC*	@HL 0010 0001 1000 0000	AC,@HL ← @HL + AC + CF	CF
SBC	Rx 0010 0010 01XX XXXX	AC ← Rx + ACB + CF	CF, Rx: 40~7Fh
SBC	@HL 0010 0010 1000 0000	AC ← @HL + ACB + CF	CF
SBC*	Rx 0010 0011 01XX XXXX	AC,Rx ← Rx + ACB + CF	CF, Rx: 40~7Fh
SBC*	@HL 0010 0011 1000 0000	AC,@HL ← @HL + ACB + CF	CF
ADD	Rx 0010 0100 01XX XXXX	AC ← Rx + AC	CF, Rx: 40~7Fh
ADD	@HL 0010 0100 1000 0000	AC ← @HL + AC	CF
ADD*	Rx 0010 0101 01XX XXXX	AC,Rx ← Rx + AC	CF, Rx: 40~7Fh
ADD*	@HL 0010 0101 1000 0000	AC,@HL ← @HL + AC	CF
SUB	Rx 0010 0110 01XX XXXX	AC ← Rx + ACB + 1	CF, Rx: 40~7Fh
SUB	@HL 0010 0110 1000 0000	AC ← @HL + ACB + 1	CF
SUB*	Rx 0010 0111 01XX XXXX	AC,Rx ← Rx + ACB + 1	CF, Rx: 40~7Fh
SUB*	@HL 0010 0111 1000 0000	AC,@HL ← @HL + ACB + 1	CF
ADN	Rx 0010 1000 01XX XXXX	AC ← Rx + AC	Rx: 40~7Fh
ADN	@HL 0010 1000 1000 0000	AC ← @HL + AC	
ADN*	Rx 0010 1001 01XX XXXX	AC,Rx ← Rx + AC	Rx: 40~7Fh
ADN*	@HL 0010 1001 1000 0000	AC,@HL ← @HL + AC	
AND	Rx 0010 1010 01XX XXXX	AC ← Rx AND AC	Rx: 40~7Fh
AND	@HL 0010 1010 1000 0000	AC ← @HL AND AC	
AND*	Rx 0010 1011 01XX XXXX	AC,Rx ← Rx AND AC	Rx: 40~7Fh
AND*	@HL 0010 1011 1000 0000	AC,@HL ← @HL AND AC	
EOR	Rx 0010 1100 01XX XXXX	AC ← Rx EOR AC	Rx: 40~7Fh
EOR	@HL 0010 1100 1000 0000	AC ← @HL EOR AC	
EOR*	Rx 0010 1101 01XX XXXX	AC,Rx ← Rx EOR AC	Rx: 40~7Fh
EOR*	@HL 0010 1101 1000 0000	AC,@HL ← @HL EOR AC	
OR	Rx 0010 1110 01XX XXXX	AC ← Rx OR AC	Rx: 40~7Fh
OR	@HL 0010 1110 1000 0000	AC ← @HL OR AC	
OR*	Rx 0010 1111 01XX XXXX	AC,Rx ← Rx OR AC	Rx: 40~7Fh
OR*	@HL 0010 1111 1000 0000	AC,@HL ← @HL OR AC	
ADCI	Ry,D 0011 0000 DDDD YYYY	AC ← Ry + D + CF	CF

Instruction		Machine Code		Function	Flag/Remark
ADCI*	Ry,D	0011 0001 DDDD YYYY	AC,Ry	$\leftarrow Ry + D + CF$	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	AC	$\leftarrow Ry + DB + CF$	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	AC,Ry	$\leftarrow Ry + DB + CF$	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	AC	$\leftarrow Ry + D$	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	AC,Ry	$\leftarrow Ry + D$	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	AC	$\leftarrow Ry + DB + 1$	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	AC,Ry	$\leftarrow Ry + DB + 1$	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	AC	$\leftarrow Ry + D$	
ADNI*	Ry,D	0011 1001 DDDD YYYY	AC,Ry	$\leftarrow Ry + D$	
ANDI	Ry,D	0011 1010 DDDD YYYY	AC	$\leftarrow Ry \text{ AND } D$	
ANDI*	Ry,D	0011 1011 DDDD YYYY	AC,Ry	$\leftarrow Ry \text{ AND } D$	
EORI	Ry,D	0011 1100 DDDD YYYY	AC	$\leftarrow Ry \text{ EOR } D$	
EORI*	Ry,D	0011 1101 DDDD YYYY	AC,Ry	$\leftarrow Ry \text{ EOR } D$	
ORI	Ry,D	0011 1110 DDDD YYYY	AC	$\leftarrow Ry \text{ OR } D$	
ORI*	Ry,D	0011 1111 DDDD YYYY	AC,Ry	$\leftarrow Ry \text{ OR } D$	
INC*	Rx	0100 0000 01XX XXXX	AC,Rx	$\leftarrow Rx + 1$	CF, Rx: 40~7Fh
INC*	@HL	0100 0000 1000 0000	AC,@HL	$\leftarrow @HL + 1$	CF
DEC*	Rx	0100 0001 01XX XXXX	AC,Rx	$\leftarrow Rx - 1$	CF, Rx: 40~7Fh
DEC*	@HL	0100 0001 1000 0000	AC,@HL	$\leftarrow @HL - 1$	CF
IPA	Rx	0100 0010 01XX XXXX	AC,Rx	$\leftarrow \text{PortA(IOA4)}$	Rx: 40~7Fh
IPB	Rx	0100 0100 01XX XXXX	AC,Rx	$\leftarrow \text{PortB(IOB4,3)}$	Rx: 40~7Fh
IPC	Rx	0100 0111 01XX XXXX	AC,Rx	$\leftarrow \text{PortC(IOC4~1)}$	Rx: 40~7Fh
MAF	Rx	0100 1010 01XX XXXX	AC,Rx	$\leftarrow \text{STS1}$	B3 : CF B2 : ZERO B1 :(Unused) B0 :(Unused) Rx: 40~7Fh
MSB	Rx	0100 1011 01XX XXXX	AC,Rx	$\leftarrow \text{STS2}$	B3 : (Unused) B2 : SCF2(HRx) B1, B0: (Unused) Rx: 40~7Fh
MSC	Rx	0100 1100 01XX XXXX	AC,Rx	$\leftarrow \text{STS3}$	B3 : SCF7(PDV) B2 : PH15 B1, B0: (Unused) Rx: 40~7Fh
MCX	Rx	0100 1101 01XX XXXX	AC,Rx	$\leftarrow \text{STS3X}$	B3 : SCF9(RFC) B2 : SCF0(APT) B1 : SCF6(TM2) B0 : (Unused) Rx: 40~7Fh
MSD	Rx	0100 1110 01XX XXXX	AC,Rx	$\leftarrow \text{STS4}$	B3 : (Unused) B2 : RFOVF B1, B0: (Unused) Rx: 40~7Fh
SR0	Rx	0101 0000 01XX XXXX	ACn, Rxn AC3, Rx3	$\leftarrow Rx(n+1)$ $\leftarrow 0$	Rx: 40~7Fh
SR1	Rx	0101 0001 01XX XXXX	ACn, Rxn AC3, Rx3	$\leftarrow Rx(n+1)$ $\leftarrow 1$	Rx: 40~7Fh
SL0	Rx	0101 0010 01XX XXXX	ACn, Rxn AC0, Rx0	$\leftarrow Rx(n-1)$ $\leftarrow 0$	Rx: 40~7Fh
SL1	Rx	0101 0011 01XX XXXX	ACn, Rxn AC0, Rx0	$\leftarrow Rx(n-1)$ $\leftarrow 1$	Rx: 40~7Fh
DAA		0101 0100 0000 0000	AC	$\leftarrow \text{BCD(AC)}$	
DAA*	Rx	0101 0101 01XX XXXX	AC,Rx	$\leftarrow \text{BCD(AC)}$	Rx: 40~7Fh
DAA*	@HL	0101 0101 1000 0000	AC,@HL	$\leftarrow \text{BCD(AC)}$	
DAS		0101 0110 0000 0000	AC	$\leftarrow \text{BCD(AC)}$	

Instruction		Machine Code	Function		Flag/Remark
DAS*	Rx	0101 0111 01XX XXXX	AC,Rx	← BCD(AC)	Rx: 40~7Fh
DAS*	@HL	0101 0111 1000 0000	AC,@HL	← BCD(AC)	
LDS	Rx,D	0101 1DDD D1XX XXXX	AC,Rx	← D	Rx: 40~7Fh
LDH	Rx,@HL	0110 0000 01XX XXXX	AC,Rx	← H(T@HL)	Rx: 40~7Fh
LDH*	Rx,@HL	0110 0001 01XX XXXX	AC,Rx HL	← H(T@HL) ← HL + 1	Rx: 40~7Fh
LDL	Rx,@HL	0110 0010 01XX XXXX	AC,Rx	← L(T@HL)	Rx: 40~7Fh
LDL*	Rx,@HL	0110 0011 01XX XXXX	AC,Rx HL	← L(T@HL) ← HL + 1	Rx: 40~7Fh
MRF1	Rx	0110 0100 01XX XXXX	AC,Rx	← RFC3-0	Rx: 40~7Fh
MRF2	Rx	0110 0101 01XX XXXX	AC,Rx	← RFC7-4	Rx: 40~7Fh
MRF3	Rx	0110 0110 01XX XXXX	AC,Rx	← RFC11-8	Rx: 40~7Fh
MRF4	Rx	0110 0111 01XX XXXX	AC,Rx	← RFC15-12	Rx: 40~7Fh
STA	Rx	0110 1000 01XX XXXX	Rx	← AC	Rx: 40~7Fh
STA	@HL	0110 1000 1000 0000	@HL	← AC	
LDA	Rx	0110 1100 01XX XXXX	AC	← Rx	Rx: 40~7Fh
LDA	@HL	0110 1100 1000 0000	AC	← @HL	
MRA	Rx	0110 1101 01XX XXXX	CF	← Rx3	Rx: 40~7Fh
MRW	@HL,Rx	0110 1110 01XX XXXX	AC,@HL	← Rx	Rx: 40~7Fh
MWR	Rx,@HL	0110 1111 01XX XXXX	AC,Rx	← @HL	Rx: 40~7Fh
MRW	Ry,Rx	0111 0YYY Y1XX XXXX	AC,Ry	← Rx	Rx: 40~7Fh
MWR	Rx,Ry	0111 1YYY Y1XX XXXX	AC,Rx	← Ry	Rx: 40~7Fh
JB0	X	1000 00XX XXXX XXXX	PC	← X	if AC0 = 1
JB1	X	1000 10XX XXXX XXXX	PC	← X	if AC1 = 1
JB2	X	1001 00XX XXXX XXXX	PC	← X	if AC2 = 1
JB3	X	1001 10XX XXXX XXXX	PC	← X	if AC3 = 1
JNZ	X	1010 00XX XXXX XXXX	PC	← X	if AC ≠ 0
JNC	X	1010 10XX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 00XX XXXX XXXX	PC	← X	if AC = 0
JC	X	1011 10XX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 00XX XXXX XXXX	STACK PC	← PC + 1 ← X	
JMP	X	1101 00XX XXXX XXXX	PC	← X	
RTS		1101 1000 0000 0000	PC	← STACK	CALL Return
SCC	X	1101 1001 0X10 0XXX	X6 = 1 X6 = 0 X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cfq = BCLK : Cfq = PH0 : Cch = PH10 : Cch = PH8 : Cch = PH6	X: 0000 0000b ~ 0x00 0xxx b
SCA	X	1101 1010 00X0 0000	X5	: Enable SEF5	IOA4, X: 0 or 20h
SPA	X	1101 1100 000X X111	X4 X3	: Set A4 Pull-Low : Set A4 I/O	1:Output, 0: Input X: 0000 0000b ~ 000x x000b
SPB	X	1101 1101 000X XX01	X4 X3~0	: Set B4-3 Pull-Low : Set B4-3 I/O	1:Output, 0: Input X: 0000 0000b~ 000x xx00b
SPC	X	1101 1110 000X XXXX	X4 X3-0	: Set C4-1 Pull-Low / Low-Level-Hold : Set C4-1 I/O	1:Output, 0: Input X: 0000 0000b~ 000x xxxxb
TM2	Rx	1110 0100 01XX XXXX	Timer2	← Rx & AC	Rx: 40~7Fh
TM2	@HL	1110 0101 0000 0000	Timer2	← T@HL	
TM2X	X	1110 011X XXXX XXXX	X8,7,6=111	: Ctm = PH13	

Instruction		Machine Code	Function		Flag/Remark
			X8,7,6=110 X8,7,6=101 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: Ctm = PH11 : Ctm = PH7 : Ctm = PH5 : Ctm = FREQ : Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer2 Value	
SHE	X	1110 1000 0X0X X000	X6 X4 X3	: Enable HEF6 : Enable HEF4 : Enable HEF3	RFC TMR2 PDV X: 0000 0000b~ 0x0x x000b
SIE*	X	1110 1001 0X0X X00X	X6 X4 X3 X0	: Enable IEF6 : Enable IEF4 : Enable IEF3 : Enable IEF0	RFC TMR2 PDV APT X: 0000 0000b~ 0x0x x00xb
PLC	X	1110 101X 0X0X X00X	X8 X6 X4 X3 X0	: Reset PH15~11 : Reset HRF6 : Reset HRF4 : Reset HRF3 : Reset HRF0	RFC TMR2 PDV APT X:00000 0000b~ x 0x0x x00xb
SRF	X	1110 1100 00XX X0XX	X5 X4 X3 X1 X0	: Enable Cx Control : Enable TM2 Control : Enable Counter : Enable RT Output : Enable RR Output	ENX ETP ERR X: 0000 0000b~ 00xx x0xxb
SRE	X	1110 1101 0X00 0000	X6	: Enable SRF6	SRF6(APT) X: 0 or 40h
SF		1111 0000 0000 0001	X0	: CF Set	CF
RF		1111 0100 0000 0001	X0	: CF Reset	CF
SF2	X	1111 1000 0000 0XXX	X2 X1 X0	: Close all Segments : Dis-ENX Set : Reload 2 Set	RSOFF DED RL2
RF2	X	1111 1001 0000 0XXX	X2 X1 X0	: Release Segments : Dis-ENX Reset : Reload 2 Reset	RSOFF DED RL2
ALM	X	1111 101X XXXX XXXX	X8,7,6=111 X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: FREQ : DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

## Symbol Description

AC	: Accumulator	D	: Immediate Data
ACn	: Accumulator bit n	PC	: Program Counter
X	: Address	CF	: Carry Flag
Rx	: Memory of address X	ZERO	: Zero Flag
Rxn	: Memory bit n of address X	HL	: Index Register
Ry	: Memory of working register Y	BCLK	: System clock, stop only in STOP condition
HRFn	: HALT Release Flag	IEFn	: Interrupt Enable Flag
HEFn	: HALT Release Enable Flag	SRFn	: STOP Release Enable Flag
PDV	: Pre-Divider	SCFn	: Start Condition Flag
Lz	: LCD Latch	Cch	: Clock Source of Chattering Detector
@HL	: Address of Index	Cfq	: Clock Source of Frequency Generator
@L	: Low address of Index	SEFn	: Switch Enable Flag
@H	: High address of Index	FREQ	: Frequency Generator setting Value
L(T@HL)	: Low Nibble of Index ROM	( )	: Content of Register
H(T@HL)	: High Nibble of Index ROM	TMR	: Timer Overflow Release Flag
T@HL	: Address of Index ROM	Ctm	: Clock Source of Timer
RFOVF	: RFC Overflow Flag		