CONTENTS

# DS-TMU3110MS

USB 1.1 to Flash Controller

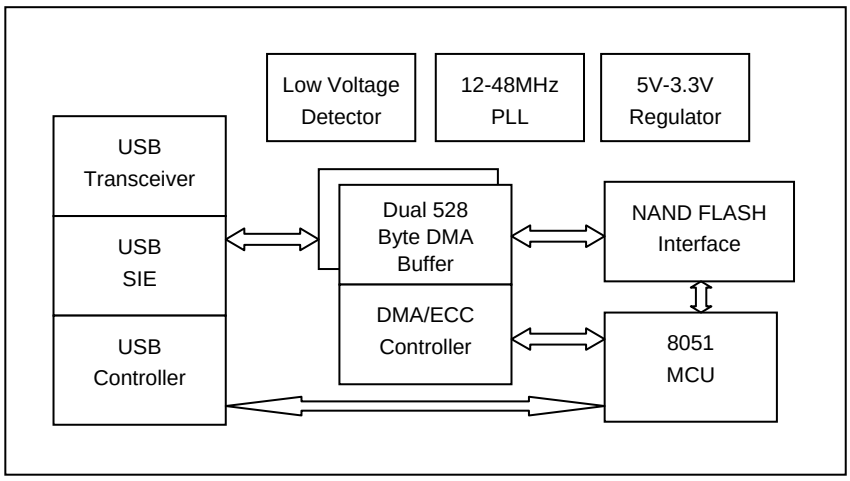
## 1. GENERAL DESCRIPTION

The TMU3110MS is an 8051 embedded device tailored to the USB Thumb Drive application. It is able to interface with maximum four Nand type Flash as its storage media and connect to PC through 12MHz Full-Speed USB bus. The TMU3110 provides the most cost-effectively solution for the emerging Flash Disc market.

## 2. FEATURES

- Compliance with the Universal Serial Bus specification v1.1
- Built-in USB Transceiver, 3.3V Regulator, and Low-Voltage-Reset circuitry
- USB mass storage class bulk-only transport compatible
- USB mass storage class SCSI transparent command set support
- Support flash memory from 32MB to 256MB
- Up to 1GB flash memory range supported
- H/W ECC Code generation
- Hardware write protection switch pin supported
- Dual 528 bytes buffer for DMA and USB Bulk data storage
- 2 partitions support
- Interface to maximum 4 NAND type Flash(32 pin SOP package only support up to 2 NAND type Flash)
- Support USB Suspend and Resume function
- 12MHz crystal oscillation with internal 48MHz PLL
- High performance data transfer rate up to 1M bytes per second
- No driver is needed under Microsoft Window ME/2000/XP, Mac OS 9.x, Linux with kernal 2.4.x
- Provide Window 98SE driver
- Window default format program is supported with the file system type FAT16/FAT32/NTFS
- LED indicator pin
- 48 pin LQFP package, 32 pin SOP package and Chip form available

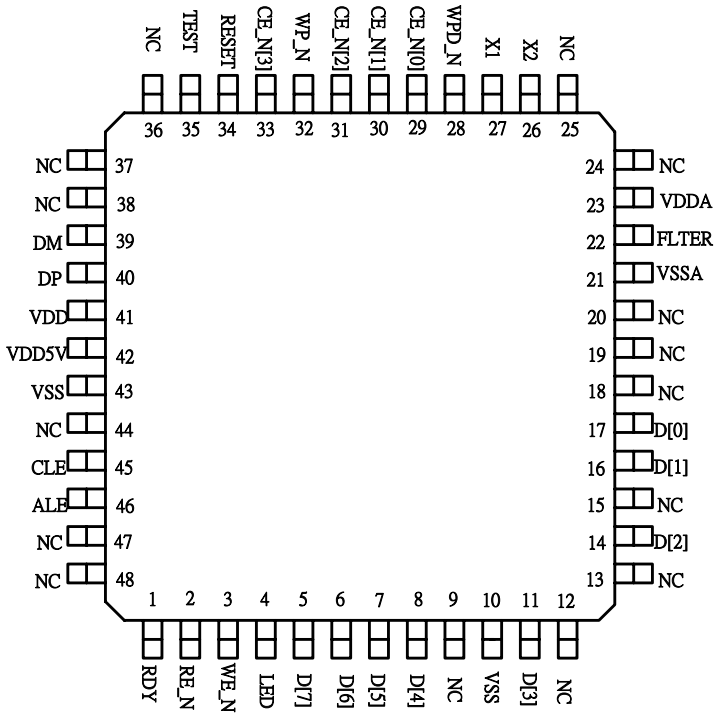
## 3. BLOCK DIAGRAM



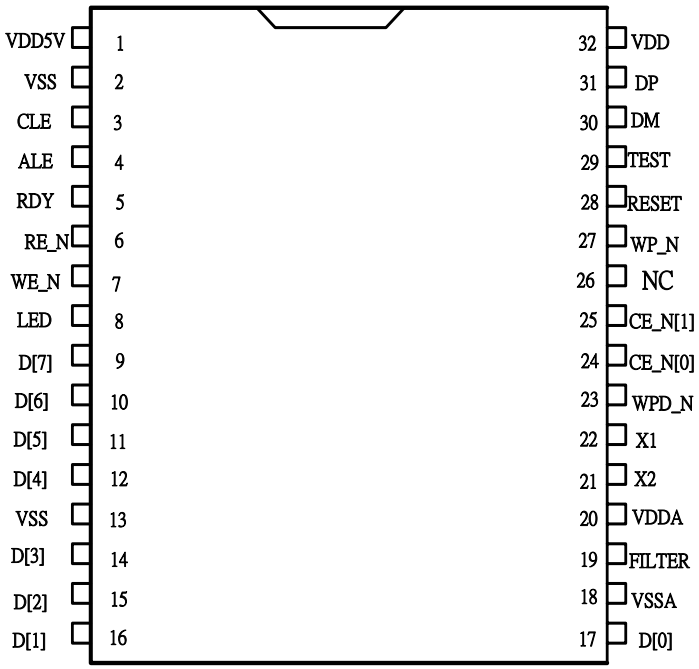
# 4. Pinning Information

### 4.1 PIN ASSIGNMENT

**a. 48 Pin LQFP**




**b. 32 Pin SOP**



**4.2 PIN DESCRIPTION**

| Name | I/O | Description |
|---|---|---|
| VDD | P | 3.3V Power, Regulator output |
| VSS | P | Ground |
| VDD5V | P | 5V Power from USB cable |
| VDDA | P | 3.3V analog power |
| VSSA | P | Analog ground |
| FILTER | O | 48MHz PLL capacitor connection |
| X1 | I | Crystal in (12MHz) |
| X2 | O | Crystal out |
| RESET | I | Chip reset |
| TEST | I | Test Mode control |
| DP | I/O | USB positive data signal |
| DM | I/O | USB negative data signal |
| WP_N | O | Flash write protect |
| CLE | I/O | Flash Command Latch Enable |
| ALE | I/O | Flash Address Latch Enable |
| RDY | I/O | Flash Ready/Busy |
| RE_N | O | Flash Read Strobe |
| WE_N | O | Flash Write Strobe |
| D[7:0] | I/O | Flash Data I/O |
| CE_N[3:0] | O | Flash Chip select |
| LED | I/O | LED indicator |
| WPD_N | I/O | Write protect detect |

# 5. FUNCTIONAL DESCRIPTION

**(1). 8051 CPU Core**
The CPU core running at 24MHz clock rate includes all 8051 functions with the following exceptions:
1.1 TMU3110MS provides 256 bytes internal RAM as 8052, while the standard 8051 provides 128 bytes.
1.2 UART function and the related SFR are not supported.

***Note: All registers listed in this document reside in external RAM area (XFR). For internal RAM memory map please refer to 8051 spec.***

**(2). DMA Transfer and ECC Calculation**
The TMU3110MS can transfer data between the XRAM buffer and Nand-Flash via DMA channel at 6MHZ clock rate. The DMA length can be set by F/W as 16, 256, 512 or 528 bytes. Once DMA being start, The H/W automatically calculates the 256 bytes data ECC and saves in the ECC registers. F/W launches DMA by giving the DMASTART bit a low to high transition. During the DMA period, the DMAFLG keeps at high and the data channel between Flash and XRAM is occupied. Since the DMAFLG is directly connected to 8051's Port3.3 inside TMU3110MS, F/W can poll it to test if DMA is over.

**(3). Power-Down and Idle Mode**
The Power-down/Idle mode is activated by F/W setting the PD/IDL bit in 8051's PCON register. In Power Down Mode, TMU3110MS's Crystal oscillation stops. In Idle mode, the 8051's instruction clock stops. The Power Down and Idle Mode are released by any enable interrupt. For standard 8051, Power Down Mode is released only by chip reset.

**(4). Built-in 3.3V Regulator**
This Regulator converts the 5V USB Bus power into 3.3V power for TMU3110MS and Nand-Flash.

**(5). Low Voltage Reseter (LVR)**
The LVR can generate chip reset when VDD5<4.0V, or VDD<2.5V, no matter power-on or power-off.

**(6). Built-in PLL**
The PLL can generate 48MHz clock for USB Bus signal synchronization.

**(7). USB Engine**
The USB engine includes the Serial Interface Engine (SIE), the high-speed USB I/O transceiver and the USB data buffers. The SIE block performs most of the USB interface function with only minimum support from S/W. Three endpoints are supported. Endpoint 0 is used to receive and transmit control (including SETUP) packets while Endpoint 1 and endpoint 2 are only used to transmit data packets.
The USB SIE handles the following USB bus activity independently:
1. Bitstuffing/unstuffing
2. CRC generation/checking
3. ACK/NAK
4. TOKEN type identification
5. Address checking

S/W handles the following tasks:
1. Coordinate enumeration by responding to SETUP packets
2. Fill and empty the FIFOs or RAM buffers
3. Suspend/Resume coordination
4. Verify and select DATA toggle values for Endpoint 0

7.1 USB Device Address

The USBADR register stores the device address. This register is reset to all 0 after chip reset or USB bus reset. S/W must write this register a valid value after the USB enumeration process.

7.2 Endpoint 0 receive

After receiving a packet and placing the data into the Endpoint 0 receive FIFO (RC0FIFO), TMU3110MS updates the Endpoint 0 status registers to record the receive status and then generates an Endpoint 0 receive interrupt (RC0I). S/W can read the status registers for the recent transfer information, which includes the data byte count (RC0CNT), data direction (EP0DIR), SETUP token flag (EP0SET) and data valid flag (RC0ERR). The received data is always stored into RC0FIFO and the RC0CNT is always updated for DATA packets following SETUP tokens. The data following an OUT token is written into the RC0FIFO, and the RC0CNT is updated unless Endpoint 0 STALL (EP0STALL) is set or Endpoint 0 receive ready (RC0RDY) is cleared. The SIE clears the RC0RDY automatically and generates RC0I interrupt when the RC0CNT / RC0FIFO is updated. As long as the RC0RDY is cleared, SIE keep responding NAK to Host's Endpoint 0 OUT packet request. F/W should set the RC0RDY flag after the RC0I interrupt is asserted and RC0FIFO is read out.

7.3 Endpoint 0 transmit

After detecting a valid Endpoint 0 IN token, TMU3110MS automatically transmit the data pre-stored in the Endpoint 0 transmit FIFO (TX0FIFO) to the USB bus if the Endpoint 0 transmit ready flag (TX0RDY) is set and the EP0STALL is cleared. The number of byte to be transmitted is according to the Endpoint 0 transmit byte count register (TX0CNT). The DATA0/1 token to be transmitted is according to the Endpoint 0 transmit toggle control bit (TX0TGL). After the TX0FIFO is updated, TX0RDY should be set to 1. This enables the TMU3110MS to respond to an Endpoint 0 IN packet. TX0RDY is cleared and an Endpoint 0 transmit interrupt (TX0I) is generated once the USB host acknowledges the data transmission. The interrupt service routine can check TX0RDY to confirm that the data transfer was successful.

7.4 Endpoint 1 transmit

Endpoint 1 is capable of transmit only. This endpoint is enabled when the Endpoint 1 configured control bit (EP1CFG) is set. To properly use this endpoint, F/W must assign exactly one XRAM buffer as USB Bulk transfer buffer. Once this endpoint is enabled, F/W should clear the Toggle sequence bit (CLRTX1TGL) and clear the BULK current counter (CLRBULKCNT) for initialization. After detecting a valid Endpoint 1 IN token, The TMU3110MS automatically transmit the data pre-stored in the XRAM buffer to the USB bus if the Endpoint 1 transmit ready flag (TX1RDY) is set and the EP1STALL is cleared. The number of byte to be transmitted is according to the Setting Bulk byte count register (BULKSETCNT). The DATA0/1 token to be transmitted is toggled by H/W itself. If the BULKSETCNT is greater than 64, H/W will transmit several 64 bytes data packets and the remainder to USB host according to the consecutive Endpoint 1 IN token until the Bulk Current Counter (BULKCURCNT) equals the BULKSETCNT. In the mean time, TX1RDY is cleared and an Endpoint 1 transmit interrupt (TX1I) is generated. During the packet transfer stage, the H/W automatically resends data packet if Host fail to acknowledge the data transmission.

7.5 Endpoint 2 receive

Endpoint 2 is capable of receive only. This endpoint is enabled when the Endpoint 2 configured control bit (EP2CFG) is set. To properly use this endpoint, F/W must assign exactly one XRAM buffer as USB Bulk transfer buffer. Once this endpoint is enabled, F/W should clear the Toggle sequence bit (CLRRC2TGL) and clear the BULK current counter (CLRBULKCNT) for initialization. After detecting a valid Endpoint 2 OUT token, The TMU3110MS automatically stores the Bulk data into the XRAM buffer and increases BULKCURCNT if the Endpoint 2 receive ready flag (RC2RDY) is set and the EP2STALL is cleared. The expected number of byte to be received is according to the Setting Bulk byte count register (BULKSETCNT). The DATA0/1 token to be checked is toggled by H/W itself. If the BULKSETCNT is greater than 64, H/W will receive several 64 bytes data packets and the remainder from USB host according to the consecutive Endpoint 2 OUT token. Once the BULKCURCNT being greater than the BULKSETCNT or a data packet other than 64 bytes received, the RC2RDY is cleared and an Endpoint 2 receive interrupt (RC2I) is generated. During the packet transfer stage, the H/W automatically drops data packet if data sequence bit mismatch.

7.6 Endpoint 0 Control Read

F/W should set the CTRRD bit when program detects the current transfer is an Endpoint 0 Control Read Transfer. Once this bit is set, the TMU3110MS will stall an Endpoint 0 OUT packet with DATA toggle 0 or byte count other than 0.

7.7 Suspend and Resume

Once the Suspend condition is asserted, F/W can set the SUSPND bit to save power. F/W can further save the device power by force the 8051 CPU core into the Power Down or Idle mode by setting the PCON register in SFR. In the Idle mode, the Crystal keeps oscillating and CPU can be waken-up by the trigger of any enabled interrupt. In the Power Down mode, the Crystal is stop, but CPU can be waken-up by USB bus reset or USB bus resume. As to the remote wake up function, the TMU3110MS can send Resume signaling to USB bus when SUSPND=1 and RSMO=1.

7.8 Interrupt

There are several interrupts generated by the USB Engine. Each interrupt source has its own enable control bit. An interrupt event will set its individual flag. If the corresponding interrupt enable bit has been set, it would trigger 8051's INT0. F/W MUST clear the interrupt event register while serves the interrupt routine.

7.9 XRAM buffer handling

The dual XRAM buffer allow TMU3110MS to exchange Bulk data with USB Host by one buffer, while F/W access or activate DMA in the other XRAM buffer. F/W should avoid accessing the XRAM buffer being assigned to USB.

# 6. Electrical Characteristics

**ABSOLOUTE MAXIMUM RATINGS**

GND= 0V

| Name | Symbol | Range | Unit |
|---|---|---|---|
| Maximum Supply Voltage | VDD5 | -0.3 to 5.5 | V |
| Maximum Supply Voltage | VDD3 | -0.3 to 3.6 | V |
| Maximum Input Voltage | Vin | -0.3 to VDD3+0.3 | V |
| Maximum output Voltage | Vout | -0.3 to VDD3+0.3 | V |
| Maximum Operating Temperature | Topg | -20 to +70 | ℃ |
| Maximum Storage Temperature | Tstg | -25 to +125 | ℃ |

**RECOMMEND OPERATING CONDITION**

at Ta=-20℃ to 70℃,GND= 0V

| Name | Symb. | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage | VDD5 | 4.5 | 5.5 | V |
| Input “H” Voltage | Vih | 2.4 | 3.6 | V |
| Input “L” Voltage | Vil1 | 0 | 0.8 | V |
| Input “L” Voltage | Vil1 | 0 | 0.8 | V |

**DC CHARACTERISTICS**

at Ta=-25 ℃,VDD5V=5.0V, VSS= 0V, Fosc=12MHz

| Name | Symb. | Min. | Typ. | Max. | Unit | Condition |
|---|---|---|---|---|---|---|
| Operating current | Icc | | 6.3 | | mA | Fosc=12MHz |
| Power Down current | Ipd | | 370 | | uA | No load |
| Output High Voltage | Voh | | 2.8 | | V | Ioh=50uA |
| Output Low Voltage | Vol | | 0.4 | | V | Iol=20mA |
| RESET pull down resistor | Rrst | | 68 | | Kohm | (Vrst=3.3v) |
| LED sink current | Iled | | 20 | | mA | Vled=2.9V |
| Input High Voltage | Vih | 2.0 | | | V | |
| Input Low Voltage | Vil | | | 0.8 | V | |
| VDD output voltage | V33 | | 3.3 | | V | |

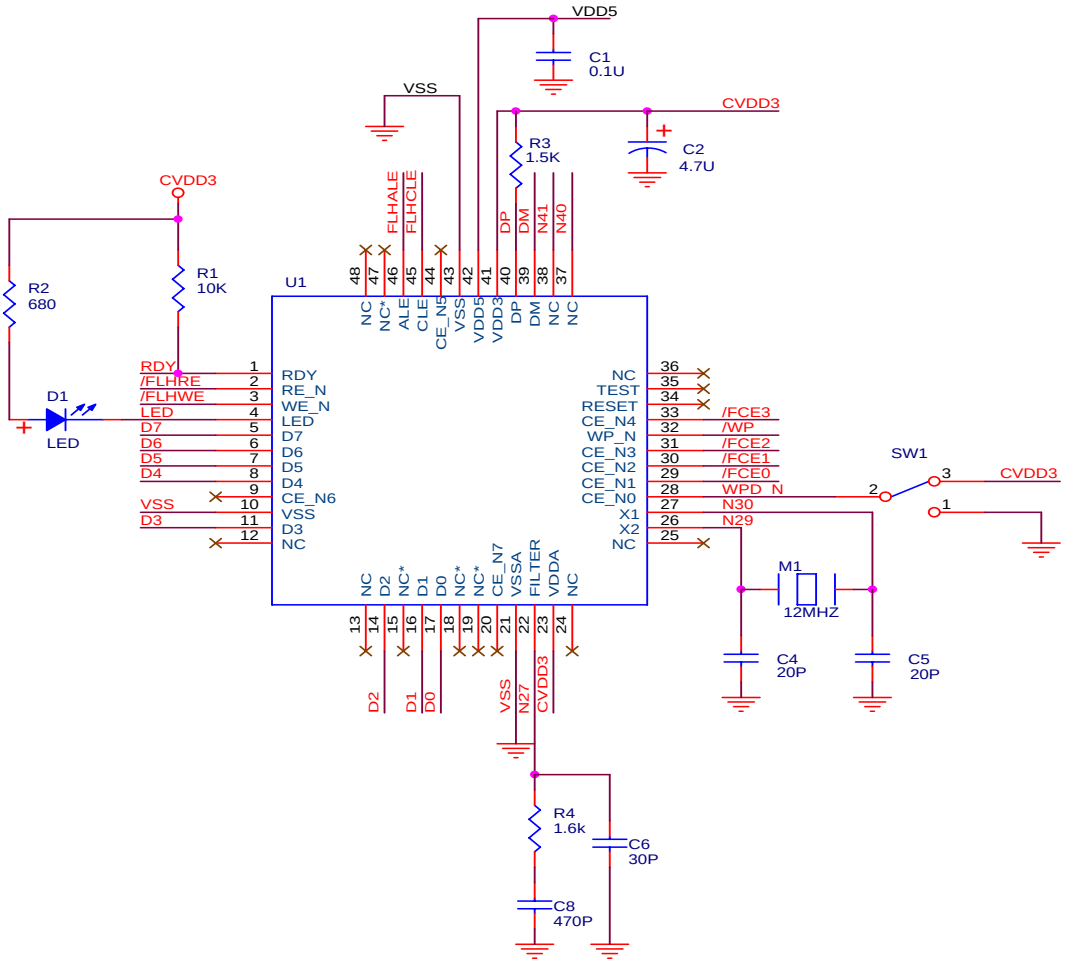
**AC CHARACTERISTICS**

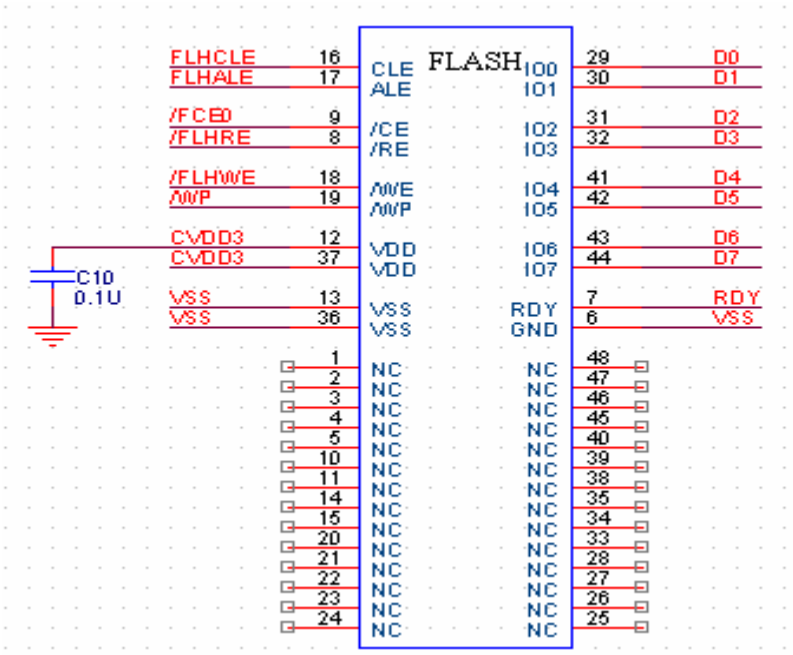
at Ta=-25 ℃,VDD5V=5.0V, VSS= 0V, Fosc=12MHz

| Name | Symb. | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| DP/DM rising time | Trise | 4 | | 20 | ns | |
| DP/DM falling time | Tfall | 4 | | 20 | ns | |
| DP,DM cross point | Vx | 1.3 | | 2.0 | V | |
| CPU Clock Freq. | Fcpu | | 24 | | MHz | |

Note: All USB transceiver characteristics can meet USB1.1 spec.

# 7. APPLICATION CIRCUIT

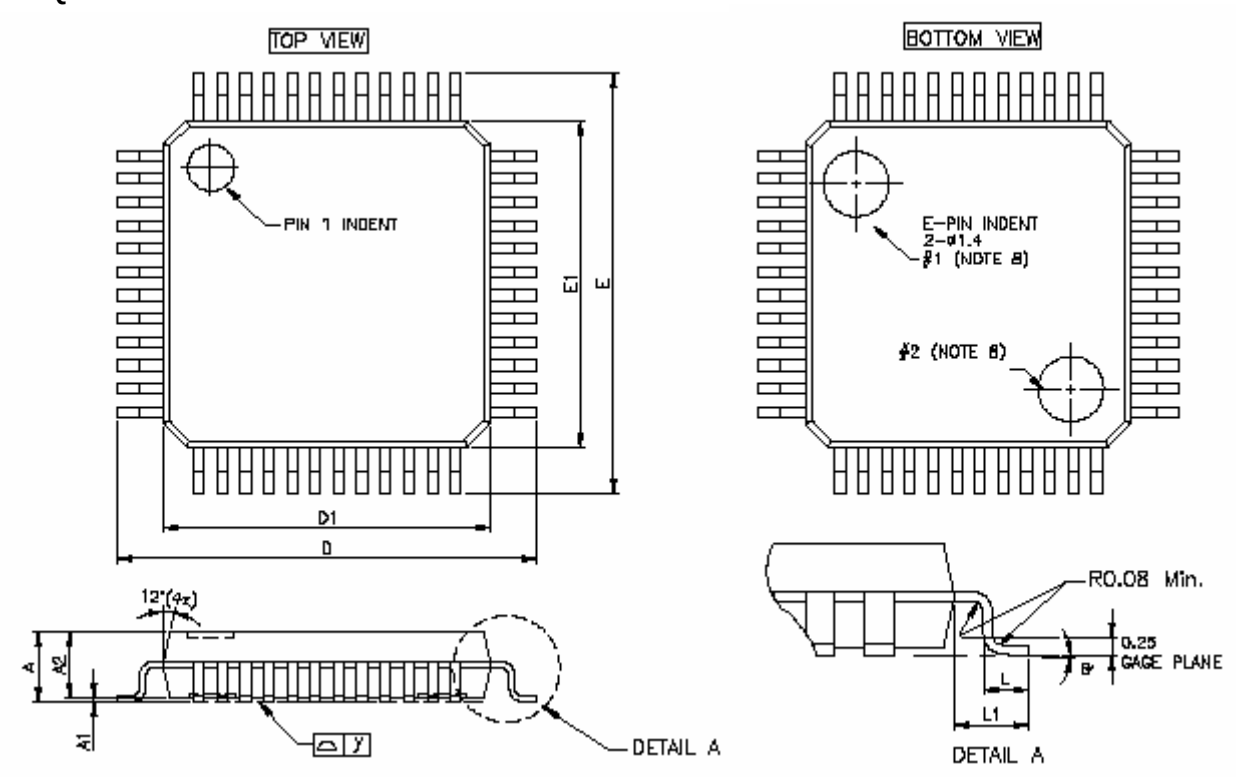





* The Flash pin assignment is the same for Samsung K9F5608U0M, K9F1208U0M, K9K1G08U0M, K9K2G08U0M

## 8. Package/Pad Locations

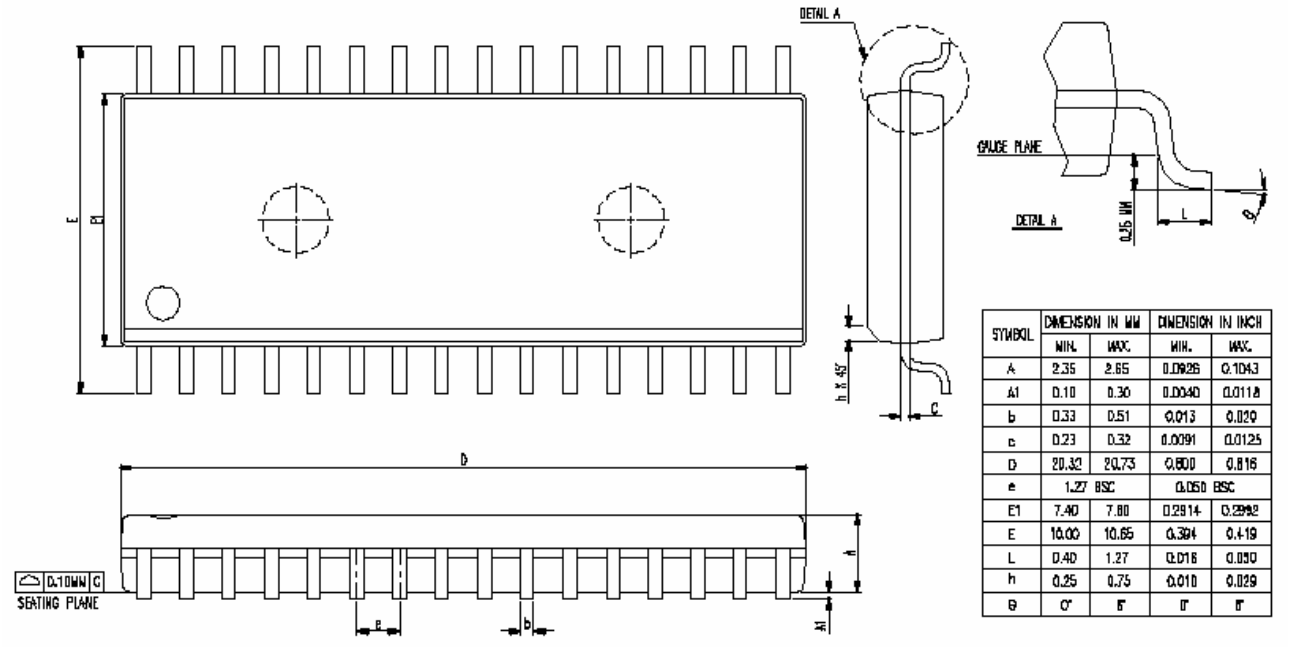
**a. LQFP 48**




| SYMBOL | DIMENSIONS IN MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | —— | —— | 1.60 |
| A1 | 0.05 | —— | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| C | 0.09 | —— | 0.20 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| e | —— | 0.50 | —— |
| L | 0.45 | 0.60 | 0.75 |
| L1 | —— | 1.00 | —— |
| θ° | 0° | 3.5° | 7° |
| y | 0.0 | —— | 0.08 |

**LQFP48 pin**

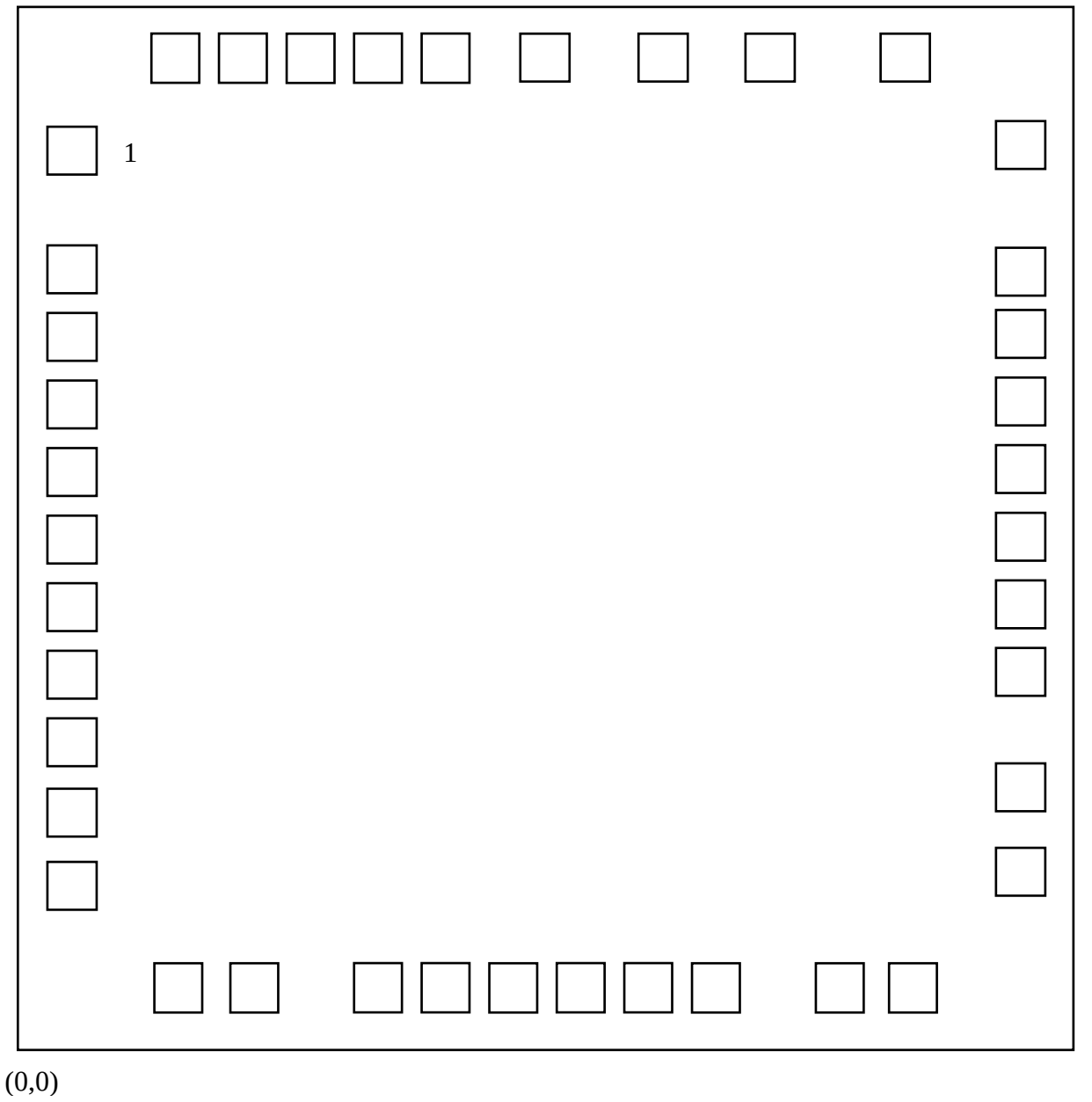
**b. SOP 32**




| SYMBOL | DIMENSION IN MM | | DIMENSION IN INCH | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 2.35 | 2.65 | 0.0926 | 0.1043 |
| A1 | 0.10 | 0.30 | 0.0040 | 0.0118 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| c | 0.23 | 0.32 | 0.0091 | 0.0125 |
| D | 20.32 | 20.73 | 0.800 | 0.816 |
| e | 1.27 BSC | | 0.050 BSC | |
| E1 | 7.40 | 7.80 | 0.2914 | 0.2992 |
| E | 10.00 | 10.65 | 0.394 | 0.419 |
| L | 0.40 | 1.27 | 0.016 | 0.050 |
| h | 0.25 | 0.75 | 0.010 | 0.029 |
| θ | 0° | 8° | 0° | 8° |

**SOP 32 pin**

**8.2 Pad Locations**



| Probe Number | PAD NAME | X Coordinate | Y Coordinate | Probe Number | PAD NAME | X Coordinate | Y Coordinate |
|---|---|---|---|---|---|---|---|
| 1 | RDY | 96.00 | 1678.60 | 21 | VDDA | 1686.00 | 96.00 |
| 2 | RE_N | 96.00 | 1443.60 | 22 | X2 | 1894.00 | 299.30 |
| 3 | WE_N | 96.00 | 1318.60 | 23 | X1 | 1894.00 | 453.20 |
| 4 | LED | 96.00 | 1193.60 | 24 | WPD_N | 1894.00 | 691.60 |
| 5 | D[7] | 96.00 | 1068.60 | 25 | CE_N[0] | 1894.00 | 816.60 |
| 6 | D[6] | 96.00 | 934.60 | 26 | CE_N[1] | 1894.00 | 941.60 |
| 7 | D[5] | 96.00 | 8118.60 | 27 | CE_N[2] | 1894.00 | 1066.60 |
| 8 | D[4] | 96.00 | 693.60 | 28 | WP_N | 1894.00 | 1191.60 |
| 9 | NC | 96.00 | 568.60 | 29 | CE_N[3] | 1894.00 | 1316.60 |
| 10 | VSS | 96.00 | 431.60 | 30 | RESET | 1894.00 | 1443.60 |
| 11 | D[3] | 96.00 | 290.00 | 31 | TEST | 1894.00 | 1678.60 |
| 12 | D[2] | 304.00 | 96.00 | 32 | DM | 1673.70 | 1874.00 |
| 13 | NC | 450.50 | 96.00 | 33 | DP | 1418.90 | 1874.00 |
| 14 | D[1] | 682.50 | 96.00 | 34 | VDD | 1208.70 | 1874.00 |
| 15 | D[0] | 807.50 | 96.00 | 35 | VDD5V | 995.70 | 1874.00 |
| 16 | NC | 932.50 | 96.00 | 36 | VSS | 795.90 | 1874.00 |
| 17 | NC | 1057.50 | 96.00 | 37 | NC | 670.90 | 1874.00 |
| 18 | NC | 1182.50 | 96.00 | 38 | CLE | 545.90 | 1874.00 |
| 19 | VSSA | 1307.50 | 96.00 | 39 | ALE | 420.90 | 1874.00 |
| 20 | FILTER | 1542.50 | 96.00 | 40 | NC | 295.90 | 1874.00 |