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TM8724

DATA SHEET

Rev 1.3

AMENDMENT HISTORY

Version	Date	Description
1.0	Apr, 2006	New release
1.1	Apr, 2015	1. Delete watchdog timer in GENERAL DESCRIPTION. (P.1) 2. Delete PAD COORDINATE (P.3)
1.2	Oct, 2018	Corrected LZ from 5 bits to 4 bits, the changed commands are: LCT, LCB, LCP, LCD (P.13)
1.3	Apr, 2022	Modify bit6 of SCC machine code to “0”

CONTENTS

GENERAL DESCRIPTION

The TM8724 is an embedded high-performance 4-bit microcomputer with LCD driver. It contains all the necessary functions, such as 4-bit parallel processing ALU, ROM, RAM, I/O ports, timer, clock generator, dual clock operation, LCD driver, look-up table in a single chip.

FEATURE

1. 1.5V and 3V operations and with low power dissipation.

2. Powerful instruction set (129 instructions).

- Binary addition, subtraction, BCD adjust, logical operation in direct and index addressing mode.
- Single-bit manipulation (set, reset, decision for branch).
- Various conditional branches.
- 16 working registers and manipulation.
- Table look-up.
- LCD driver data transfer.

3. Memory capacity.

- ROM capacity 1152 x 16 bits.
- RAM capacity 80 x 4 bits.

4. LCD driver output.

- 5 common outputs and 24 segment outputs (up to drive 120 LCD pixels).
- 1/1 Duty, 1/2 Duty, 1/3 Duty, 1/4 Duty or 1/5 Duty is selected by MASK option.
- 1/2 Bias or 1/3 Bias is selected by MASK option.
- Single instruction to turn off all segments and coms.
- Segment output pins (SEG1~12) could be defined as CMOS or P_open drain output type by mask option.

5. Input/output ports.

- Port IOA 4 pins, muxed with SEG24~SEG27.
- Port IOB 4 pins (with internal pull-low), muxed with SEG28~SEG31.
- Port IOC 4 pins (with internal pull-low), muxed with SEG32~SEG35.
  IOC port had built in the input signal chattering prevention circuitry.

6. 8 level subroutine nesting.

7. Interrupt function.

- External factor 2 (INT pin, Port IOC).
- Internal factors 2 (Pre-Divider, Timer1).

8. Built in Alarm generator.

- BZB, BZ (Muxed with SEG30, SEG31).

9. One 6-bit programmable timer with programmable clock source.

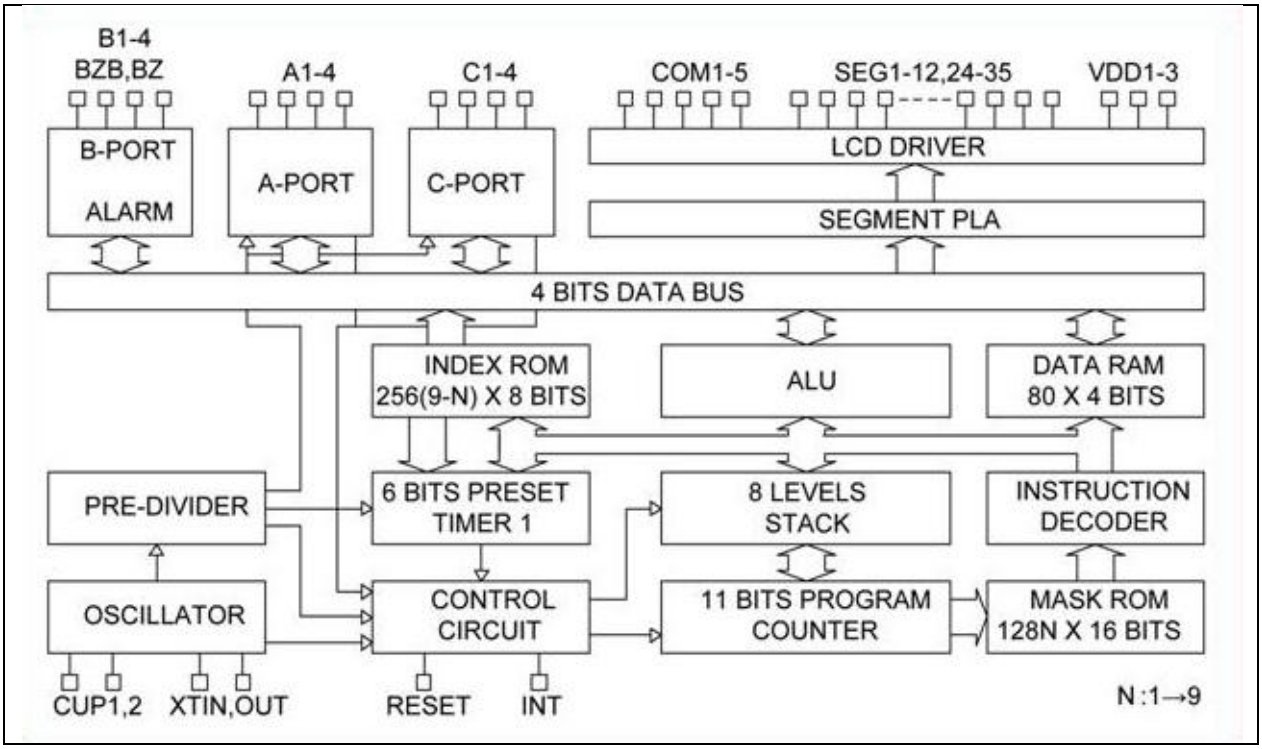
10. Built-in Voltage doubler, tripler charge pump circuit.

11. Dual clock operation.

12. HALT function.

13. STOP function.

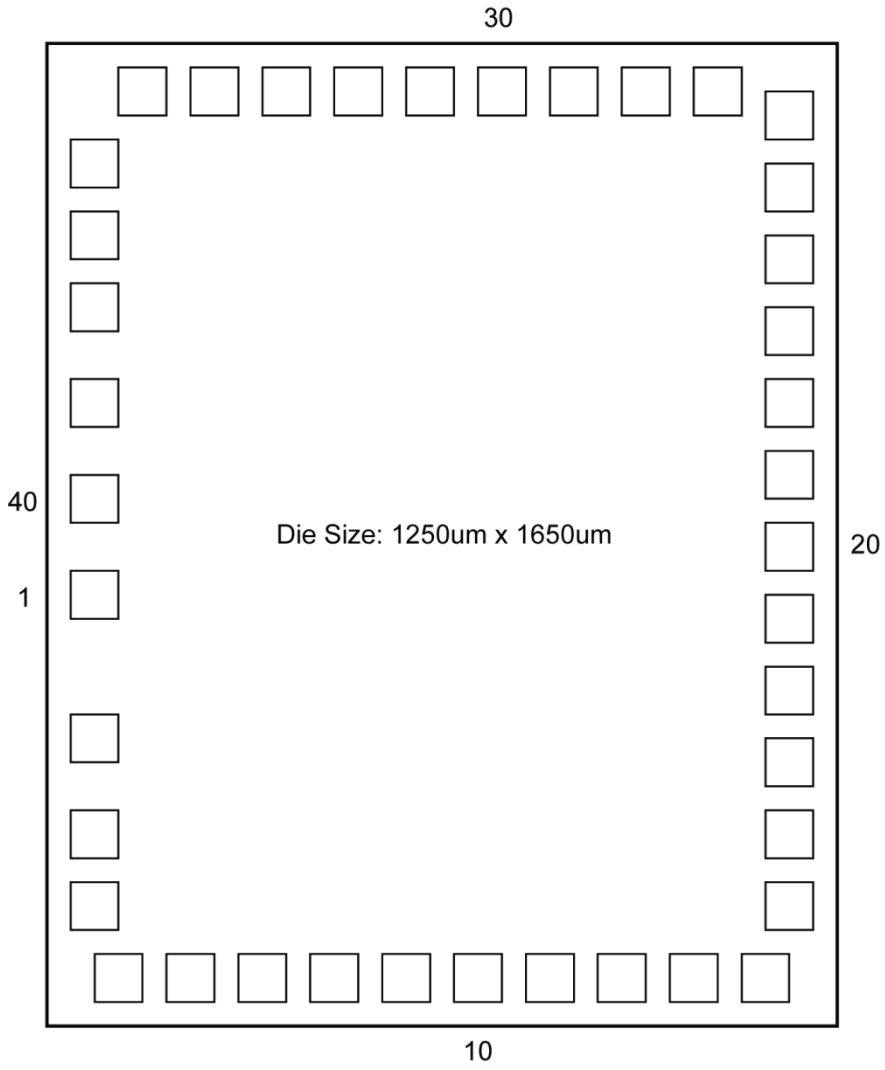
BLOCK DIAGRAM



APPLICATION

- Timer / Calendar / Calculator

PAD DIAGRAM



The substrate of chip should be connected to GND.

PIN DESCRIPTION

Name	I/O	Description
VDD1, 2, 3	P	LCD supplies voltage, and positive supply voltage.
RESET	I	Input pin for external reset request signal, built-in internal pull-down resistor.
INT	I	Input pin for external interrupt request signal. ◆ Falling edge or rising edge triggered is defined by mask option. ◆ Internal pull-down or pull-up resistor is defined by mask option.
TEST		Test signal input pin.
CUP1, 2	O	Switching pins for supply the LCD driving voltage to the VDD1, 2, 3 pins. ◆ Connect the CUP1 and CUP2 pins with non-polarized electrolytic capacitor when chip operated in 1/2 or 1/3 bias mode. ◆ In no BIAS mode, leave these pins opened.
XIN XOUT	I O	Time base counter frequency (clock specified. LCD alternating frequency. Alarm signal frequency) or system clock oscillation. ◆ 32KHz Crystal oscillator or External RC for SLOW ONLY or DUAL by mask option. ◆ In FAST ONLY mode option, connect an external resistor could compose a RC oscillator.
COM1~5	O	Output pins for driving the common pins of the LCD panel.
SEG1-12, SEG24-35	O	Output pins for driving the LCD panel segment.
IOA1-4	I/O	Input / Output port A. (muxed with SEG24~27)
IOB1-4	I/O	Input / Output port B. (muxed with SEG28~30)
IOC1-4	I/O	Input / Output port C. (muxed with SEG32~35)
BZB/BZ	O	Output port for alarm generator
GND	P	Negative supply voltage.

ABSOLOUTE MAXIMUM RATINGS

at Ta=-40 to 80°C,GND= 0V

Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD1	-0.3 to 2.0	V
	VDD2	-0.3 to 4.0	
	VDD3	-0.3 to 6.0	
Maximum Input Voltage	Vin	-0.3 to VDD1/2+0.3	
Maximum output Voltage	Vout1	-0.3 to VDD1/2+0.3	
	Vout2	-0.3 to VDD3+0.3	
Maximum Operating Temperature	Topg	-40 to +80	°C
Maximum Storage Temperature	Tstg	-50 to +125	

POWER CONSUMPTION

at Ta=-40 to 80°C,GND= 0V

Name	Sym.	Condition	Min.	Typ.	Max.	Unit
HALT mode	IHALT1	Only 32.768KHz Crystal Oscillator operating, without loading. (BCF = 0) Ag mode, VDD1=1.5V, BCF = 0		2	5	uA
	IHALT2	Only 32.768KHz Crystal Oscillator operating, without loading. (BCF = 0) Li mode, VDD2=3.0V, BCF = 0		5	10	
STOP mode	ISTOP				1	

Note:

When RC oscillator function is operating, the current consumption will depend on the frequency of oscillation.

ALLOWABLE OPERATING CONDITIONS

at Ta=-40 to 80°C,GND= 0V

Name	Symb.	Condition	Min.	Max.	Unit
Supply Voltage	VDD1		1.2	1.8	V
	VDD2		2.4	3.6	
	VDD3		2.4	5.4	
Supply Voltage	VDD1	Ag Mode	1.2	1.65	
Supply Voltage	VDD2	EXT-V, Li Mode	2.4	5.25	
Oscillator Start-Up Voltage	VDDB	Crystal Mode	1.3		
Oscillator Sustain Voltage	VDDB	Crystal Mode	1.2		
Input “H” Voltage	Vih1	Ag Battery Mode	VDD1-0.7	VDD1+0.7	
Input “L” Voltage	Vil1		-0.7	0.7	
Input “H” Voltage	Vih2	Li Battery Mode	VDD2-0.7	VDD2+0.7	
Input “L” Voltage	Vil2		-0.7	0.7	
Input “H” Voltage	Vih3	OSCIN at Ag Battery Mode	0.8xVDD1	VDD1	
Input “L” Voltage	Vil3		0	0.2xVDD1	
Input “H” Voltage	Vih4	OSCIN at Li Battery Mode	0.8xVDD2	VDD2	
Input “L” Voltage	Vil4		0	0.2xVDD2	
Operating Freq	Fopg1	Crystal Mode	32		KHz
	Fopg2	RC/CF Mode	10	1000	

INTERNAL RC FREQUENCY RANGE

Option Mode	BAK	Min.	Typ.	Max.
250KHz	1.5V	300KHz	350KHz	400KHz
	3.0V	250KHz	300KHz	350KHz
500KHz	1.5V	550KHz	650KHz	750KHz
	3.0V	450KHz	550KHz	650KHz

ELECTRICAL CHARACTERISTICS

- at #1:VDD1=1.5V(Ag);
- at #2:VDD2=3.0V(Li);

Input Resistance

Name	Symb.	Condition	Min.	Typ.	Max.	Unit
IOB, C Pull-Down Tr	Rmad1	Vi=VDD1, #1	200	500	1000	KΩ
	Rmad2	Vi=VDD2, #2	200	500	1000	
INT Pull-up Tr	Rintu1	Vi=VDD1, #1	100	250	500	
	Rintu2	Vi=VDD2, #2	100	250	500	
INT Pull-Down Tr	Rintd1	Vi=GND, #1	200	500	1000	
	Rintd2	Vi=GND, #2	200	500	1000	
RES Pull-Down R	Rres1	Vi=VDD1, #1	10	40	100	
	Rres2	Vi=VDD2, #2	10	40	100	

DC Output Characteristics

Name	Symb.	Condition	Port	Min.	Typ.	Max.	Unit
Output "H" Voltage	Voh1c	Ioh=-200uA	COM1~5 SEG1~35	0.8	0.9	1.0	V
	Voh2c	Ioh=-1mA		1.5	1.8	2.1	
Output "L" Voltage	Vol1c	Iol=400uA		0.2	0.3	0.4	
	Vol2c	Iol=2mA		0.3	0.6	0.9	

Segment Driver Output Characteristics

(1). Static Display Mode

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
Output "H" Voltage	Voh1d	Ioh=-1uA, #1	SEG-n	1.0			V
	Voh2d	Ioh=-1uA, #2		2.2			
Output "L" Voltage	Vol1d	Iol=1uA, #1				0.2	
	Vol2d	Iol=1uA, #2				0.2	
Output "H" Voltage	Voh1e	Ioh=-10uA, #1	COM-n	1.0			
	Voh2e	Ioh=-10uA, #2		2.2			
Output "L" Voltage	Vol1e	Iol=10uA, #1				0.2	
	Vol2e	Iol=10uA, #2				0.2	

(2). 1/2 Bias Display Mode

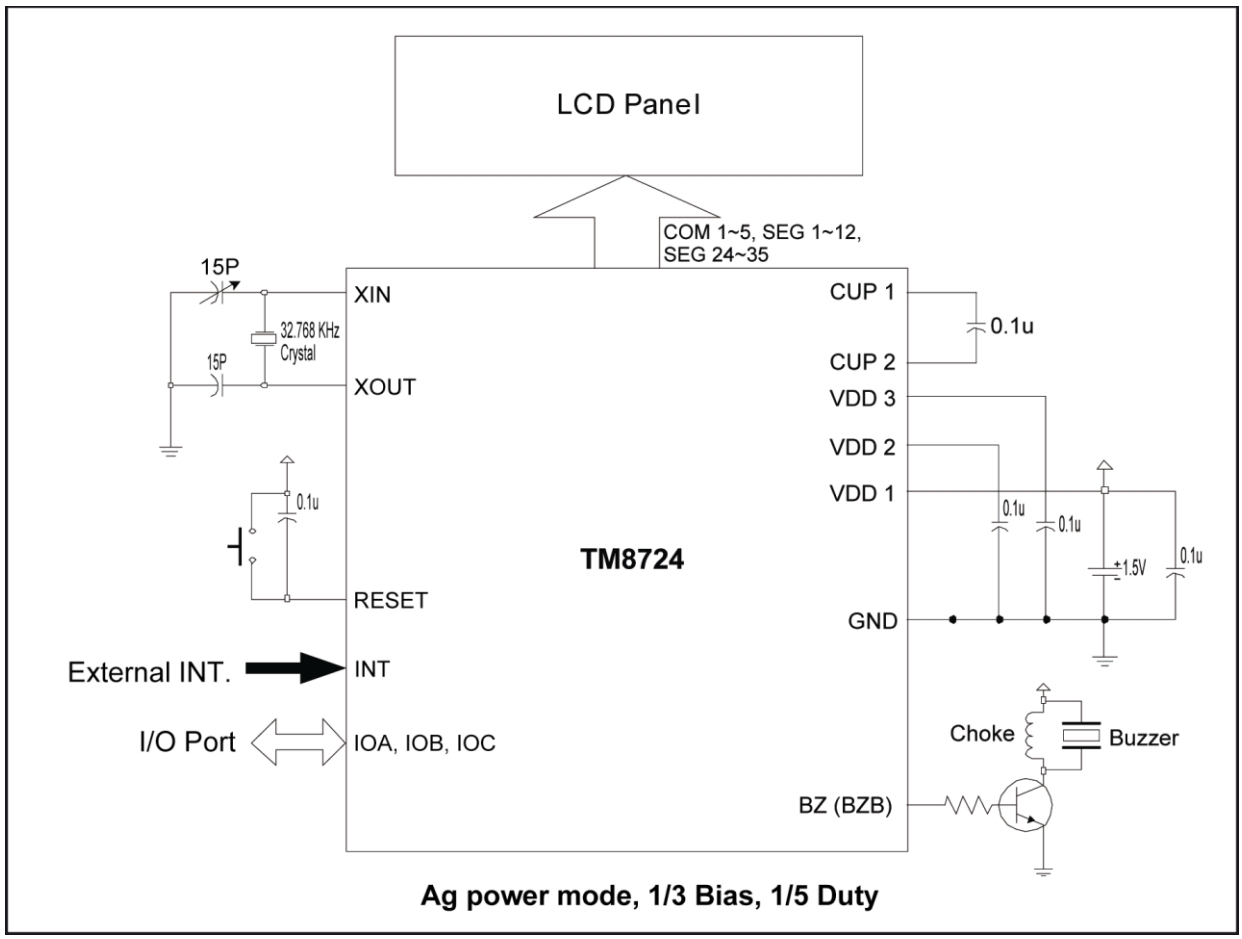
Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
Output ”H” Voltage	Vohd	Ioh=-1uA, #1, #2	SEG-n	2.2			V
Output ”L” Voltage	Vold	Iol=1uA, #1,#2				0.2	
Output ”H” Voltage	Vohe	Ioh=-10uA, #1, #2	COM-n	2.2			
Output ”M” Voltage	Vom1e	Iol/h=+/-10uA, #1,#2		1.0		1.4	
Output ”L” Voltage	Vole	Iol=10uA, #1, #2				0.2	

(3). 1/3 Bias display Mode

Name	Symb.	Condition	For	Min.	Typ.	Max.	Unit.
Output ”H” Voltage	Vohf	Ioh=-1uA, #1, #2	SEG-n	3.4			V
Output ”M1” Voltage	Vom1f	Iol/h=+/-10uA, #1, #2		1.0		1.4	
Output ”M2” Voltage	Vom2f	Iol/h=+/-10uA, #1, #2		2.2		2.6	
Output ”L” Voltage	Volf	Iol=1uA, #1, #2				0.2	
Output ”H” Voltage	Vohg	Ioh=-10uA, #1, #2	COM-n	3.4			
Output ”M1” Voltage	Vom1g	Iol/h=+/-10uA, #1, #2		1.0		1.4	
Output ”M2” Voltage	Vom2g	Iol/h=+/-10uA, #1, #2		2.2		2.6	
Output ”L” Voltage	Volg	Iol=10uA, #1, #2				0.2	

Typical Application Circuit

This application circuit is simply an example, and is not guaranteed to work.



Appendix A - TM8724 Instruction Table

Instruction		Machine Code	Function		Flag/Remark
NOP		0000 0000 0000 0000	No Operation		
LCT	Lz,Ry	0000 0010 ZZZZ YYYY	(Lz)	←7SEG ← (Ry)	
LCB	Lz,Ry	0000 0100 ZZZZ YYYY	(Lz)	←7SEG ←(Ry)	Blank Zero
LCP	Lz,Ry	0000 0110 ZZZZ YYYY	(Lz)	← (Ry) , (AC)	
LCD	Lz,@HL	0000 1000 ZZZZ 0000	(Lz)	← (R@HL)	
LCT	Lz,@HL	0000 1000 ZZZZ 0001	(Lz)	←7SEG ←(R@HL)	
LCB	Lz,@HL	0000 1000 ZZZZ 0010	(Lz)	←7SEG ←(R@HL)	Blank Zero
LCP	Lz,@HL	0000 1000 ZZZZ 0011	(Lz)	←(R@HL) , (AC)	
OPA	Rx	0000 1010 0XXX XXXX	(IOA)	← (Rx)	
OPAS	Rx,D	0000 1011 DXXX XXXX	IOA1,2,3,4	← (Rx)0,(Rx)1,D,Pulse	
OPB	Rx	0000 1100 0XXX XXXX	(IOB)	←(Rx)	
OPC	Rx	0000 1101 0XXX XXXX	(IOC)	←(Rx)	
MVL	Rx	0001 1100 0XXX XXXX	(@L)	← (Rx)	
MVH	Rx	0001 1101 0XXX XXXX	(@H)	← (Rx) , (AC)	
ADC	Rx	0010 0000 0XXX XXXX	(AC)	← (Rx) + (AC) + CF	CF
ADC	@HL	0010 0000 1000 0000	(AC)	← (R@HL) + (AC) + CF	CF
ADC*	Rx	0010 0001 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC) + CF	CF
ADC*	@HL	0010 0001 1000 0000	(AC),(R@HL)	← (R@HL) + (AC) + CF	CF
SBC	Rx	0010 0010 0XXX XXXX	(AC)	← (Rx) + (AC)B + CF	CF
SBC	@HL	0010 0010 1000 0000	(AC)	← (R@HL) + (AC)B + CF	CF
SBC*	Rx	0010 0011 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)B + CF	CF
SBC*	@HL	0010 0011 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)B + CF	CF
ADD	Rx	0010 0100 0XXX XXXX	(AC)	← (Rx) + (AC)	CF
ADD	@HL	0010 0100 1000 0000	(AC)	← (R@HL) + (AC)	CF
ADD*	Rx	0010 0101 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	CF
ADD*	@HL	0010 0101 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)	CF
SUB	Rx	0010 0110 0XXX XXXX	(AC)	← (Rx) + (AC)B + 1	CF
SUB	@HL	0010 0110 1000 0000	(AC)	← (R@HL) + (AC)B + 1	CF
SUB*	Rx	0010 0111 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)B + 1	CF
SUB*	@HL	0010 0111 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)B + 1	CF
ADN	Rx	0010 1000 0XXX XXXX	(AC)	← (Rx) + (AC)	
ADN	@HL	0010 1000 1000 0000	(AC)	← (R@HL) + (AC)	
ADN*	Rx	0010 1001 0XXX XXXX	(AC),(Rx)	← (Rx) + (AC)	
ADN*	@HL	0010 1001 1000 0000	(AC),(R@HL)	← (R@HL) + (AC)	
AND	Rx	0010 1010 0XXX XXXX	(AC)	← (Rx) AND (AC)	
AND	@HL	0010 1010 1000 0000	(AC)	← (R@HL) AND (AC)	
AND*	Rx	0010 1011 0XXX XXXX	(AC),(Rx)	← (Rx) AND (AC)	
AND*	@HL	0010 1011 1000 0000	(AC),(R@HL)	← (R@HL) AND (AC)	
EOR	Rx	0010 1100 0XXX XXXX	(AC)	← (Rx) EOR (AC)	
EOR	@HL	0010 1100 1000 0000	(AC)	← (R@HL) EOR (AC)	
EOR*	Rx	0010 1101 0XXX XXXX	(AC),(Rx)	← (Rx) EOR (AC)	
EOR*	@HL	0010 1101 1000 0000	(AC),(R@HL)	← (R@HL) EOR (AC)	
OR	Rx	0010 1110 0XXX XXXX	(AC)	← (Rx) OR (AC)	
OR	@HL	0010 1110 1000 0000	(AC)	← (R@HL) OR (AC)	

Instruction		Machine Code	Function		Flag/Remark
OR*	Rx	0010 1111 0XXX XXXX	(AC),(Rx)	← (Rx) OR (AC)	
OR*	@HL	0010 1111 1000 0000	(AC),(R@HL)	← (R@HL) OR (AC)	
ADCI	Ry,D	0011 0000 DDDD YYYY	(AC)	← (Ry) + D + CF	CF
ADCI*	Ry,D	0011 0001 DDDD YYYY	(AC),(Ry)	← (Ry) + D + CF	CF
SBCI	Ry,D	0011 0010 DDDD YYYY	(AC)	← (Ry) + DB + CF	CF
SBCI*	Ry,D	0011 0011 DDDD YYYY	(AC),(Ry)	← (Ry) + DB + CF	CF
ADDI	Ry,D	0011 0100 DDDD YYYY	(AC)	← (Ry) + D	CF
ADDI*	Ry,D	0011 0101 DDDD YYYY	(AC),(Ry)	← (Ry) + D	CF
SUBI	Ry,D	0011 0110 DDDD YYYY	(AC)	← (Ry) + DB + 1	CF
SUBI*	Ry,D	0011 0111 DDDD YYYY	(AC),(Ry)	← (Ry) + DB + 1	CF
ADNI	Ry,D	0011 1000 DDDD YYYY	(AC)	← (Ry) + D	
ADNI*	Ry,D	0011 1001 DDDD YYYY	(AC),(Ry)	← (Ry) + D	
ANDI	Ry,D	0011 1010 DDDD YYYY	(AC)	← (Ry) AND D	
ANDI*	Ry,D	0011 1011 DDDD YYYY	(AC),(Ry)	← (Ry) AND D	
EORI	Ry,D	0011 1100 DDDD YYYY	(AC)	← (Ry) EOR D	
EORI*	Ry,D	0011 1101 DDDD YYYY	(AC),(Ry)	← (Ry) EOR D	
ORI	Ry,D	0011 1110 DDDD YYYY	(AC)	← (Ry) OR D	
ORI*	Ry,D	0011 1111 DDDD YYYY	(AC),(Ry)	← (Ry) OR D	
INC*	Rx	0100 0000 0XXX XXXX	(AC),(Rx)	← (Rx) + 1	CF
INC*	@HL	0100 0000 1000 0000	(AC),(R@HL)	← (R@HL) + 1	CF
DEC*	Rx	0100 0001 0XXX XXXX	(AC),(Rx)	← (Rx) - 1	CF
DEC*	@HL	0100 0001 1000 0000	(AC),(R@HL)	← (R@HL) - 1	CF
IPA	Rx	0100 0010 0XXX XXXX	(AC),(Rx)	← (IOA)	
IPB	Rx	0100 0100 0XXX XXXX	(AC),(Rx)	← (IOB)	
IPC	Rx	0100 0111 0XXX XXXX	(AC),(Rx)	← (IOC)	
MAF	Rx	0100 1010 0XXX XXXX	(AC),(Rx)	← STS1	B3 : CF B2 : ZERO B1 : (No use) B0 : (No use)
MSB	Rx	0100 1011 0XXX XXXX	(AC),(Rx)	← STS2	B3 : (No use) B2 : SCF2(HRx) B1 : SCF1(CPT) B0 : BCF
MSC	Rx	0100 1100 0XXX XXXX	(AC),(Rx)	← STS3	B3 : SCF7(PDV) B2 : PH15 B1 : SCF5(TM1) B0 : SCF4(INT)
MSD	Rx	0100 1110 0XXX XXXX	(AC),(Rx)	← STS4	B3 : (No use) B2 : (No use) B1 : (No use) B0 : CSF
SR0	Rx	0101 0000 0XXX XXXX	(AC)n, (Rx)n (AC)3, (Rx)3	← (Rx)(n+1) ← 0	
SR1	Rx	0101 0001 0XXX XXXX	(AC)n, (Rx)n	← (Rx)(n+1)	

Instruction		Machine Code	Function		Flag/Remark
			(AC)3, (Rx)3	← 1	
SL0	Rx	0101 0010 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx)(n-1) ← 0	
SL1	Rx	0101 0011 0XXX XXXX	(AC)n, (Rx)n (AC)0, (Rx)0	← (Rx)(n-1) ← 1	
DAA		0101 0100 0000 0000	(AC)	← BCD(AC)	CF
DAA*	Rx	0101 0101 0XXX XXXX	(AC),(Rx)	← BCD(AC)	CF
DAA*	@HL	0101 0101 1000 0000	(AC),(R@HL)	← BCD(AC)	CF
DAS		0101 0110 0000 0000	(AC)	← BCD(AC)	CF
DAS*	Rx	0101 0111 0XXX XXXX	(AC),(Rx)	← BCD(AC)	CF
DAS*	@HL	0101 0111 1000 0000	(AC),(R@HL)	← BCD(AC)	CF
LDS	Rx,D	0101 1DDD DXXX XXXX	(AC),(Rx)	← D	
LDH	Rx,@HL	0110 0000 0XXX XXXX	(AC),(Rx)	← H(T@HL)	
LDH*	Rx,@HL	0110 0001 0XXX XXXX	(AC),(Rx) (@HL)	← H(T@HL) ← (@HL) + 1	
LDL	Rx,@HL	0110 0010 0XXX XXXX	(AC),(Rx)	← L(T@HL)	
LDL*	Rx,@HL	0110 0011 0XXX XXXX	(AC),(Rx) (@HL)	← L(T@HL) ← (@HL) + 1	
STA	Rx	0110 1000 0XXX XXXX	(Rx)	← (AC)	
STA	@HL	0110 1000 1000 0000	(R@HL)	← (AC)	
LDA	Rx	0110 1100 0XXX XXXX	(AC)	← (Rx)	
LDA	@HL	0100 1100 1000 0000	(AC)	← (R@HL)	
MRA	Rx	0110 1101 0XXX XXXX	CF	← (Rx)3	
MRW	@HL,Rx	0110 1110 0XXX XXXX	(AC),(R@HL)	← (Rx)	
MWR	Rx,@HL	0110 1111 0XXX XXXX	(AC),(Rx)	← (R@HL)	
MRW	Ry,Rx	0111 0YYY YXXX XXXX	(AC),(Ry)	← (Rx)	
MWR	Rx,Ry	0111 1YYY YXXX XXXX	(AC),(Rx)	← (Ry)	
JB0	X	1000 0XXX XXXX XXXX	PC	← X	if (AC)0 = 1
JB1	X	1000 1XXX XXXX XXXX	PC	← X	if (AC)1 = 1
JB2	X	1001 0XXX XXXX XXXX	PC	← X	if (AC)2 = 1
JB3	X	1001 1XXX XXXX XXXX	PC	← X	if (AC)3 = 1
JNZ	X	1010 0XXX XXXX XXXX	PC	← X	if (AC) ≠ 0
JNC	X	1010 1XXX XXXX XXXX	PC	← X	if CF = 0
JZ	X	1011 0XXX XXXX XXXX	PC	← X	if (AC) = 0
JC	X	1011 1XXX XXXX XXXX	PC	← X	if CF = 1
CALL	X	1100 0XXX XXXX XXXX	STACK (PC)	← (PC) + 1 ← X	
JMP	X	1101 0XXX XXXX XXXX	(PC)	← X	
RTS		1101 1000 0000 0000	(PC)	← STACK	CALL Return
SCC	X	1101 1001 0000 0XXX	X2,1,0=001 X2,1,0=010 X2,1,0=100	: Cch = PH10 : Cch = PH8 : Cch = PH6	
SCA	X	1101 1010 000X 0000	X4	: Enable SEF4	C1-4
SPA	X	1101 1100 0000 XXXX	X3~0	: Set IOA4-1 Output enable	
SPB	X	1101 1101 000X XXXX	X4 X3~0	: Set IOC4-1 Pull-Low : Set IOB4-1 Output enable	
SPC	X	1101 1110 000X XXXX	X4 X3-0	: Set IOC4-1 Pull-Low / Low-Level-Hold : Set IOC4-1 Output enable	

Instruction		Machine Code	Function		Flag/Remark
TMS	Rx	1110 0000 0XXX XXXX	Timer1	← (Rx) & (AC)	
TMS	@HL	1110 0001 0000 0000	Timer1	← (T@HL)	
TMSX	X	1110 0010 XXXX XXXX	X7,6 = 10 X7,6 = 01 X7,6 = 00 X5~0	: Ctm = PH15 : Ctm = PH3 : Ctm = PH9 : Set Timer1 Value	
SHE	X	1110 1000 0XXX XXX0	X3 X2 X1	: Enable HEF3 : Enable HEF2 : Enable HEF1	PDV INT TMR1
SIE*	X	1110 1001 0XXX XXXX	X3 X2 X1 X0	: Enable IEF3 : Enable IEF2 : Enable IEF1 : Enable IEF0	PDV INT TMR1 CPT
PLC	X	1110 101X 0XXX XXXX	X8 X3-0	: Reset PH15~11 : Reset HRF3-0	
SRE	X	1110 1101 X0XX 0000	X5 X4	: Enable SRF5 : Enable SRF4	SRF5 (INT) SRF4 (C Port)
FAST		1110 1110 0000 0000	SCLK	: High Speed Clock	
SLOW		1110 1111 0000 0000	SCLK	: Low Speed Clock	
SF	X	1111 0000 X00X XXXX	X7 X1 X0	: Reload 1 Set : BCF Set : CF Set	RL1 BCF CF
RF	X	1111 0100 X00X 0XXX	X7 X1 X0	:Reload 1 Reset : BCF Reset : CF Reset	RL1 BCF CF
SF2	X	1111 1000 0000 XXXX	X3 X2	: Enable INT strong Pull-low : Close all Segments	INTPL RSOFF
RF2	X	1111 1001 0000 XXXX	X3 X2	: Disable INT strong Pull-low : Release Segments	INTPL RSOFF
ALM	X	1111 101X XXXX XXXX	X8,7,6=100 X8,7,6=011 X8,7,6=010 X8,7,6=001 X8,7,6=000 X5~0	: DC1 : PH3 : PH4 : PH5 : DC0 ← PH15~10	
HALT		1111 1110 0000 0000	Halt Operation		
STOP		1111 1111 0000 0000	Stop Operation		

Appendix B -Symbol Description

Symbol	Description	Symbol	Description
( )	Content of Register	PDV	Pre-Divider
AC	Accumulator	STACK	Content of stack
(AC)n	Content of Accumulator (bit n)	TM1	Timer 1
(AC)B	Complement of content of Accumulator	D	Immediate Data
X	Address of program or control data	(D)B	Complement of Immediate Data
Rx	Address X of data RAM	PC	Program Counter
(Rx)n	Bit n content of Rx	CF	Carry Flag
Ry	Address Y of working register	ZERO	Zero Flag
R@HL	Address of data RAM specified by @HL	7SEG	7 segment decoder for LCD
BCF	Back-up Flag	BCLK	System clock for instruction
@HL	Generic Index address register	IEFn	Interrupt Enable Flag
(@HL)	Content of generic Index address register	HRFn	HALT Release Flag
(@L)	Content of lowest nibble Index register	HEFn	HALT Release Enable Flag
(@H)	Content of middle nibble Index register	Lz	Address of LCD PLA Latch
(@U)	Content of highest nibble Index register	SRFn	STOP Release Enable Flag
T@HL	Address of Table ROM	SCFn	Start Condition Flag
H(T@HL)	High Nibble content of Table ROM	Cch	Clock Source of Chattering prevention ckt.
L(T@HL)	Low Nibble content of Table ROM	SEFn	Switch Enable Flag
TMR	Timer Overflow Release Flag	CSF	Clock Source Flag
Ctm	Clock Source of Timer		