十速科技股份有限公司 tenx technology inc.	Total page	98
	Doc No	
	Rev.	V1.06

文件名稱	DS-TM32G078_Datasheet			
版次	生效日	ECN No.	制修訂者	修訂內容概要

TM32G078

DATA SHEET

Rev 1.06

Revision history

Revision	Date	Changes
V0.10	2023/04/18	Initial release.
V0.11	2023/10/24	Section 5.3.16/17 adc/dac test result added.
V0.12	2023/12/20	Section 5.3 other modules test result added.
V0.13	2024/1/5	Section 5.3 updated.
V0.14	2024/1/10	1. Remove “boot from sram” in Section 3.2.1. 2. Section 3.4 description modified. 3. Section 5.3 updated. 4. Section 4 updated.
V0.15	2024/2/29	1. Modify some registers and bits’ name according to Reference Manual. 2. Section 6.1 “LQFP64-7x7mm” modified. 3. Section 7 Microcontroller’s naming rule updated. 4. Remove MPU related in Section 3.1. 5. Add PA4/PC0/PC1/PC3’s usage tips in Section 4.2 6. Add three IO types’ definition in Section 3.7.2
V1.00	2024/4/26	1.Modify Bytes to bytes
V1.01	2024/5/17	1. Delete descriptions about the usage of RCC_CR.HSEX2S 2. Modify OPA to OPAMP 3. Modify PMU to PWR 4. Remove “except for Standby mode” in Section 3.23.1
V1.02	2024/6/14	1. Modify R_{AIN} and R_{AOUT}’s unit into Ω in Section 5.3.15 2. File standardization.
V1.03	2024/9/11	1. Modify layout format errors. 2. Modify test’s accuracy in Section 5. 3. Add LQFP80 package information.
V1.04	2024/11/19	1. Adjust file publishment. 2. Modify additional functions in section4
V1.05	2025/2/5	1. Delete content TM32G0788BF related.
V1.06	2025/02/24	1. Modify Section 6 2. Modify Table 2-1, and move it to the above of the doc.

Contents

TM32G078 family device features and peripheral counts

Peripheral		TM32G07889L	TM32G0788AL
CPU		Cortex-M0+	
Max. CPU frequency		48MHz	
Flash (Kbyte)		256	256
SRAM (Kbyte)		32	32
Timers	Advanced control	1(16-bit)	
	General-purpose	3(16-bit)	
	Basic	3(16-bit)	
	Low-power	1(16-bit)	
	SysTick	1	
	Watchdog	2	
Comm. interfaces	SPI	2	
	I℃	2	
	USART	3	
	LPUART	1	
RTC		YES	
CRC		YES	
HDIV		YES	
GPIOs		46	62
12-bit ADC channels		42 ext. + 3 int.	55 ext. + 3 int.
12-bit DAC channels		4	4
Analog comparators		4	4
Operational amplifier		3	4
PLA（Programble Logic Array）		4	4
LCD		8COM*24SEG	8COM*24SEG
LED		Dot: 7*8	Dot: 7*8
		Matrix: 8*8	Matrix: 8*8
Touch key		31	42
Operating voltage		2.2~5.5V	2.2~5.5V
Operating temperature		-40 to 105℃	-40 to 105℃
Number of pins		48	64
Package		LQFP	LQFP
Shipment method		Tray Pack	Tray Pack
Pitch		0.5BSC	0.4BSC

1 Introduction

The TM32G078 mainstream microcontrollers are based on high-performance ARM®Cortex®M0+ 32-bit RISC core operating at up to 48 MHz frequency. High anti-interference ability, and able to operate with supply voltages from 2.2V to 5.5V, large-capacity memory and rich peripherals are also involved.

The devices incorporate high-speed embedded memories (up to 256 Kbytes of Flash program memory with read protection, write protection, proprietary code protection, and securable area, and 32 Kbytes of SRAM), 8-level Brown-Out Reset (BOR), 16-level Programmable Voltage Detect (PVD), Smart Analog Combo (SAC), 3 Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) and one Low-Power UART (LPUART), one advanced-control timer, 3 general-purpose timers, 3 basic timers and one low-power timer, Real-time Clock (RTC), one 12-bit ADC (1.0 MSps) with multiple channels, high sensitive touch circuit, LCD/LED circuit, 2 SPIs, 2 I2Cs, Hardware coprocess Divider (HDIV) and CRC, multiple channels DMA and two Watch Dogs (IWDG/WWDG). Offering a high level of integration, they are suitable for a wide range of applications in consumer, industrial and appliance domains and ready for the Internet of Things (IoT) solutions.

2 Description

2.1 Features

- Core: Arm®32-bit Cortex®-M0+ CPU, frequency up to 48MHz
- Reset and power management
  - Peripherals can switch off/on independently.
  - Programmable voltage detector (PVD) and Programmable Brownout reset (BOR)
  - Low-power modes(Stop): CPU stopped, high frequency clock shutdown, part of peripherals continues to operate, PVD enable to wakeup mcu, main regulator is in standby mode.
  - Low-power modes(Sleep): CPU stopped, all peripherals are working, system clock keeps running.
  - Low speed work mode: CPU and all peripherals are working while high frequency clock is closed.
  - Normal speed work mode: CPU and all peripherals are working while high frequency clock is opened.
- Memories
  - 32 Kbytes of SRAM.
  - 6 Kbytes NVR area.
  - 0~16 Kbytes configurable system area.
  - Up to 252 Kbytes of Flash memory with protection and securable area.
- Clock management
  - Crystal oscillator(4~24MHz)
  - Crystal oscillator(32.768KHz)
  - Internal high frequency RC(18MHz)
  - Internal median frequency RC(3.686MHz)
  - Internal low frequency RC(32KHz)
  - PLL(8~48MHz)
- High sensitive touch circute
  - Up to 42 channels touch key detect.
  - Low-power consumption supported.
- Timer
  - One 16-bit timer for advanced motor control, with 3-channel complementary PWM output, dead zone protection.
  - Three 16-bit general-purpose timers, with functions of input capture/output compare function, PWM output and counter.
  - Three 16-bit basic timers.
  - One 16-bit low-power timer.
  - One 24-bit SysTicker timer.
- Communication interfaces
  - Three USARTs with master/slave synchronous SPI, IrDA capability and wakeup feature; one support auto baudrate detection.
  - One low-power UART
  - Two SPIs
  - Two I2Cs
- 32-bit Hardware Divider (HDIV)
- CRC calculation unit for 16/32 bit data.
- 4-channel DMA controller with flexible mapping, up to 26 requests.
- Independt Watchdog (IWDG) and Window Watchdog (WWDG)
- One 12-bit (1Msps) SAR ADC.
- Two 12-bit DACs each with two channels, four fast low-power analog comparators (COMP) and up to four operational amplifiers (OPAMP).
- LED
  - Support matrix arrangement including 8×8.
  - Support dot arrangement including 7×8, 6×7, 5×6, 4×5
  - Support constant current mode.
- LCD
  - Support 8 Coms*24 Segs, 4 Coms*28 Segs
  - Support duty including 1/4, 1/5, 1/6 and 1/8

- Calendar RTC with alarm and periodic wakeup from Stop/Sleep.
- IR output supported.
- 1 PLA including 4 Programmable Logic Unit (PLU)
- Development support: serial wire debug (SWD)
- Support bias including 1/3
- Operation condition: -40°C to 105°C operating temperature, 2.2V to 5.5V voltage range.
- Package: LQFP64 7mm*7mm, LQFP48

3 Functional overview

3.1 Arm®Cortex®-M0+ core

3.1.1 Introduction

The Cortex-M0+ is an entry-level 32-bit Arm Cortex processor designed for a broad range of embedded applications.

3.1.2 Main features

It offers significant benefits to developers, including:

- a simple architecture, easy to learn and program
- ultra-low power, energy-efficient operation
- excellent code density
- deterministic, high-performance interrupt handling
- upward compatibility with Cortex-M processor family

The Cortex-M0+ processor is built on a highly area- and power-optimized 32-bit core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex-M0+ processor provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

Owing to embedded Arm core, the TM32G078 devices are compatible with Arm tools and software.

The Cortex-M0+ is tightly coupled with a nested vectored interrupt controller (NVIC) described in Section 3.12

3.2 Boot modes

3.2.1 Introduction

At startup, the boot pin and boot selector option bit are used to select one of the two boot options:

- boot from User Flash memory
- boot from System memory

3.2.2 Main features

The boot pin is shared with a standard GPIO and can be enabled through the boot selector option bit. The boot loader is located in System memory. It manages the Flash memory reprogramming through USART on pins PB1/PB6, PA12/PA13 or PD3/PD4, though I2C on pins PA10/PA11 or PA14/PA15, or though SPI on pins PB4/PB5/PB9/PB10 or PD6/PD7/PD8/PD9.

3.3 Embeded SRAM

3.3.1 Introduction

TM32G078 devices have up to 32 Kbytes of embedded SRAM.

3.3.2 Main features

It support read and write operation by byte, halfword and word align. The memory can be read/write-accessed at CPU clock speed, with 0 wait states.

3.4 Embedded Flash Memory

3.4.1 Introduction

Flash controller manager flash memory by AHB bus. Operation including instruction fetch, read, erase and program. It also offers security access mechanism and read/write protection.

3.4.2 Main features

- Up to 252 Kbytes of embedded flash memory available for storing code and data, described as below:
  - Page size: 1 Kbytes
  - NVR area size: 6 Kbytes
  - System memory area size: 0~16 Kbytes configurable (default, 16 Kbytes)
  - User flash size: 236~252 Kbytes configurable (default, 236 Kbytes)
- Read/Write unit using 16-bits or 32-bits.
- Page erase supported.
- 3-level readout protection (RDP): RDP0/RDP1/RDP2
- Proprietary code readout protection (PCROP): Two areas can be selected and configured.
- Write protection (WRP): Two areas can be selected and configured.
- Securable area can be configured.

3.4.3 Flash content

The composition of Flash memory as below:

- User flash: Used for storing user code and data, memory size is configurable from 252 to 236 Kbytes.
- System memory: Used for storing Bootloader and important API, memory size is configurable from 0 to 16 Kbytes. It can be configured by FLASH_OPTR2.BOOTSIZE.
- NVR: The memory size is 6 Kbytes, consists of following content:
  - Engineer Data area: Used for storing information about manufacturer and UID.
  - Option bytes area: Used for storing option bytes.
  - Trim area: Used for storing peripheral's trim parameter.
  - Customer's SN area: Used for customers to store important information such as SN.
  - Customer's Configure area: Userd for customers to store configure data.
  - Customer's Backup area: Used for customers to store backup data.

Flash memory's physical area allocation demonstrated as Figure. 3-4-3.

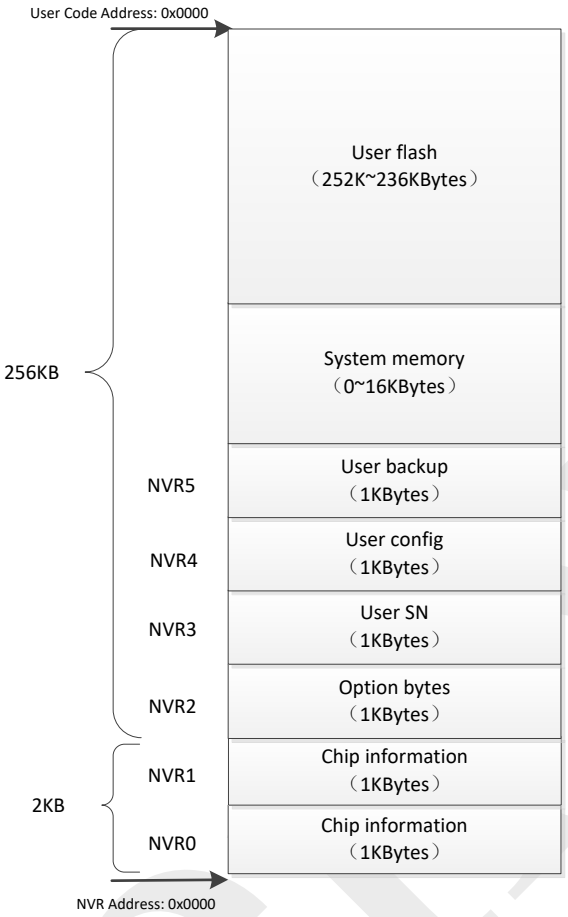


Figure 3-4-3 Flash memory's physical area allocation

3.4.4 Flash security protection mechanism

Flexible protections can be configured thanks to option bytes:

- Readout protection (RDP): protect the whole memory.
- Proprietary code readout protection (PCROP): a part of the Flash memory can be protected against read and write from third parties. The protected area is execute-only: it can only be reached by the TM32 CPU as instruction code, while all other accesses (DMA, debug and CPU data read, write and erase) are strictly prohibited.
- Write protection (WRP): the protected area is protected against erasing and programming.
- Securable area: A part of the Flash memory can be hidden from the application once the code it contains is executed. As soon as the write-once SEC_PROT bit is set, the securable memory cannot be accessed until the system resets. The securable area generally contains the secure boot code to execute only once at boot. This helps to isolate secret code from untrusted application code.

3.5 Power supply management (PWR)

3.5.1 Introduction

There are four power supplies. Each different power supply is provided to specific peripherals:

- V_{DD} = 2.0V to 5.5V. It supplies LCD, HSE, LSE* and regulator (REG/POR). Regulator give power to V_{CORE} domain and V_{core_ana} domain.
- V_{DDA} = 2.0V to 5.5V. It supplies analog peripherials such as ADC, SAC, BGR, ATK, TS (Temperature Sensor), BOR and PVD.
- V_{CORE} = V_{CORE_ANA} = 1.5V. An embedded linear voltage regulator is used to supply the V_{CORE} internal digital power. It supplies Cortex®-M0+, SRAM, digital peripherals and internal RC HSI/LSI/MSI/PLL.

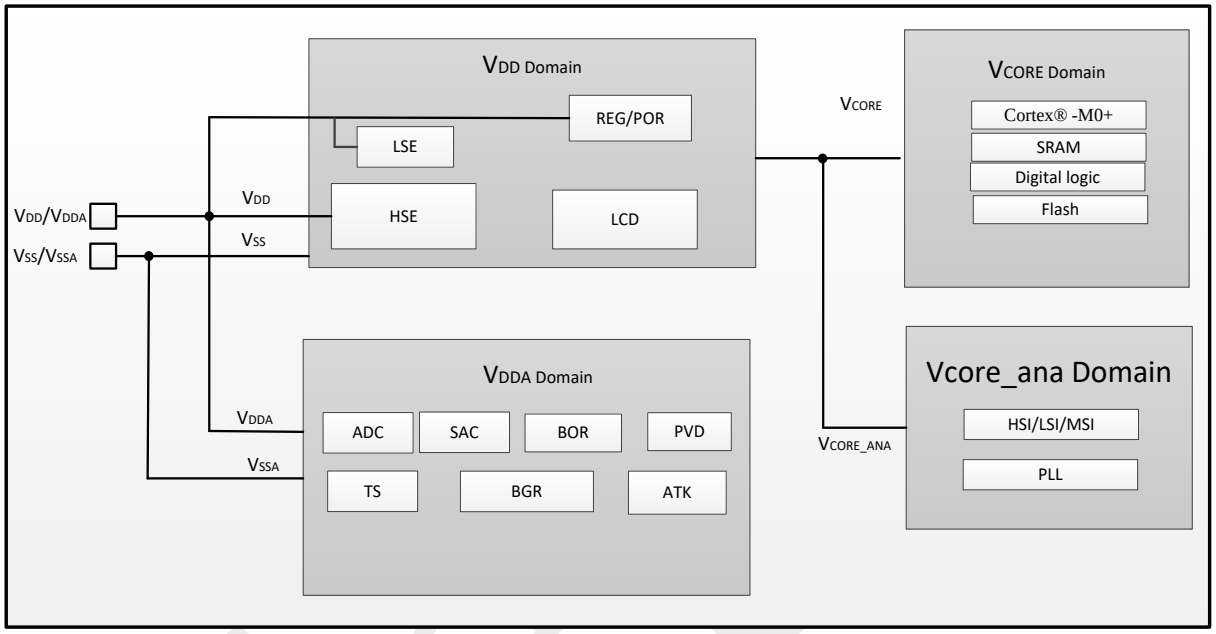


Figure 3-5-1 Power supply overview

Note: IWDG will use LSI.

3.5.2 POR/PDR

The device has an integrated power-on/power-down (POR/PDR) reset active in all power modes.

3.5.3 BOR

Brownout reset (BOR) function allows extra flexibility. It can be enabled and configured through option bytes FLASH_OPTR1, by selecting one of eight thresholds for rising VDD and falling VDD.

3.5.4 PVD

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply or specific IOs' voltage, and compares it to V_{PVD} threshold. It allows generating an interrupt when V_{DD} level crosses the V_{PVD} threshold, selectively while falling, while rising, or while falling and rising. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.5 Low-Power modes

By default, the microcontroller is in Run mode after system or power reset. In Run mode, system clock source uses HSISYS (18 MHz), and it is proper to lower the system clock's frequency or close the unused peripherials' clock to lower the power consumption. It is up to the user to select one of the low-power modes described below:

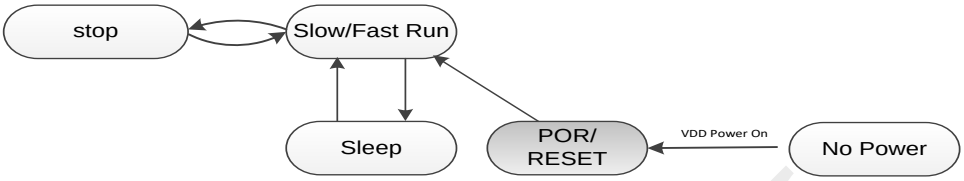


Figure 3-5-5 Low-power modes' conversion flow

- Sleep mode: In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Stop mode: In Stop mode, all clocks in the VCORE domain (such as CPU, digital peripherals) are stopped. The PLL, as well as the HSI/MSI RC oscillator and the HSE crystal oscillator are disabled. The LSE or LSI keep running. Data in SRAM and registers are still maintained.

Some peripherals with wakeup capability can enable the HSI RC during Stop mode, so as to get clock for processing the wakeup event.

3.6 Reset and Clock Controller (RCC)

3.6.1 Reset

The microcontroller's reset including three types: POR/PDR, BOR and system reset.

3.6.2 POR/PDR

POR/PDR have effects as below:

- All registers in V_{CORE} domain (Trim registers included).

3.6.3 System reset

System reset will reset all registers in VCORE domain (Trim and Option bytes' registers are excluded).

System reset will occur as well as one of the listed events fits:

- NRST pin input low level voltage for a certain interval.
- WWDG reset
- IWDG reset
- Software reset by instructions
- Option bytes reload reset
- LOCKUP reset
- BOR

Customers can query the reset flag in RCC_CSR2 to find the reset reason.

NRST: System reset will occur when NRST pin detect the input low level voltage. NRST pin has a built-in pull-up resistor, meanwhile, it integrated a glitch filter which filtered the glitch signal with width below 20us (typical). It is necessary to make sure the low level voltage interval is longer than 20us, to make the NRST reliable.

Software reset: It is proper to set SYSRESETREQ to get the software reset.

3.6.4 Clocks

The clock controller distributes the clocks coming from different oscillators to the core and the peripherals. It also manages clock gating for low-power modes and ensures clock robustness.

- HSI: internal RC clock with high frequency 18MHz.
- MSI: internal RC clock with median frequency 3.686MHz.
- HSE: external oscillator with high frequency 4 to 24MHz.
- LSI: internal RC clock with low frequency 32KHz.
- LSE: external oscillator with low frequency 32.768KHz.

Several prescalers allow the application to configure AHB and APB1/2 domain clock frequencies, 48 MHz at maximum.

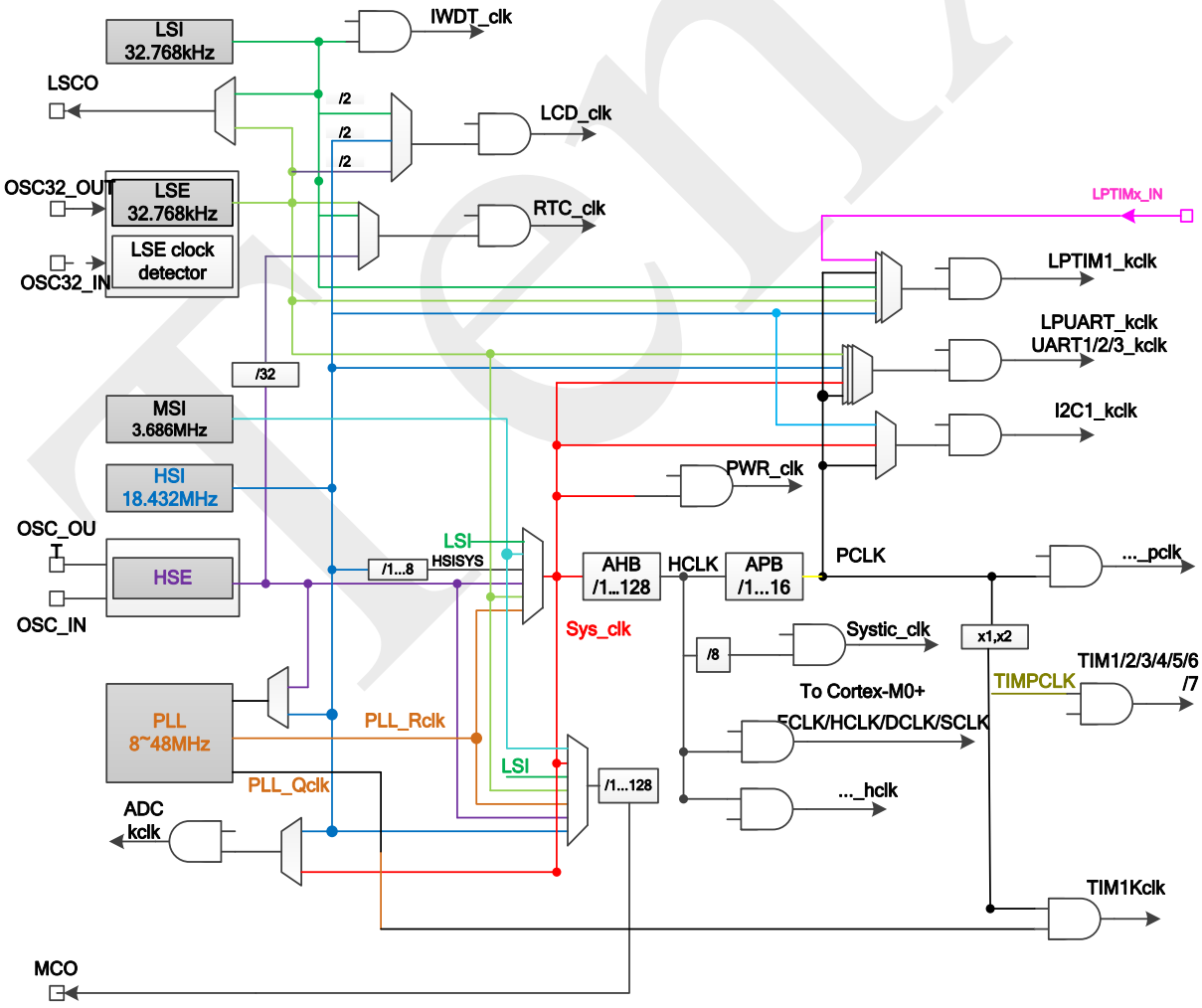


Figure 3-6-4 Clock tree

3.6.5 Peripheral clock sources

Several peripherals have their own clock independent of the system clock.

Table 3-6-5 Peripheral clock sources

Peripheral	Clock sources
IWDG	LSI
ADC	SYSCLK's prescaler 1/2/4, HSI
USART1	PCLK2, LSE, HSI, SYSCLK
LPUART	PCLK1, LSE, HSI, SYSCLK
LPTIM	LSI, LSE, HSI, PCLK1
TIM1	PLLQCLK, PCLK2's frequency or doublling
I2C	PCLK1, HSI, SYSCLK
RTC	LSI, LSE, HSE's prescaler
LCD	LSI's prescaler 2, LSE's prescaler 2 (used in LCD), HSI's prescaler 2 (used in LED)

3.7 General-purpose inputs/outputs (GPIO)

3.7.1 Introduction

Each general-purpose I/O port includes three 32-bit configuration registers (GPOx_MODE, GPOx_TYPE, GPOx_PUDP), two 32-bit data registers (GPOx_IDR, GPOx_ODR), one 32-bit position/reset register (GPOx_BR), and one 32-bit reset register (GPOx_BR); All GPIO include one 32-bit lock register (GPOx_LOCK) and two 32-bit multiplexing function selection registers (GPOx_AFH, GPOx_AFL).

3.7.2 Main features

- GPIO modes
  - Input
  - Output
  - Peripheral alternate function (AF), up to 8 AFs for each I/O.
  - Analog
- With or without pull-up or pull-down.
- Push-pull or open-drain.
- Highly flexible pin multiplexing allows the use of I/O pins as GPIOs or as one of several peripheral functions.
- Bit set and reset register (GPIOx_ BSRR) for bitwise write access to GPIOx_ODR.
- Locking mechanism (GPIOx_LCKR) provided to freeze the I/O port configurations.

3.8 System configuration controller (SYSCFG)

3.8.1 Introduction

The devices feature a set of configuration registers. The main purposes of the system configuration controller

are the following:

- Configuring the IR modulation signal and its output polarity.
- TIM1 break input source control.
- Remapping the memory located at the beginning of the code area.

3.9 Interconnect Matrix

3.9.1 Introduction

Several peripherals have direct connections between them.

This allows autonomous communication and/or synchronization between peripherals, saving CPU resources thus power consumption.

In addition, these hardware connections remove software latency and allow design of predictable systems.

Depending on peripherals, these interconnections can operate in Run, Sleep, Stop modes.

For availability of peripherals on different TM32G078 products, refer to Section 2.

3.9.2 Connection summary

Table 3-9-2 Interconnect matrix (1)

	TIM1	TIM2	TIM3	TIM4	LPTIM	MCO	LSCO	IRTIM	ADC	DMA	DMAMUX	SAC	PLA
TIM1		√	√	√					√			√	√
TIM2	√		√	√					√			√	√
TIM3	√	√		√								√	√
TIM4	√	√	√			√	√	√	√		√	√	√
LPTIM											√	√	√
USART1													√
USART2								√					√
USART3								√					√
SPI1													√
SPI2													√
ADC	√												√
TS									√				
BGR									√			√	
HSE						√							
LSE			√			√	√						
HSI						√							
LSI						√	√						
MSI						√							
PLL						√							

	TIM1	TIM2	TIM3	TIM4	LPTIM	MCO	LSCO	IRTIM	ADC	DMA	DMAMUX	SAC	PLA
MCO													
SYSCLK						√							√
EXTI									√		√		
RTC					√								√
SAC	√		√	√	√								√
SYSERR(2)	√												
DMAMUX										√			
PVD	√												
CSS	√												
LCD											√		

1. √-peripheral interconnected.
2. SYSERR: Cortex®-M0+ LOCKUP.

3.10 Direct memory access controller (DMA)

3.10.1 Introduction

The direct memory access (DMA) controller is a bus master and system peripheral. The DMA is used to perform programmable data transfers between memory-mapped peripherals and/or memories, upon the control of an off-loaded CPU.

DMA has four channels. Each channel is dedicated to managing memory access requests from one or more peripherals. The DMA includes an arbiter for handling the priority between DMA requests.

3.10.2 Main features

- Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-toperipheral data transfers.
- All DMA channels independently configurable.
- Each channel is associated either with a DMA request signal coming from a peripheral, or with a software trigger in memory-to-memory transfers. This configuration is done by software.
- Priority between the requests is programmable by software (4 levels per channel: very high, high, medium, low) and by hardware in case of equality (such as request to channel 1 has priority over request to channel 2).
- Transfer size of source and destination are independent (byte, half-word, word).
- Programmable number of data to be transferred: 0 to 65535.
- Support of transfers from/to peripherals to/from memory with circular buffer management.
- Generation of an interrupt request per channel. Each interrupt request is caused from any of the three DMA events: transfer complete, half transfer, or transfer error.

3.11 DMA request multiplexer (DMAMUX)

3.11.1 Introduction

The DMAMUX request multiplexer enables routing a DMA request line between the peripherals and the DMA controller. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

DMAMUX may also be used as a DMA request generator from programmable events on its input trigger signals.

DMAMUX request multiplexer has four channels, while DMAMUX request generator has two channels.

3.11.2 Main features

- 4-channel programmable DMA request line multiplexer output
- 2-channel DMA request generator
- Per DMA request generator channel:
  - 8 trigger inputs to DMA request generator
  - DMA request counter
  - Event overrun flag for selected DMA request trigger input
- Per DMA request line multiplexer channel output:
  - Several input DMA request lines from peripherals
  - One DMA request line output
  - One event output, for DMA request chaining (channel 0/1 only)
  - DMA request counter (channel 0/1 only)

3.12 Nested vectored interrupt controller (NVIC)

3.12.1 Introduction

The configurable nested vectored interrupt controller is tightly coupled with the core. handles physical line events associated with a non-maskable interrupt (NMI) and maskable interrupts, and Cortex-M0+ exceptions.

All interrupts including the core exceptions are managed by the NVIC.

3.12.2 Main features

- 32 maskable interrupt channels (not including the sixteen Cortex®-M0+ interrupt lines)
- Low-latency exception and interrupt handling
- Implementation of system control registers
- 4 programmable priority levels (“0” as the highest priority)
- Later-arriving higher-priority interrupt processed first

If a higher-priority interrupt event happens while a lower-priority interrupt event occurring just before is waiting for being served, the later-arriving higher-priority interrupt event is served first. Another optimization is called tail-chaining. Upon a return from a higher-priority ISR then start of a pending lower-priority ISR, the unnecessary processor context unstacking and stacking is skipped. This reduces latency and contributes to power efficiency. Any detail information refers to <*Cortex-M0+ Technical Reference Manual*>.

3.13 Extended interrupt/event controller (EXTI)

3.13.1 Introduction

The Extended interrupts and events controller (EXTI) manages the CPU and system wakeup through configurable and direct event inputs (lines). It provides wakeup requests to the power control, and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU an additional event generation block (EVG) is needed to generate the CPU event signal.

The EXTI wakeup requests allow the system to be woken up from Stop modes.

The EXTI controls 26 event lines, including 18 configurable lines and 8 direct lines.

The interrupt request and event request generation can also be used in Run modes. The EXTI also includes the EXTI I/O port mux.

3.13.2 Main features

- System wakeup upon event on any input.
- Configurable events (from I/Os, peripherals not having an associated interrupt pending status bit, or peripherals generating a pulse)
  - Selectable active trigger edge.
  - Independent rising and falling edge interrupt pending status bits.
  - Individual interrupt and event generation mask, used for conditioning the CPU wakeup, interrupt and event generation.
- Direct events (from peripherals having an associated flag and interrupt pending status bit)
  - Fixed rising edge active trigger.
  - No interrupt pending status bit in the EXTI.
  - Individual interrupt and event generation mask for conditioning the CPU wakeup and event generation.
- I/O port selector.

3.14 Hardware Divider (HDIV)

3.14.1 Introduction

HDIV (Hardware Divider) is a coprocessor unit capable of execute 32-bit signed/unsigned integer division automatically.

3.14.2 Main feature

- Able to calculate signed/unsigned integer division.
- Dividend and divisor should be 32-bit integer as input.
- 32-bit integer quotient and remainder will be output as result.
- Including warning flag (divisor is zero) and calculation finished flag.
- Single division operation cost 10 clock cycles.
- Automatically start operation from the divisor is written.
- Return the quotient/remainder result until calculation finished.

3.15 Cyclic redundancy check calculation unit (CRC)

3.15.1 Introduction

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from 8-, 16- or 32-bit data word and a generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

3.15.2 Main features

- Support CRC-16 and CRC-32 individually.
- Uses CRC-16 polynomial: 0x1021
  $X^{16}+X^{12}+X^5+1$
- Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7
  $X^{32}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X+1$
- Both of calculation mode and validation mode are supported.
- Handles 8-,16-, 32-bit data size.
- CRC computation done in 1 AHB clock cycles (HCLK)

3.16 Analog-to-digital converter (ADC)

3.16.1 Introduction

The 12-bit ADC is a successive approximation (SAR) analog-to-digital converter. It has up to 59 multiplexed channels allowing it to measure signals from 56 external and 3 internal sources. A/D conversion of the various channels can be performed in single, continuous, scan or discontinuous mode. The result of the ADC is stored in a left-aligned or right-aligned 16-bit data register.

The analog watchdog feature allows the application to detect if the input voltage goes outside the user-defined higher or lower thresholds.

3.16.2 Main features

- High performance
  - Programmable sampling time
  - ADC conversion time: 1Msps
  - Self-calibration
  - Data alignment with built-in data coherency
  - DMA support
- Low-power
  - The application can reduce PCLK frequency or an asynchronize clock source for low-power operation while still keeping optimum ADC performance. For example, 1µs conversion time is kept, whatever the PCLK frequency)
  - Wait mode: prevents ADC overrun in applications with low PCLK frequency.
- Analog input channels
  - 56 external analog inputs

- 3 internal analog inputs
  1 channel for internal temperature sensor (VTS).
  1 channel for internal reference voltage (VBGR).
  1 channel for monitoring external 1/4 VCC power supply pin.
- Start-of-conversion can be initiated:
- By software
- By hardware triggers with configurable polarity (timer events or GPIO input events).
- Conversion modes
- Can convert a single channel or can scan a sequence of channels
- Single mode converts selected inputs once per trigger
- Continuous mode converts selected inputs continuously
- Discontinuous mode
- Interrupt generation
- End of conversion
- End of sequence conversion
- Analog watchdog event
- Overrun event
- Analog watchdog
- ADC supply requirements: 2.4 to 5.5 V
- ADC input range: VSSA≤VIN≤VDDA

3.17 Touch key (ATK)

3.17.1 Introduction

Touch key offers a simple and reliable way to implement finger touch detection. ATK peripheral supports up to two groups with 21 channels in each groups touch detection during the operation.

3.17.2 Main features

- High sensitive detection.
- Strong anti-interference ability.
- Up to 42 channels touch key detection.
- Low-power

3.18 Smart Analog Combo (SAC)

3.18.1 Introduction

The microcontroller SAC build-in four 12-bit DACs, four fast low-power analog comparators (COMP) and up to four operational amplifiers (OPAMP). These three modules can be used individually or combined.

The comparators can be used for a variety of functions including:

- Wakeup from low-power mode triggered by an analog signal.
- Analog signal conditioning.

- Cycle-by-cycle current control loop when combined with a PWM output from a timer.

OPAMP can be configured as positive/negative input with different pga gain setting. It also can use external resistance to cascade. OPAMP's input voltage range from 0 to AVCC, output range from 0.1V to AVCC-0.1V.

3.18.2 Main features

- Each comparator has configurable plus and minus inputs used for flexible voltage selection:
  - Multiplexed I/O pins
  - DAC output
  - Internal reference voltage (VBGR) and three submultiple values (1/4, 1/2, 3/4) provided by scaler (buffered voltage divider)
  - Internal reference voltage Vcore.
- COMP has programmable hysteresis
- COMP's outputs can be redirected to an I/O or to timer inputs for triggering:
- Capture event
- Break events for fast PWM shutdowns
- COMP output has digital filter and filter time configurable.
- Each comparator has interrupt generation capability with wakeup from Sleep and Stop modes (through the EXTI controller)
- OPAMP's PGA gain is programmable.
- OPAMP's outputs can connect with COMP inputs.
- OPAMP's inputs can be configurable.

3.19 LCD/LED

3.19.1 Introduction

LCD/LED module can be configured as three modes: LCD mode, LED matrix mode and LED dot mode, and only one mode is available at the same time. LCD controller has up to eight COMs and 28 SEGs, to light up 112(4x28) or 192(8x24) pixels of LCD images. The available number of COMs and SEGs mainly depends on the product package.

Vocabulary	
LCD	Liquid Crystal Display
LED	Light Emitting Diode
Bias	LCD voltage level. Defined as 1/(LCD voltage level number-1)
Duty	LCD duty. Defined as 1/(LCD COM number-1)
Frame	A cycle of LCD period
f_{frame}	Frame number per second

3.19.2 Main features

LCD's main features are described as below.

- Support from 4x28 to 8x24 LCD driver.
- Support duty including 1/4, 1/5, 1/6 and 1/8

- Support bias voltage 1/3
- Up to eight 32-bit data LCD RAM display.
- Eight levels brightness configurable.
- Low-power supported.
- LCD controller can work in Sleep and Stop mode, it also can deactivate to lower the power consumption.
- Build-in inverse feature to lower the power consumption and EMI standard suitable.
- LED's main features are described as below.
- Matrix mode: including 8*8 pixels, 16 pins, up to 64 dots.
- Dot mode: including 7*8, 6*7, 5*6, 4*5 pixels, 8 pins, up to 56 dots.

3.20 Advanced-control timer (TIM1)

3.20.1 Introduction

The advanced-control timer (TIM1) consists of a 16-bit auto-reload counter driven by a programmable prescaler.

It may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The advanced-control (TIM1) and general-purpose (TIM2/3/4) timers are completely independent, and do not share any resources.

3.20.2 Main features

- 16-bit up, down, up/down auto-reload counter.
- 16-bit programmable prescaler allowing dividing (also "on the fly") the counter clock frequency either by any factor between 1 and 65535.
- Up to 6 independent channels for:
- Input Capture (but channels 5 and 6)
- Output Compare
- PWM generation (Edge and Center-aligned Mode)
- One-pulse mode output
- Repeated triggering in one-pulse mode (OPM).
- Complementary outputs with programmable dead-time
- Synchronization circuit to control the timer with external signals and to interconnect several timers together.
- Repetition counter to update the timer registers only after a given number of cycles of the counter.
- 2 break inputs to put the timer's output signals in a safe user selectable configuration.
- Interrupt/DMA generation on the following events:
- Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
- Trigger event (counter start, stop, initialization or count by internal/external trigger)
- Input capture
- Output compare
- Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes.

- Trigger input for external clock or cycle-by-cycle current management
- DMA burst transfer.

Interface with CPU:

- Connected on APB2, 32-bit access only.
- To undefined register bits, the data read out will be 0.

Clock and reset:

- Two clock sources can be selected
- Asynchonize reset and low level voltage effects.

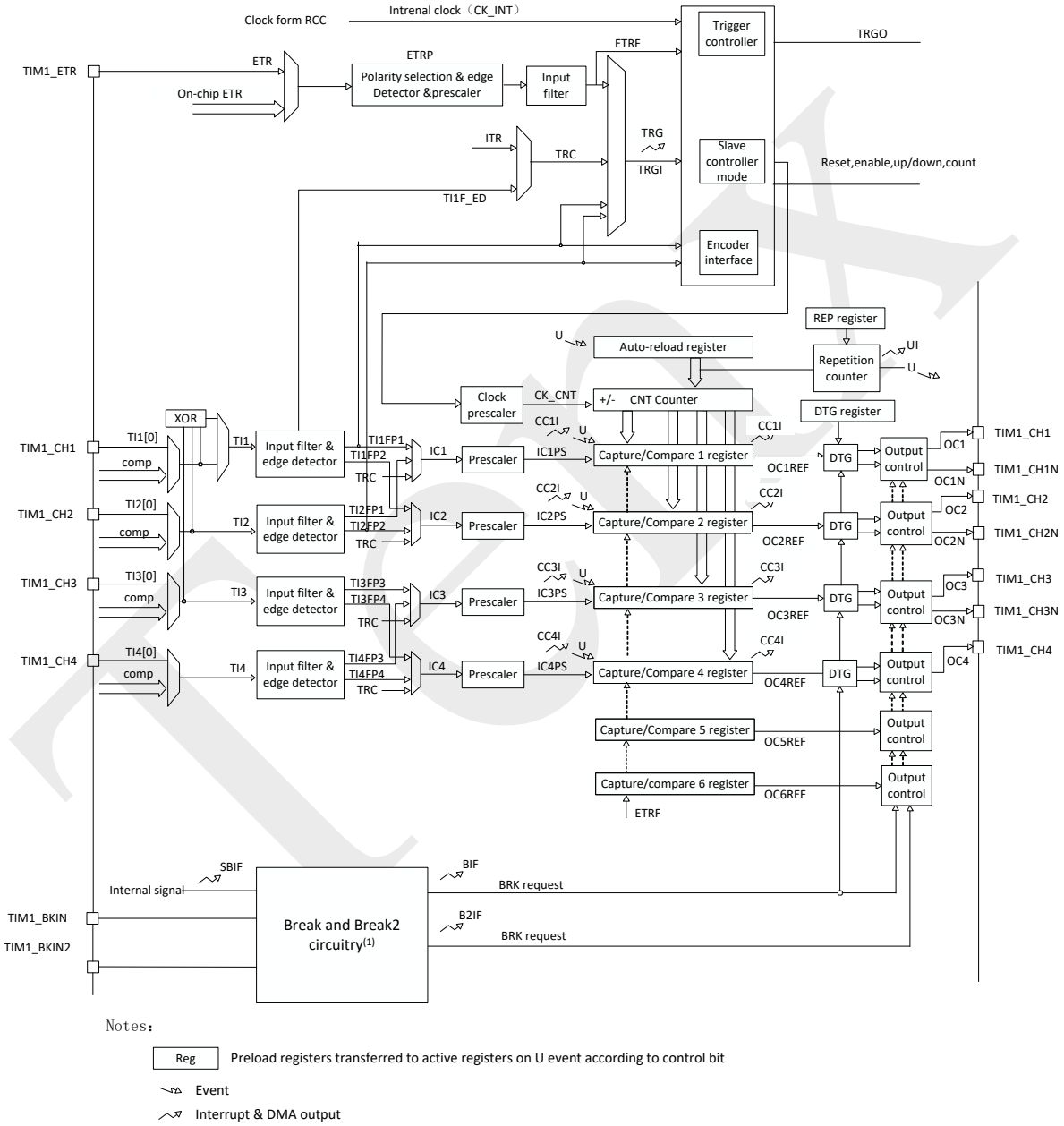


Figure 3-20-2 Advanced-control timer block diagram

3.21 General-purpose timers (TIM2/3/4)

3.21.1 Introduction

The general-purpose timers consist of a 16-bit auto-reload counter driven by a programmable prescaler.

They may be used for a variety of purposes, including measuring the pulse lengths of input signals (input capture) or generating output waveforms (output compare and PWM).

Pulse lengths and waveform periods can be modulated from a few microseconds to several milliseconds using the timer prescaler and the RCC clock controller prescalers.

The timers are completely independent, and do not share any resources.

3.21.2 Main features

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535.
- Up to 6 independent channels for:
  - Input capture
  - Output compare
  - PWM generation (Edge- and Center-aligned modes)
  - One-pulse mode output
- Synchronization circuit to control the timer with external signals and to interconnect several timers.
- Interrupt/DMA generation on the following events:
  - Update: counter overflow/underflow, counter initialization (by software or internal/external trigger)
  - Trigger event (counter start, stop, initialization or count by internal/external trigger)
  - Input capture
  - Output compare

Interface with CPU:

- Connected on APB2, 32-bit access only.
- To undefined register bits, the data read out will be 0.

Clock and reset:

- Two clock sources can be selected
- Asynchonize reset and low level voltage effects.

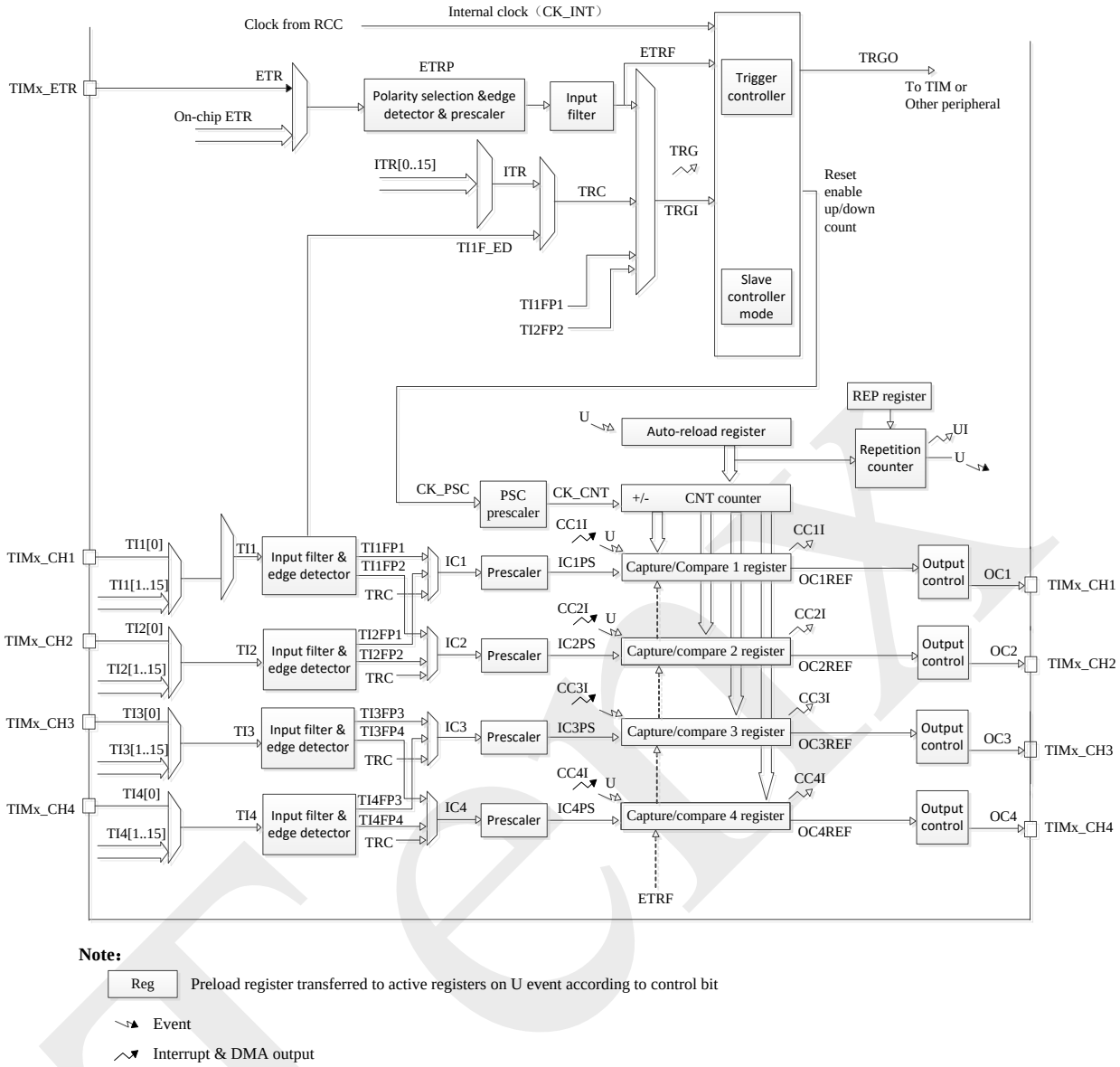


Figure 3-21-2 General-purpose timer block diagram

3.22 Basic timers (TIM5/6/7)

3.22.1 Introduction

The basic timers consist of a 16-bit auto-reload counter driven by a programmable prescaler.

They may be used as generic timers for time base generation but they are also specifically used to drive the analog-to-digital converter (ADC). In fact, the timers are internally connected to the ADC and are able to drive it through their trigger outputs.

The timers are completely independent, and do not share any resources.

3.22.2 Main features

- 16-bit auto-reload upcounter

- 16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535.
- Synchronization circuit to trigger the DAC
- Interrupt/DMA generation on the update event: counter overflow

Interface with CPU:

- Connected on APB1, 32-bit access only.
- To undefined register bits, the data read out will be 0.

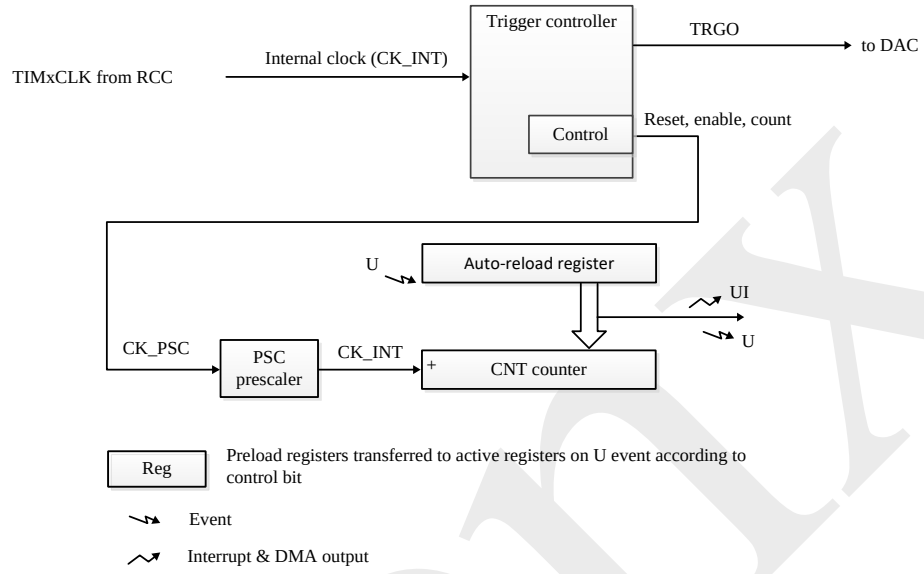


Figure 3-22-2 Basic timer block diagram

3.23 Low-power timer (LPTIM)

3.23.1 Introduction

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. Thanks to its diversity of clock sources, the LPTIM is able to keep running in all power modes. Given its capability to run even with no internal clock source, the LPTIM can be used as a “Pulse Counter” which can be useful in some applications. Also, the LPTIM capability to wake up the system from low-power modes, makes it suitable to realize “Timeout functions” with extremely low power consumption.

The LPTIM introduces a flexible clock scheme that provides the needed functionalities and performance, while minimizing the power consumption.

3.23.2 Main features

- 16 bit upcounter
- 3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Selectable clock

- Internal clock sources: LSE. LSI. HSI or APB1
- External clock source over LPTIM input (working with no embedded oscillator running, used by Pulse Counter application)

- 16 bit ARR autoreload register
- 16 bit compare register
- Continuous/One-shot mode
- Selectable software/hardware input trigger
- 3-bit digital filter prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)
- Programmable Digital Glitch filter
- Configurable output: Pulse, PWM
- Configurable I/O polarity
- Encoder mode

Interface with CPU:

- Connected on APB1, 32-bit access only.
- To undefined register bits, the data read out will be 0.

Clock and reset:

- Two clock sources can be selected
- Asynchonize reset and low level voltage effects.

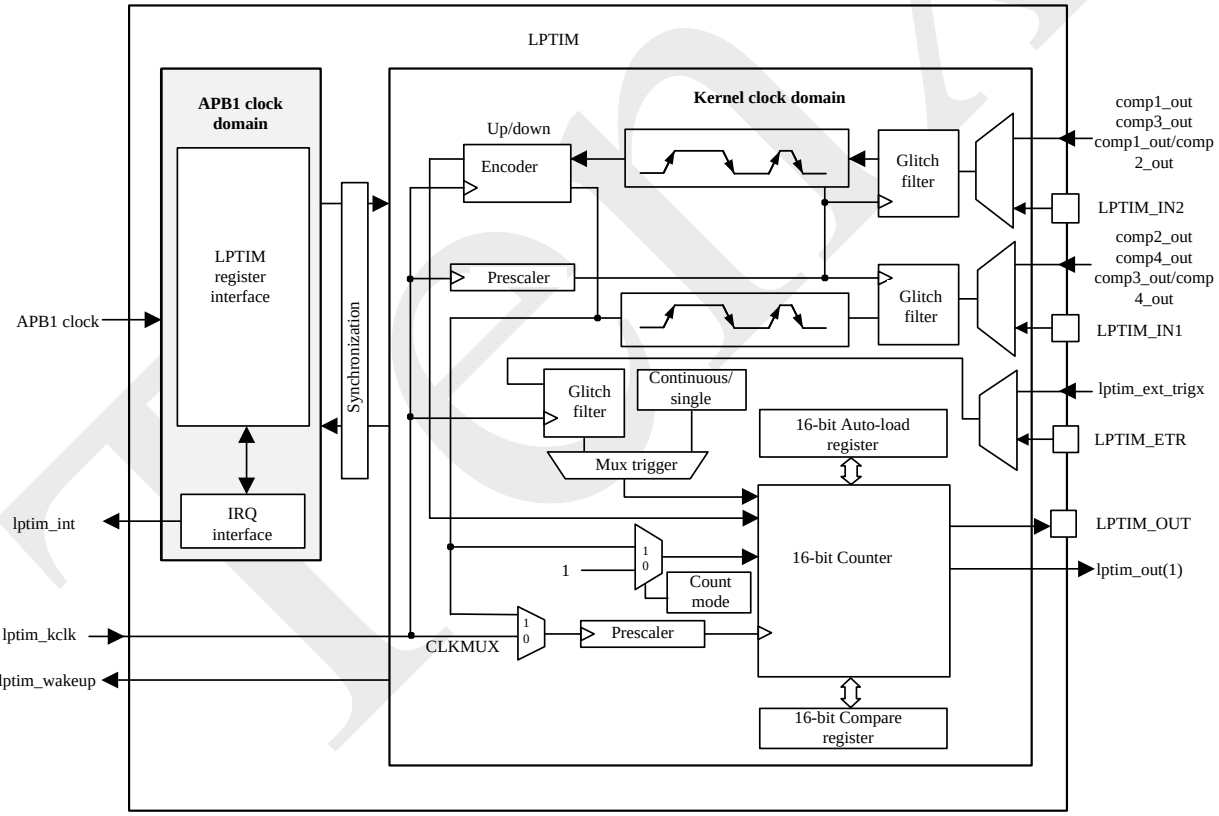


Figure 3-23-2 Low-power timer block diagram

Note: lptim_out is the internal LPTIM output signal that can be connected to internal peripherals.

3.24 SysTick

3.24.1 Introduction

This timer is dedicated to real-time operating systems, but it can also be used as a standard down counter.

3.24.2 Main features

- 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.25 Infrared interface (IRTIM)

3.25.1 Introduction

An infrared interface (IRTIM) for remote control is available on the device. It can be used with an infrared LED to perform remote control functions.

3.25.2 Main features

It uses internal connections with USART2, USART3, TIM3 and TIM4 as shown in Figure 3-25-2.

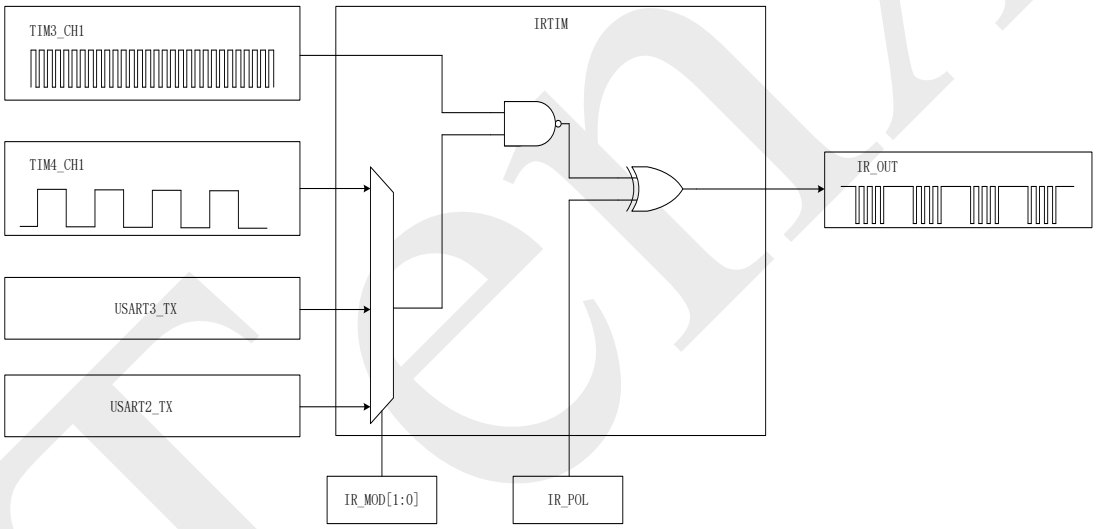


Figure 3-25-2 IRTIM internal hardware connections

All standard IR pulse modulation modes can be obtained by programming the two timer output compare channels.

TIM3 is used to generate the high frequency carrier signal, while TIM4 or alternatively USART2 or USART3 generates the modulation envelope according to the setting of the IR_MOD[1:0] bits in the SYSCFG_CFGR1 register.

The polarity of the output signal from IRTIM is controlled by the IR_POL bit in the SYSCFG_CFGR1 register and could be inverted by setting of this bit.

The infrared function is output on the IR_OUT pin. The activation of this function is done through the GPIOx_AFRx register by enabling the related alternate function bit.

3.26 Independent watchdog (IWDG)

3.26.1 Introduction

The devices feature an embedded watchdog peripheral that offers a combination of high safety level, timing accuracy and flexibility of use. The Independent watchdog peripheral detects and solves malfunctions due to software failure, and triggers system reset when the counter reaches a given timeout value.

The independent watchdog (IWDG) is clocked by its own dedicated low-speed clock (LSI) and thus stays active even if the main clock fails.

3.26.2 Main features

- Free-running downcounter
- Clocked from an independent RC oscillator (can operate in Stop modes)
- Conditional reset
- Reset (if watchdog activated) when the downcounter value becomes lower than 0x000
- Reset (if watchdog activated) if the downcounter is reloaded outside the window
- By option bytes' setting to control IWDG activate/deactivate.

3.27 System window watchdog (WWDG)

3.27.1 Introduction

The system window watchdog (WWDG) is used to detect the occurrence of a software fault, usually generated by external interference or by unforeseen logical conditions, which causes the application program to abandon its normal sequence.

The WWDG clock is prescaled from the APB clock and has a configurable time-window that can be programmed to detect abnormally late or early application behavior.

3.27.2 Main features

- Programmable free-running down-counter
- Conditional reset
- Reset (if watchdog activated) when the down-counter value becomes lower than 0x40
- Reset (if watchdog activated) if the down-counter is reloaded outside the window
- Early wakeup interrupt (EWI): triggered (if enabled and the watchdog activated) when the down-counter is equal to 0x40.

3.28 Inter-integrated circuit interface (I2C)

3.28.1 Introduction

The I2C (inter-integrated circuit) bus interface handles communications between the microcontroller and the serial I2C bus. It provides multimaster capability, and controls all I2C bus-specific sequencing, protocol, arbitration and timing. It supports Standard-mode (Sm), Fast-mode (Fm) and Fast-mode Plus (Fm+).

3.28.2 Main features

- I2C bus specification rev03 compatibility:
- Slave and master modes
- Multimaster capability
- Standard-mode (up to 100 KHz)
- Fast-mode (up to 400 KHz)
- Fast-mode Plus (up to 1 MHz)
- 7-bit and 10-bit addressing mode
- Multiple 7-bit slave addresses (2 addresses, 1 with configurable mask)
- All 7-bit addresses acknowledge mode
- General call
- Programmable setup and hold times
- Optional clock stretching
- Easy to use event management
- Software reset
- 1-byte buffer with DMA capability
- Programmable analog and digital noise filters

  I2C1 have following features while I2C2 haven't.
- Independent clock
- Wakeup from Stop mode

3.29 Universal synchronous receiver transmitter (USART)

3.29.1 Introduction

The USART offers a flexible means to perform Full-duplex data exchange with external equipments requiring an industry standard NRZ asynchronous serial data format. A very wide range of baud rates can be achieved through a fractional baud rate generator.

The USART supports both synchronous one-way and Half-Duplex Single-wire communications, as well as IrDA (infrared data association) SIR ENDEC specifications, and Modem operations (CTS/RTS). Multiprocessor communications are also supported.

High-speed data communications are possible by using the DMA (direct memory access) for multibuffer configuration.

3.29.2 Main features

- Full-duplex asynchronous communication
- NRZ standard format (mark/space)
- Configurable oversampling method by 16 or 8 to achieve the best compromise between speed and clock tolerance
- Baud rate generator systems
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK
- Separate enable bits for transmitter and receiver

- Swappable Tx/Rx pin configuration
- Separate signal polarity control for transmission and reception
- Two internal FIFOs for transmit and receive data
- Auto baud rate detection
- Programmable data word length (7, 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (0.5, 1, 1.5 or 2 stop bits)
- Parity control configure: odd, even, none parity.
- Continuous communications using DMA
- Synchronous master/slave mode and clock output/input for synchronous communications
- Single-wire Half-duplex communications
- Hardware flow control(CTS/RTS) for modem and RS-485 transceiver
- Multiprocessor communications: wakeup from Mute mode by idle line detection or address mark detection

3.30 Low-power universal asynchronous receiver transmitter (LPUART)

3.30.1 Introduction

The LPUART is an UART which enables bidirectional UART communications with a limited power consumption. Only 32.768 KHz LSE clock is required to enable UART communications up to 9600 baud/s. Higher baud rates can be reached when the LPUART is clocked by clock sources different from the LSE clock.

Even when the device is in low-power mode, the LPUART can wait for an incoming UART frame while having an extremely low energy consumption. The LPUART includes all necessary hardware support to make asynchronous serial communications possible with minimum power consumption.

It supports Half-Duplex Single-wire communications and modem operations (CTS/RTS).

It also supports multiprocessor communications.

DMA (direct memory access) can be used for data transmission/reception.

3.30.2 Main features

- Full-duplex asynchronous communications
- NRZ standard format (mark/space)
- Programmable baud rate
- From 300 baud/s to 9600 baud/s using a 32.768 KHz clock source.
- Dual clock domain with dedicated kernel clock for peripherals independent from PCLK
- Two internal FIFOs to transmit and receive data
- Programmable data word length (7 or 8 or 9 bits)
- Programmable data order with MSB-first or LSB-first shifting
- Configurable stop bits (1 or 2 stop bits)
- Single-wire Half-duplex communications
- Continuous communications using DMA
- Separate enable bits for transmitter and receiver
- Separate signal polarity control for transmission and reception
- Communication control/Error detection flags

- Transfer detection flags:
- Receive buffer full
- Transmit buffer empty
- Busy and end of transmission flags
- Parity control:
- Transmits parity bit
- Checks parity of received data byte
- Four error detection flags:
- Overrun error
- Noise detection
- Frame error
- Parity error
- Interrupt sources with flags
- Hardware flow control (CTS/RTS) for modem and RS-485 transceiver
- Multiprocessor communications: wakeup from Mute mode by idle line detection or address mark detection

3.31 Serial peripheral interface (SPI)

3.31.1 Introduction

The serial peripheral interface (SPI) protocol supports half-duplex, full-duplex and simplex synchronous, serial communication with external devices. The interface can be configured as master and in this case it provides the communication clock (SCK) to the external slave device. The interface is also capable of operating in multimaster configuration.

3.31.2 Main features

- Master or slave operation
- Multimaster mode capability
- Full-duplex synchronous transfers on four lines (NSS, SCK, MISO and MOSI).
- Frame size is 8bit.
- 7 master mode baud rate prescalers up to fPCLK/8, maximum baudrate is 6.25Mbps.
- Slave mode frequency up to fPCLK/8, maximum baudrate is 6.25Mbps.
- Programmable clock polarity and phase
- Programmable data order with MSB-first or LSB-first shifting
- Error events type to trigger interrupt: master mode conflict, data overrun, slave fault and slave
- Interrupt generated by error events: Master mode fault, overrun error, slave mode fault, underrun error
- Two 32-bit embedded Rx and Tx FIFOs with DMA capability

In SPI TX and RX period, data will be transfered and received in the same time. Four modes with different CPOL/CPHA configure show as Table 3-31-2.

Table 3-31-2 CPOL/CPHA configure

SPI Mode	CPOL	CPHA	Note
Mode 0	0	0	Low level voltage during clock idle, data sample using clock's first edge(rising edge).
Mode 1	0	1	Low level voltage during clock idle, data sample using clock's second edge(falling edge).
Mode 2	1	0	High level voltage during clock idle, data sample using clock's first edge(rising edge).
Mode 3	1	1	High level voltage during clock idle, data sample using clock's second edge(falling edge).

3.32 Real-time clock (RTC)

3.32.1 Introduction

The RTC provides an automatic wakeup to manage all low-power modes.

The real-time clock (RTC) is an independent BCD timer/counter. The RTC provides a timeof-day clock/calendar with programmable alarm interrupts.

As long as the supply voltage remains in the operating range, the RTC never stops, regardless of the device status (Run mode, low-power mode or under reset).

3.32.2 Main features

- Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month
- Programmable alarm
- On-the-fly correction from 1 to 32767 RTC clock pulses, usable for synchronization with a master clock.
- Digital calibration circuit with 0.95 ppm resolution, to compensate for quartz crystal inaccuracy
- 16-bit auto-reload wakeup timer (WUT) for periodic events, with programmable resolution and period
- Multiple clock sources and references:
- A 32.768 KHz external crystal (LSE)
- The internal low-power RC oscillator (LSI, with typical frequency of 32 KHz)
- The high-speed external clock (HSE) divided by 32

When clocked by LSE or LSI, the RTC operates in all low-power modes. All RTC events (Alarm, WakeUp Timer, Timestamp) can generate an interrupt and wake the device up from the low-power modes.

3.33 Programmable Logic Array (PLA)

3.33.1 Introduction

PLA offers customers several programmable logic digital arrays, which can be independently operated without CPU. PLA consists of four indepent programmable logic unit (PLU). They offer customers to do asynchonize and synchronize bool logic operation. Internal and external signals can be used as PLU's input, and

output port can be directly connected to I/O pin or input port.

3.33.2 Main features

- Four programmable logic unit (PLU), connect to pins or internal logic.
- Each unit support 256 different combinational logics (such as AND, OR, XOR and combined logic function), including a clock trigger to meet synchronize operation.
- Each unit can perform operation synchronously or a synchronously.
- Units can be cascaded to do more complicated logic functions.
- PLA can connect with USARTT, SPI or TIMs.
- Able to synchonize or trigger multiple modules such as ADC, DAC or TIMs.
- Asynchonize output can be used as wakeup source to low-power mode.

4 Pinouts, pin description and alternate functions

4.1 Pinouts

The devices housed in two packages with LQFP64 and LQFP48, pinouts described as below

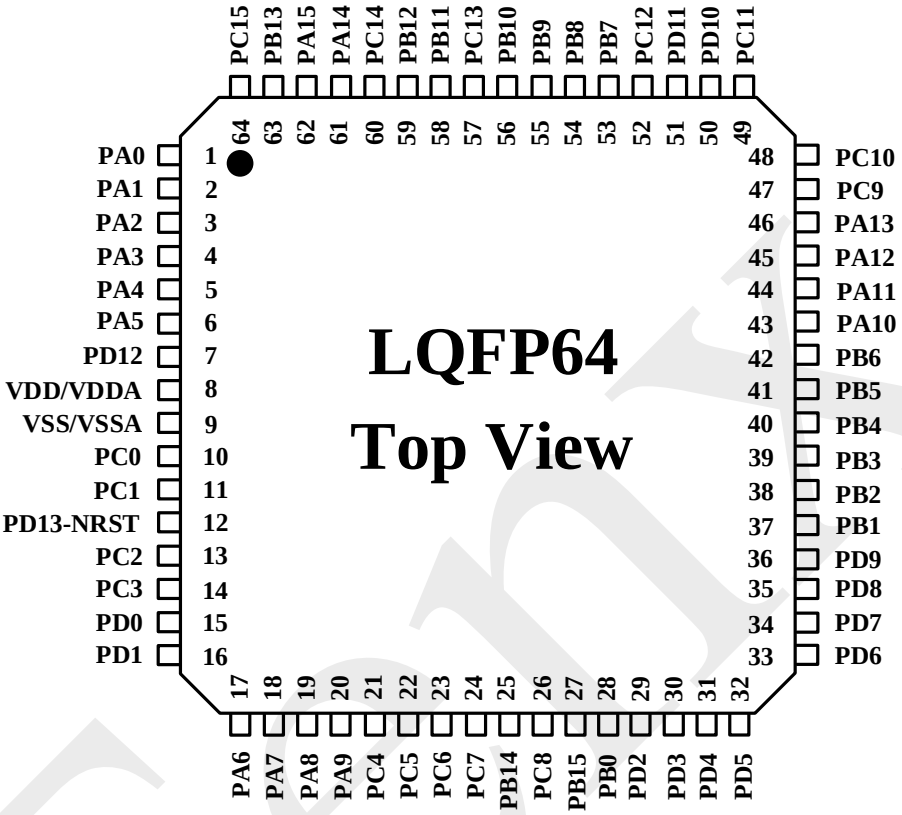


Figure 4-1-1 LQFP64 pinout

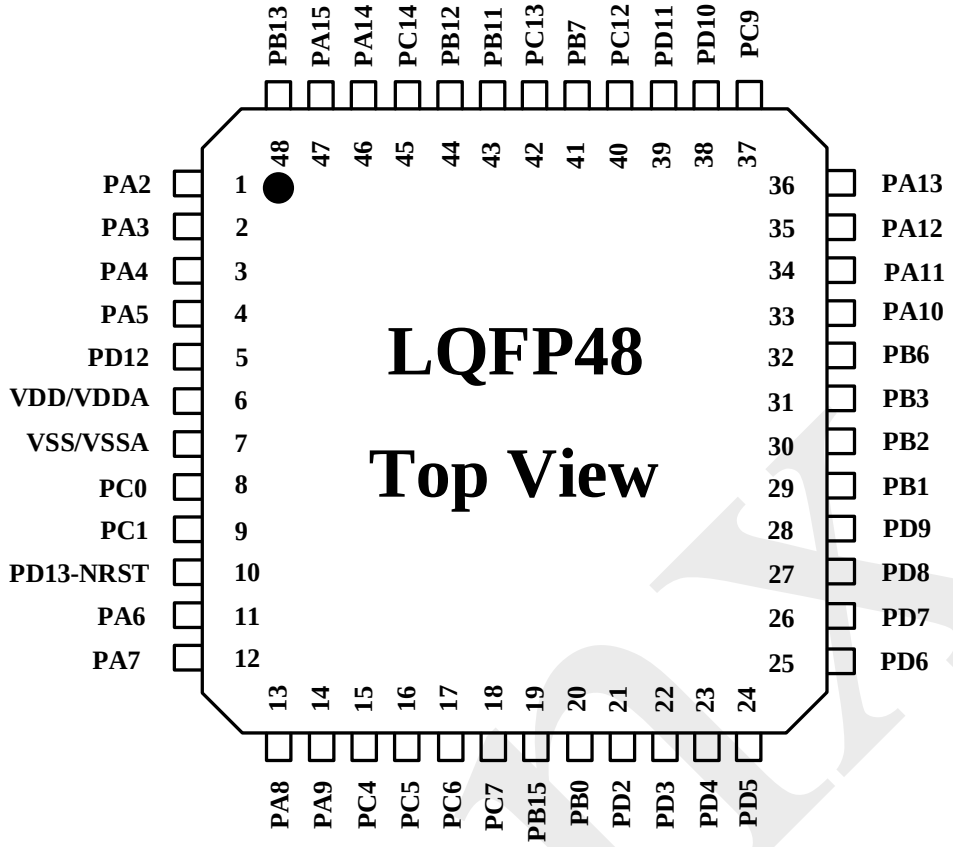


Figure 4-1-2 LQFP48 pinout

4.2 Pin assignment and description

Table 4-2-1 TM32G0788AL and TM32G07889L's Pin assignment and description

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
-	1	PA0	I/O		ATK1_B11,ADC1_00,COMP3_INP1,COMP3_INM1,COM5,SEG25,LED5,LCOM5
-	2	PA1	I/O	USART3_RX,TIM1_CH4	ATK1_B12,ADC1_01,COM4,SEG24,LED4,LCOM4
1	3	PA2	I/O	LPTIM1_IN1	ATK1_B13,ADC1_02,COM3,LED3,LCOM3
2	4	PA3	I/O	TIM1_BKIN1,RTC1_OUT1	ATK1_B14,ADC1_03,COM2,LED2,LCOM2

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
3	5	PA4	I/O	COMP2_OUT,TIM1_BKIN2	ATK1_B15,ADC1_04,COM1,LED1,LCOM1,OSC_IN,OSC32_IN
4	6	PA5	I/O	OSC32_EN,OSC_EN	ATK1_B16,ADC1_05,COMP2_INM1,COM0,LED0,LCOM0,OSC32_OUT
5	7	PD12	I/O		ADC1_55,COMP1_INM1,COMP2_INP1,VREF+
6	8	VDD/VDDA	S		
7	9	VSS/VSSA	S		
8	10	PC0	I/O	PLA1_IN1	ATK1_B17,ADC1_06,OSC_IN
9	11	PC1	I/O	OSC_EN,PLA1_IN2	ATK1_B18,ADC1_07,OSC_OUT
10	12	PD13	I/O	MCO	NRST
-	13	PC2	I/O	LPUART1_RX,LPTIM1_IN1	ATK1_B19,ADC1_08,COMP1_INM2,COMP2_INP2,OSC_IN
-	14	PC3	I/O	LPUART1_TX,LPTIM1_OUT	ATK1_B20,ADC1_09,OSC_OUT
-	15	PD0	I/O	SPI2_MISO,LPTIM1_IN2	DAC2_CH2_OUT0
-	16	PD1	I/O	SPI2_MOSI,LPTIM1_ETR	DAC2_CH1_OUT0
11	17	PA6	I/O	COMP1_OUT,SPI2_SCK,USART2_CTS_NSS,TIM2_CH1_ETR,LPTIM1_OUT,PLA1_IN3	ATK1_A20,ADC1_10,COMP1_INM3,LSEG7
12	18	PA7	I/O	SPI1_SCK,USART2_RTS_DE_CK,TIM2_CH2,EVENTOUT,COMP3_OUT,PLA1_OUT0,PLA1_IN4	ATK1_A19,ADC1_11,COMP1_INP1,DAC1_CH2_OUT0,LSEG6
13	19	PA8	I/O	COMP2_OUT,SPI1_MOSI,USART2_TX,LPUART1_TX,TIM2_CH3,LSCO,PLA1_IN5	ATK1_A18,ADC1_12,COMP2_INM2,DAC1_CH1_OUT0,LSEG5
14	20	PA9	I/O	SPI2_MISO,USART2_RX,LPUART1_RX,TIM2_CH	ATK1_A17,ADC1_13,COMP2_INP3,COMP4_INP9,COMP4_INM9,LSEG4

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
				4,COMP4_OUT,PLA1_OUT1,PLA1_IN6	
15	21	PC4	I/O	SPI1_NSS,SPI2_MOSI,TIM2_CH1,RTC1_OUT1,PLA1_IN7	ATK1_A16,ADC1_14,COMP4_INP8,COMP4_INM8,DAC1_CH1_OUT1,LSEG3,PVD_IN1
16	22	PC5	I/O	SPI1_SCK,USART3_TX,TIM2_CH1_ETR,COMP3_OUT,PLA1_OUT2,PLA1_IN8	ATK1_A15,ADC1_15,COMP4_INP7,COMP4_INM7,DAC1_CH2_OUT1,LSEG2
17	23	PC6	I/O	COMP1_OUT,SPI1_MISO,USART3_CTS_NSS,LPUART1_CTS,TIM1_BKIN1,TIM3_CH1,TIM4_CH1,PLA1_IN9	ATK1_A14,ADC1_16,COMP4_INP6,COMP4_INM6,DAC2_CH1_OUT1,SEG23,LSEG1
18	24	PC7	I/O	COMP2_OUT,SPI1_MOSI,TIM1_CH1N,TIM2_CH1,TIM3_CH2,TIM4_CH4,PLA1_OUT3,PLA1_IN10	ATK1_A13,ADC1_17,COMP4_INP5,COMP4_INM5,DAC2_CH2_OUT1,SEG22,LSEG0
-	25	PB14	I/O	USART1_TX,USART3_TX,TIM2_CH1_ETR	ATK1_A12,ADC1_18,COMP1_INM4,COMP4_INP4,COMP4_INM4,SEG21
-	26	PC8	I/O	USART1_RX,USART3_RX,TIM2_CH2	ADC1_19,COMP1_INP2
19	27	PB15	I/O	COMP1_OUT,SPI1_NSS,USART3_RX,TIM1_CH2N,TIM3_CH3,LPTIM1_OUT,PLA1_IN11	ADC1_20,COMP4_INP3,COMP4_INM3
20	28	PB0	I/O	USART3_RTS_DE_CK,LPUART1_RTS_DE,TIM1_CH3N,TIM2_CH1,TIM3_CH4,EVENTOUT,COMP4_OUT,PLA1_IN12	ATK1_A11,ADC1_21,COMP1_INM5,SEG20
21	29	PD2	I/O	SPI2_MISO,USART3_TX,LPTIM1_OUT,EVENTOUT	ADC1_46,COMP1_INP3,OPAMP4_INP2

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
22	30	PD3	I/O	COMP1_OUT,SPI2_SCK, I2C2_SCL,USART3_TX, LPUART1_RX,TIM2_CH 3	ADC1_47,OPAMP4_INP1
23	31	PD4	I/O	COMP2_OUT,SPI2_MOSI,I 2C2_SDA,USART3_RX,LPU ART1_TX,TIM2_CH4	ADC1_48,COMP1_INP4,COM P2_INM3,OPAMP4_INM1,PVD _IN2
24	32	PD5	I/O	SPI2_NSS,LPUART1_RT S_DE,TIM1_BKIN1,EVE NTOUT	ADC1_49
25	33	PD6	I/O	SPI2_SCK,I2C2_SCL,US ART3_CTS_NSS,LPUAR T1_CTS,TIM1_CH1N,TI M2_CH3,EVENTOUT	COMP1_INP5,COMP2_INM4,P VD_IN3
26	34	PD7	I/O	SPI2_MISO,I2C2_SDA,U SART3_RTS_DE_CK,TI M1_CH2N,EVENTOUT	ADC1_50,OPAMP2_INP2
27	35	PD8	I/O	SPI2_MOSI,TIM1_CH3N, EVENTOUT	OPAMP2_INP1
28	36	PD9	I/O	SPI2_NSS,TIM1_CH1,M CO,EVENTOUT,PLA1_I N13	OPAMP2_INM1
29	37	PB1	I/O	SPI2_MISO,I2C1_SCL,U SART1_TX,TIM1_CH2,M CO,TIM1_CH1N,PLA1_I N14	ATK1_A10,ADC1_22,SEG19
30	38	PB2	I/O	TIM2_CH3,TIM3_CH1,TI M1_CH2,PLA1_IN15	ATK1_A09,ADC1_23,COMP3_ INP10,COMP3_INM10,SEG18
31	39	PB3	I/O	TIM2_CH4,TIM3_CH2,TI M1_CH2N	ADC1_24
-	40	PB4	I/O	SPI1_SCK,USART3_TX, LPTIM1_OUT,TIM1_CH3	ADC1_25
-	41	PB5	I/O	SPI1_NSS,USART3_RX, TIM1_BKIN2,TIM1_CH3 N	ATK1_A08,ADC1_26,SEG17

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
32	42	PB6	I/O	SPI2_MOSI,I2C1_SDA,USART1_RX,TIM1_CH3,EVENTOUT,COMP3_OUT,PLA1_OUT0,PLA1_IN16	ATK1_A07,ADC1_27,COMP4_INP3,COMP4_INM3,SEG16
33	43	PA10	I/O	SPI1_MISO,COMP1_OUT,I2C2_SCL,USART1_CTS_NSS,TIM1_CH4,TIM1_BKIN2,PLA1_IN17	ATK1_A06,ADC1_28,SEG15
34	44	PA11	I/O	SPI1_MOSI,COMP2_OUT,I2C2_SDA,USART1_RTS_DE_CK,TIM1_ETR,PLA1_IN18	ATK1_A05,ADC1_29,OPAMP1_OUT,SEG14
35	45	PA12	I/O	SWDIO,IRTIM1_OUT,EVENTOUT,USART2_RX	ATK1_A04,ADC1_30,COMP3_INP9,COMP3_INM9,OPAMP1_INP2,SEG13
36	46	PA13	I/O	SWCLK,USART2_TX,BOOT0,EVENTOUT	ATK1_A03,ADC1_31,COMP3_INP8,COMP3_INM8,OPAMP1_INP1,SEG12,BOOT0
37	47	PC9	I/O	SPI1_NSS,USART2_RX,USART3_RTS_DE_CK,TIM2_CH1_ETR,EVENTOUT,PLA1_OUT1	ATK1_A02,ADC1_32,DAC1_CH1_OUT2,OPAMP1_INP0,SEG11
-	48	PC10	I/O	TIM1_CH1,TIM3_CH3	ATK1_A01,ADC1_33,OPAMP1_INM1,SEG10
-	49	PC11	I/O	TIM1_CH2,TIM3_CH4	ATK1_A00,ADC1_34,SEG9
38	50	PD10	I/O	SPI2_NSS,TIM4_CH1,EVENTOUT,TIM1_CH3	ADC1_51,COMP1_INP6,COMP2_INM5,OPAMP1_INM0
39	51	PD11	I/O	SPI2_SCK,TIM4_CH4,EVENTOUT	ADC1_52,COMP1_INP7,COMP2_INM6,OPAMP2_OUT
40	52	PC12	I/O	USART3_RTS_DE_CK,TIM1_CH1N,TIM3_ETR	ATK1_B00,ADC1_35,OPAMP2_INP0,SEG8
41	53	PB7	I/O	SPI2_MISO,USART2_CTS_NSS,TIM1_CH2N	ATK1_B01,ADC1_36,COMP3_INP7,COMP3_INM7,COMP4_INP2,COMP4_INM2,OPAMP2_INM0,SEG7
-	54	PB8	I/O	SPI2_MOSI,USART2_RT	ATK1_B02,ADC1_37,COMP3_

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
				S_DE_CK,TIM1_CH3N	INP6,COMP3_INM6,COMP4_INP1,COMP4_INM1,OPAMP3_INP2,SEG6
-	55	PB9	I/O	SPI1_MISO,USART2_TX,TIM1_BKIN1,TIM1_CH1	ATK1_B03,ADC1_38,COMP3_INP5,COMP3_INM5,OPAMP3_INM1,SEG5
-	56	PB10	I/O	SPI1_MOSI,USART2_RX	ATK1_B04,ADC1_39,COMP3_INP4,COMP3_INM4,OPAMP3_INP1,SEG4
42	57	PC13	I/O	SPI1_SCK,USART1_RTS_DE_CK,TIM1_CH2,TIM2_CH2,EVENTOUT,PLA1_OUT2	ATK1_B05,ADC1_40,COMP2_INM7,DAC1_CH2_OUT2,OPAMP3_OUT,SEG3
43	58	PB11	I/O	SPI1_MISO,USART1_CTS_NSS,TIM3_CH1,EVENTOUT,PLA1_OUT3	ATK1_B06,ADC1_41,COMP2_INP4,COMP3_INP3,COMP3_INM3,DAC2_CH1_OUT2,OPAMP3_INP0,SEG2
44	59	PB12	I/O	COMP2_OUT,SPI1_MOSI,TIM3_CH2,TIM4_CH3,LPTIM1_IN1	ATK1_B07,ADC1_42,DAC2_CH2_OUT2,OPAMP3_INM0,SEG1
45	60	PC14	I/O	SPI2_MISO,I2C1_SCL,USART1_TX,TIM1_CH3,TIM4_CH2,LPTIM1_ETR,EVENTOUT	ATK1_B08,ADC1_43,COMP2_INP5,SEG0
46	61	PA14	I/O	SPI2_MOSI,I2C1_SDA,USART1_RX,LPTIM1_IN2,TIM4_ETR,EVENTOUT	ATK1_B09,ADC1_44,COMP2_INM8,COM7,SEG27,LED7,LCOM7
47	62	PA15	I/O	SPI2_SCK,I2C1_SCL,USART3_TX,TIM4_CH1,COMP4_OUT,PLA1_IN19	ATK1_B10,ADC1_45,COMP3_INP2,COMP3_INM2,OPAMP4_INP0,COM6,SEG26,LED6,LCOM6
48	63	PB13	I/O	SPI2_NSS,I2C1_SDA,USART3_RX,TIM4_CH4,IRTIM1_OUT,EVENTOUT,PLA1_IN20	ADC1_53,COMP1_INM6,COMP2_INP6,OPAMP4_INM0
-	64	PC15	I/O	USART3_TX,TIM1_CH3	ADC1_54,COMP1_INM7,COM

Pin Number		Pin name	Pin type	Alternate functions	Additional functions
LQFP48	LQFP64				
					P2_INP7,OPAMP4_OUT

If LED module is activated (LCD_CR.LCDON=1) and LED mode is matrix mode(LCD_CR.LEDMODE=00), all used pins occupied by this mode will not share their additional functions to other modules. Matrix mode of LED's additional functions including LSEG0~7 and LCOM0~x (x is decided by the value of LCD_CR.DUTY).

If LCD module is activated (LCD_CR.LCDON=1), all used pins occupied by LCD will not share their additional functions to other modules. LCD's additional functions including SEG0~27 and COM0~7.

4.3 Pin's alternate functions

Table 4-3-1 Port A alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0								
PA1	USART3_RX	TIM1_CH4						
PA2	LPTIM1_IN1							
PA3	TIM1_BKIN	RTC_OUT						
PA4	COMP2_OUT	TIM1_BKIN2						
PA5	OSC32_EN	OSC_EN						
PA6	COMP1_OUT	SPI2_SCK	USART2_CTS_NSS	TIM2_CH1_ETR	LPTIM1_OUT			PLA_IN3
PA7	SPI1_SCK	USART2_RTS_DE_CK	TIM2_CH2	EVENTOUT		COMP3_OUT	PLA_OUT0	PLA_IN4
PA8	COMP2_OUT	SPI1_MOSI	USART2_TX	LPUART1_TX	TIM2_CH3	LSCO		PLA_IN5
PA9	SPI2_MISO	USART2_RX	LPUART1_RX	TIM2_CH4		COMP4_OUT	PLA_OUT1	PLA_IN6
PA10	SPI1_MISO	COMP1_OUT	I2C2_SCL	USART1_CTS_NSS	TIM1_CH4	TIM1_BKIN2		PLA_IN17
PA11	SPI1_MOSI	COMP2_OUT	I2C2_SDA	USART1_RTS_DE_CK	TIM1_ETR			PLA_IN18

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA12	SWDIO	IRTIM1_OUT	EVENTOUT	USART2_RX				
PA13	SWCLK	USART2_TX	BOOT0	EVENTOUT				
PA14	SPI2_MOSI	I2C1_SDA	USART1_RX	LPTIM1_IN2	TIM4_ETR	EVENTOUT		
PA15	SPI2_SCK	I2C1_SCL	USART3_TX	TIM4_CH1		COMP4_OUT		PLA_IN19

Table 4-3-2 Port B alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB0	USART3_RTS_DE_CK		TIM1_CH3N	TIM2_CH1	TIM3_CH4	EVENTOUT	COMP4_OUT	PLA_IN12
PB1	SPI2_MISO	I2C1_SCL	USART1_TX	TIM1_CH2	MCO		TIM1_CH1N	PLA_IN14
PB2	TIM2_CH3	TIM3_CH1					TIM1_CH2	PLA_IN15
PB3	TIM2_CH4	TIM3_CH2					TIM1_CH2N	
PB4	SPI1_SCK	USART3_TX	LPTIM1_OUT				TIM1_CH3	
PB5	SPI1_NSS	USART3_RX	TIM1_BKIN2				TIM1_CH3N	
PB6	SPI2_MOSI	I2C1_SDA	USART1_RX	TIM1_CH3	EVENTOUT	COMP3_OUT	PLA_OUT0	PLA_IN16
PB7	SPI2_MISO	USART2_CTS_NSS	TIM1_CH2N					
PB8	SPI2_MOSI	USART2_RTS_DE_CK	TIM1_CH3N					
PB9	SPI1_MISO	USART2_TX	TIM1_BKIN				TIM1_CH1	
PB10	SPI1_MOSI	USART2_RX						
PB11	SPI1_MISO	USART1_CTS_NSS	TIM3_CH1	EVENTOUT			PLA_OUT3	
PB12	COMP2_OUT	SPI1_MOSI	TIM3_CH2	TIM4_CH3	LPTIM1_IN1			
PB13	SPI2_NSS	I2C1_SDA	USART3_RX	TIM4_CH4	IRTIM1_OUT	EVENTOUT		PLA_IN20

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB14	USART1_TX	USART3_TX	TIM2_CH1_ETR					
PB15	COMP1_OUT	SPI1_NSS	USART3_RX	TIM1_CH2N	TIM3_CH3	LPTIM1_OUT		PLA_IN11

Table 4-3-3 Port C alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC0								PLA_IN1
PC1	OSC_EN							PLA_IN2
PC2	LPUART1_RX	LPTIM1_IN1						
PC3	LPUART1_TX	LPTIM1_OUT						
PC4	SPI1_NSS	SPI2_MOSI	TIM2_CH1	RTC_OUT				PLA_IN7
PC5	SPI1_SCK	USART3_TX	TIM2_CH1_ETR			COMP3_OUT	PLA_OUT2	PLA_IN8
PC6	COMP1_OUT	SPI1_MISO	USART3_CTS_NSS		TIM1_BKIN	TIM3_CH1	TIM4_CH1	PLA_IN9
PC7	COMP2_OUT	SPI1_MOSI	TIM1_CH1N	TIM2_CH1	TIM3_CH2	TIM4_CH4	PLA_OUT3	PLA_IN10
PC8	USART1_RX	USART3_RX	TIM2_CH2					
PC9	SPI1_NSS	USART2_RX	USART3_RTS_DE_CK	TIM2_CH1_ETR	EVENTOUT		PLA_OUT1	
PC10	TIM1_CH1	TIM3_CH3						
PC11	TIM1_CH2	TIM3_CH4						
PC12	USART3_RTS_DE_CK	TIM1_CH1N	TIM3_ETR					
PC13	SPI1_SCK	USART1_RTS_DE_CK	TIM1_CH2	TIM2_CH2	EVENTOUT		PLA_OUT2	
PC14	SPI2_MISO	I2C1_SCL	USART1_TX	TIM1_CH3	TIM4_CH2	LPTIM1_ETR	EVENTOUT	
PC15	USART3_TX	TIM1_CH3						

Table 4-3-4 Port D alternate function mapping

Port	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PD0	SPI2_MISO	LPTIM1_IN2						
PD1	SPI2_MOSI	LPTIM1_ETR						
PD2	SPI2_MISO	USART3_TX	LPTIM1_OUT	EVENTOUT				
PD3	COMP1_OUT	SPI2_SCK	I2C2_SCL	USART3_TX	LPUART1_RX	TIM2_CH3		
PD4	COMP2_OUT	SPI2_MOSI	I2C2_SDA	USART3_RX	LPUART1_TX	TIM2_CH4		
PD5	SPI2_NSS		TIM1_BKIN	EVENTOUT				
PD6	SPI2_SCK	I2C2_SCL	USART3_CTS_NSS		TIM1_CH1N	TIM2_CH3	EVENTOUT	
PD7	SPI2_MISO	I2C2_SDA	USART3_RTS_DE_CK	TIM1_CH2N	EVENTOUT			
PD8	SPI2_MOSI	TIM1_CH3N	EVENTOUT					
PD9	SPI2_NSS	TIM1_CH1	MCO	EVENTOUT				PLA_IN13
PD10	SPI2_NSS	TIM4_CH1	EVENTOUT				TIM1_CH3	
PD11	SPI2_SCK	TIM4_CH4	EVENTOUT					
PD12								
PD13	MCO							

Table 4-3-5 Pin function description

Pin name	Pin type	Description
I/O		
PA0~PA15	I/O	16-bit bidirectional I/O port
PB0~PB15	I/O	16-bit bidirectional I/O port
PC0~PC15	I/O	16-bit bidirectional I/O port
PD0~PD13	I/O	14-bit bidirectional I/O port
USART		
USART1_TX~USART3_TX	O	USART1-3 data transfer port
USART1_RX~USART3_RX	I	USART1-3 data receive port
USART1_RTS~USART3_RTS	O	USART1-3 require to send (RTS) port
USART1_CTS~USART3_CTS	I	USART1-3 clear to send (CTS) port

Pin name	Pin type	Description
LPUART		
LPUART1_TX	O	LPUART1 data transfer port
LPUART1_RX	I	LPUART1 data receive port
LPUART1_RTS	O	LPUART1 require to send (RTS) port
LPUART1_CTS	I	LPUART1 clear to send (CTS) port
SPI		
SPI1_MOSI~SPI2_MOSI	I/O	SPI1-2 master output slave input (MOSI) pin
SPI1_MISO~SPI2_MISO	I/O	SPI1-2 master input slave output (MISO) pin
SPI1_SCK~SPI2_SCK	I/O	SPI1-2 serial clock (SCK) pin
SPI1_NSS~SPI2_NSS	I	SPI1-2 negative slave select (NSS) pin
I²C		
I²C1_SCL~I²C2_SCL	I/O	I2C1-2 serial clock (SCL) pin
I²C1_SDA~I²C2_SDA	I/O	I2C1-2 serial data (SDA) pin
TIM1		
TIM1_CH1/CH1N	I/O	Advanced-control timer TIM1's channel1, support dual channel complementary PWM output with dead-time insertion and input capture.
TIM1_CH2/CH2N	I/O	Advanced-control timer TIM1's channel2, support dual channel complementary PWM output with dead-time insertion and input capture.
TIM1_CH3/CH3N	I/O	Advanced-control timer TIM1's channel3, support dual channel complementary PWM output with dead-time insertion and input capture.
TIM1_CH4	I/O	Advanced-control timer TIM1's channel3, support PWM output and input capture.
TIM1_ETR	I	Advanced-control timer TIM1's external trigger input.
TIM1_BKIN	I	Advanced-control timer TIM1's break input.
TIM2~TIM4		
TIM2_CH1/CH2/CH3/CH4	I/O	General-purpose timer TIM2's channel1/2/3/4, support PWM output and input capture.
TIM3_CH1/CH2/CH3/CH4	I/O	General-purpose timer TIM3's channel1/2/3/4, support PWM output and input capture.
TIM4_CH1/CH2/CH3/CH4	I/O	General-purpose timer TIM4's channel1/2/3/4, support PWM output and input capture.
TIM2_ETR~TIM4_ETR	I	General-purpose timer TIM2-4's external trigger input.
TIM2_TRGO~TIM4_TRGO	O	General-purpose timer TIM2-4's trigger output.
LPTIM		
LPTIM1_OUT	O	LPTIM1's output.
LPTIM1_IN1~LPTIM1_IN2	I	LPTIM1's input to wakeup.
LPTIM1_ETR	I	LPTIM1's external trigger input.

Pin name	Pin type	Description
LED		
LCOM0~LCOM7	O	LED matrix mode's COM output.
LSEG0~LSEG7	O	LED matrix mode's SEG output.
LED0~LED7	O	LED dot mode's output.
LCD		
COM0~COM7	O	LCD COM0-7 output
SEG0~SEG27	O	LCD SEG0-27 output
TK		
TKA00~TKA20, TKB00~TKB20	I	Touch key channel00-20's input in each group A and B.
12bit ADC		
ADC1_00~ADC1_55	I	ADC1 channel00-55's input.
SAC's OPAMP		
OPAMP1_INP~OPAMP4_INP	I	OPAMP1-4 positive input.
OPAMP1_INM~OPAMP4_INM	I	OPAMP1-4 negative input.
OPAMP1_OUT~OPAMP4_OUT	O	OPAMP1-4 output.
SAC's DAC		
DAC1_CH1_OUTx~DAC1_CH2_OUTx	O	DAC1 output.
DAC2_CH1_OUTx~DAC2_CH2_OUTx	O	DAC2 output.
SAC's COMP		
COMP1_INP~COMP4_INP	I	COMP1-4 positive input.
COMP1_INM~COMP4_INM	I	COMP1-4 negative input.
COMP1_OUT~COMP4_OUT	O	COMP1-4 output.
PLA		
PLA_IN1~PLA_IN20	I	PLA channel1-20's input.
PLA_OUT0~PLA_OUT3	O	PLA channel0-3's output.
Power		
VDD/VDDA	P	Power
VSS/VSSA	P	Ground
VREF+	P	VREF+reference voltage pin
AVDD	P	24 bit ADC analog power input pin/analog power low voltage difference regulator output pin
VDDO	P	24 bit ADC positive power supply voltage
DVDD	P	24 bit ADC digital power input pin/digital power low-voltage regulator output pin
REFP	P	24 bit ADC external positive reference voltage input pin/internal positive reference voltage output pin
Reset		
NRST	I/O	Microcontroller's external global reset signal pin with pull-up resistor connected. Low level voltage input available for RST.

Pin name	Pin type	Description
Clock		
OSC_IN	I	External high frequency oscillator or clock signal input.
OSC_OUT	O	External high frequency oscillator signal output.
OSC_EN	I	External high frequency clock signal input enable.
OSC32_IN	I	External low frequency oscillator or clock signal input.
OSC32_OUT	O	External low frequency oscillator signal output.
OSC32_EN	I	External low frequency clock signal input enable.
MCO	O	Microcontroller's high frequency clock output.
RTC_OUT	O	RTC clock output (1Hz)
LSCO	O	Microcontroller's low frequency clock output.
24bit ADC		
INN1~3	I	24 bit ADC full differential input for negative input (with INP1~3)/pseudo differential or single ended input channels 1-3
INP1~3	I	24 bit ADC fully differential input paired with positive input (compatible with INN1-3)/pseudo differential or single ended input channels 1-3
Others		
IRTIM1_OUT	O	IRTIM1 output.
EVENTOUT	O	Quick event output.
BOOT0	I	Microcontroller's boot mode control.
SWD		
SWDIO	I/O	SWDP data input/output.
SWCLK	I	SWDP clock input.

5 Electrical characteristics

5.1 Parameter conditions

- Unless otherwise specified, all voltages are referenced to VSS.
- Parameter values defined at temperatures or in temperature ranges out of the ordering information scope are to be ignored.
- Packages used for characterizing certain electrical parameters may differ from the commercial packages as per the ordering information.

5.1.1 Minimum and maximum values

- Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at TA = 25 °C and TA = TA(max) (given by the selected temperature range).
- Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

5.1.2 Typical values

- Unless otherwise specified, typical data are based on TA = 25 °C, VDD = VDDA = VREF+ = 5V. They are given only as design guidelines and are not tested.
- Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in Figure 5-1-5.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in Figure 5-1-5.

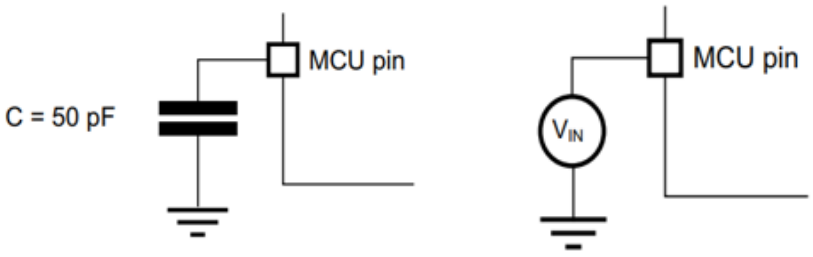


Figure 5-1-5 Pin loading conditions and input voltage

5.1.6 Power supply scheme

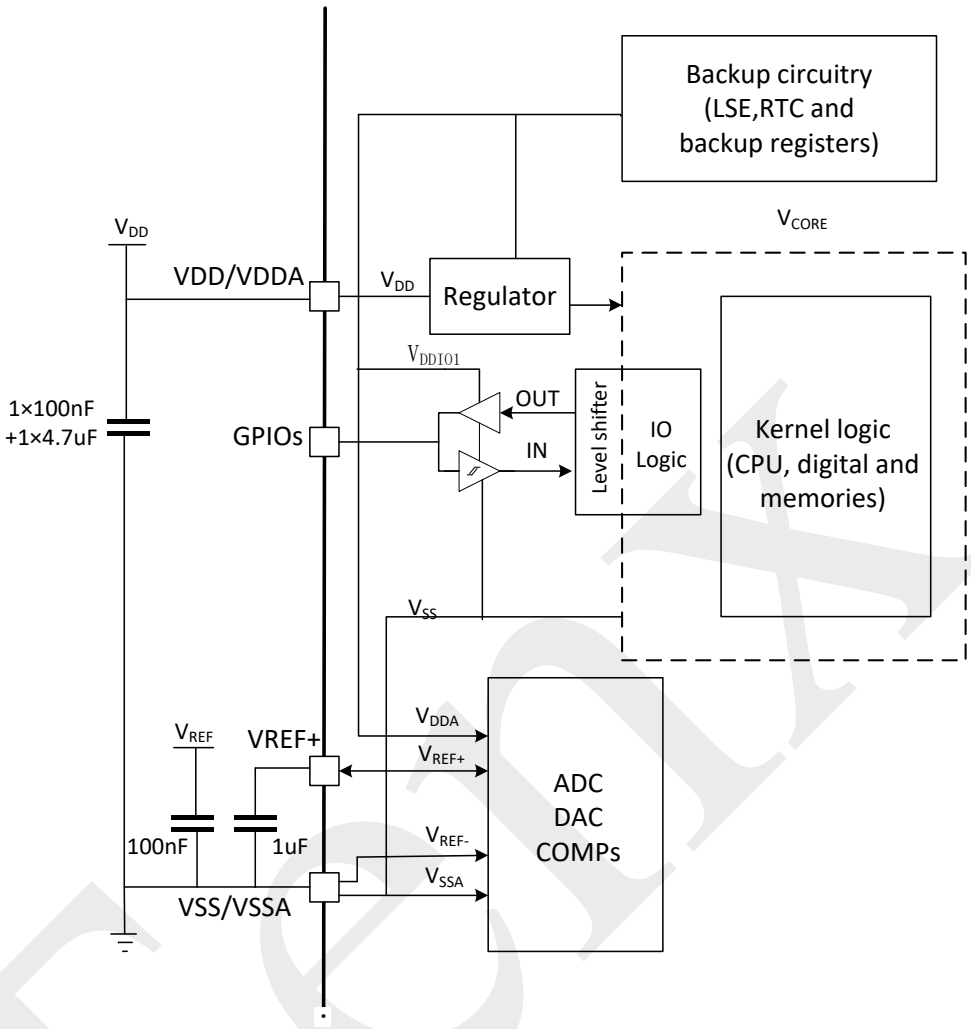


Figure 5-1-6 Power supply scheme

Note: Power supply pin pair (VDD/VDDA and VSS/VSSA) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure the good functionality of the device.

5.1.7 Current consumption measurement

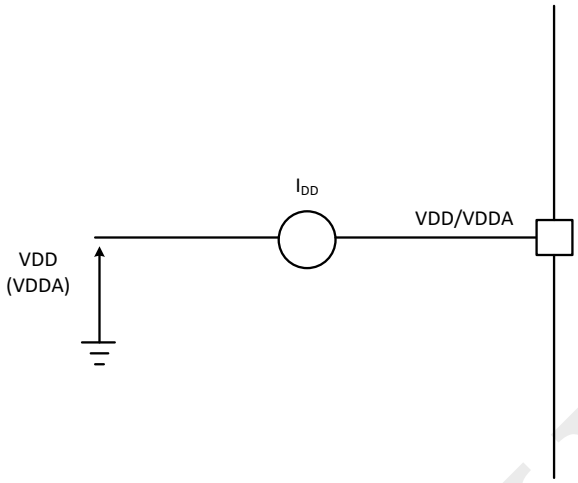


Figure 5-1-7 Current consumption measurement scheme

5.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in following may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

All voltages are defined with respect to VSS.

5.2.1 Voltage characteristics

Table 5-2-1 Voltage characteristics (1)

Symbol	Ratings	Min	Max	Unit
V_{DD}	External supply voltage	-0.3	6.0	V
V_{DDA}	External analog supply voltage	-0.3	6.0	V
V_{IN}	Input voltage on I/O pins	-0.3	6.0	V
V_{REF+}	External voltage on VREF+ pin	-0.3	6.0	V

1. Guaranteed by design.

5.2.2 Current characteristics

Table 5-2-2 Current characteristics

Symbol	Ratings	Max	Unit
$I_{VDD/VDDA}$	Current into VDD/VDDA power pin (source)	249	mA
$I_{VSS/VSSA}$	Current out of VSS/VSSA ground pin (sink)	249	mA
$I_{IO(PIN)}$	Output current sourced by any I/O(GL2 type) and control pin.	47	mA
	Output current sourced by any I/O(GLC type) and control pin.	44	
	Output current sourced by any I/O(GLE type) and control pin.	47	

Symbol	Ratings	Max	Unit
	Output current sunk by any I/O(GL2 type) and control pin.	140	
	Output current sunk by any I/O(GLC type) and control pin.	138	
	Output current sunk by any I/O(GLE type) and control pin.	140	
$\sum I_{IO(PIN)}$	Total output current sourced by sum of all I/Os and control pins.	241	mA
	Total output current sunk by sum of all I/Os and control pins.	242	
$I_{INJ(PIN)}$(2)	Injected current on any I/O(GL2 type)	0.77	mA
	Injected current on any I/O(GLC type)	0.20	
	Injected current on any I/O(GLE type)	0.17	
$\sum\|I_{INJ(PIN)}\|$	Total injected current (sum of all I/Os and control pins)	0.00017	mA

1. Guaranteed by design.
2. A positive injection is induced by $V_{IN}>V_{DDIOx}$ while a negative injection is induced by $V_{IN}<V_{SS}$.

5.2.3 Thermal characteristics

Table 5-2-3 Thermal characteristics

Symbol	Ratings	Min	Max	Unit
T_{STG}	Storage temperature range	-65(1)	150(1)	℃
T_A	Ambient temperature range	-40	105	℃
T_J	Maximum junction temperature	-	125(1)	℃

1. Guaranteed by design.

5.2.4 Other characteristics

Table 5-2-4 Other characteristics

Symbol	Parameter	Max	Unit
Nend	Flash endurance	100k(1)	cycles
Tret	Fash data retention	≥10(1)	years
ESD(HBM)	Electrostatic discharge	≥8000(1)	V

1. Guaranteed by design.

5.3 Operating conditions

5.3.1 General operating conditions

Table 5-3-1 General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
F_{HCLK}	Internal AHB clock frequency	-	0	48	MHz
F_{PCLK}	Internal APB clock frequency	-	0	48	MHz
V_{DD}	Standard operating voltage	-	2.2(1)	5.5	V
V_{DDA}	Analog supply voltage	COMP operation	1.6(2)	6.0(2)	V
		OPAMP operation	2.4(2)	5.5(2)	

Symbol	Parameter	Conditions	Min	Max	Unit
		DAC operation	1.7(2)	6.0(2)	
		ADC operation	2.0(2)	5.5(2)	
		V_{BGO} operation	2.0(2)	5.5(2)	
V_{REF+}	Reference voltage	DAC operation	1.7(2)	6.0(2)	V
		ADC operation	2.4(2)	V_{DDA}(2)	
V_{IN}	I/O input voltage	-	-0.3	V_{DD}+0.3	V
T_A	Ambient temperature	-	-40	105	℃
T_J	Junction temperature	-	-40(3)	125(3)	℃

1. When RESET is released functionality is guaranteed down to V_{POR} min.
2. Test result under 25℃ condition.
3. Guaranteed by design.

5.3.2 Operating conditions at power-up/power-down

The parameters given in Table 5-3-2 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-2 Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} slew rate	V_{DD} rising	-	∞	μs/V
		V_{DD} falling	14	∞	ms/V

5.3.3 Embedded reset and power control block characteristics

The parameters given in Table 5-3-3 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-3 Embedded reset and power control block characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$t_{RSTTEMPO}$	POR temporization when V_{DD} crosses V_{POR}	V_{DD} rising		-	605(1)	-	μs
V_{POR}	Power-on reset threshold	-		1.833	2.186	2.542	V
V_{PDR}	Power-down reset threshold	-		1.801	2.205	2.523	V
V_{PVD}	Programmable voltage detector threshold	PVD_HYS[1:0]=00; PVDT[4:0]=00000	V_{DD} rising	-	1.99	-	V
			V_{DD} falling	-	1.98	-	
		PVD_HYS[1:0]=01; PVDT[4:0]=00000	V_{DD} rising	-	2.02	-	
			V_{DD} falling	-	1.96	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=00000	V_{DD} rising	-	2.04	-	
			V_{DD} falling	-	1.93	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=00000	V_{DD} rising	-	2.05	-	
			V_{DD} falling	-	1.92	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		PVD_HYS[1:0]=00; PVDT[4:0]=01111	V_{DD} rising	-	3.37	-	
			V_{DD} falling	-	3.35	-	
		PVD_HYS[1:0]=01; PVDT[4:0]=01111	V_{DD} rising	-	3.42	-	
			V_{DD} falling	-	3.30	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=01111	V_{DD} rising	-	3.45	-	
			V_{DD} falling	-	3.26	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=01111	V_{DD} rising	-	3.46	-	
			V_{DD} falling	-	3.23	-	
		PVD_HYS[1:0]=00; PVDT[4:0]=11111	V_{DD} rising	-	4.84	-	
			V_{DD} falling	-	4.81	-	
		PVD_HYS[1:0]=01; PVDT[4:0]=11111	V_{DD} rising	-	4.91	-	
			V_{DD} falling	-	4.75	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=11111	V_{DD} rising	-	4.96	-	
			V_{DD} falling	-	4.68	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=11111	V_{DD} rising	-	4.97	-	
			V_{DD} falling	-	4.65	-	
V_{BOR}	Brownout reset threshold	BOR_HYS[1:0]=00; BOR_LEV[2:0]=000	V_{DD} rising	-	2.34	-	V
			V_{DD} falling	-	2.25	-	
		BOR_HYS[1:0]=01; BOR_LEV[2:0]=000	V_{DD} rising	-	2.34	-	
			V_{DD} falling	-	2.23	-	
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=000	V_{DD} rising	-	2.37	-	
			V_{DD} falling	-	2.22	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=000	V_{DD} rising	-	2.38	-	
			V_{DD} falling	-	2.21	-	
		BOR_HYS[1:0]=00; BOR_LEV[2:0]=100	V_{DD} rising	-	3.21	-	
			V_{DD} falling	-	3.16	-	
		BOR_HYS[1:0]=01; BOR_LEV[2:0]=100	V_{DD} rising	-	3.26	-	
			V_{DD} falling	-	3.12	-	
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=100	V_{DD} rising	-	3.26	-	
			V_{DD} falling	-	3.09	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=100	V_{DD} rising	-	3.30	-	
			V_{DD} falling	-	3.07	-	
		BOR_HYS[1:0]=00; BOR_LEV[2:0]=111	V_{DD} rising	-	3.94	-	
			V_{DD} falling	-	3.87	-	
		BOR_HYS[1:0]=01; BOR_LEV[2:0]=111	V_{DD} rising	-	4.00	-	
			V_{DD} falling	-	3.82	-	
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=111	V_{DD} rising	-	4.02	-	
			V_{DD} falling	-	3.79	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=111	V_{DD} rising	-	4.06	-	
			V_{DD} falling	-	3.76	-	
V_{hyst_PVD}	Hysteresis of V_{PVD}	PVD_HYS[1:0]=00;		-	11	-	mV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		PVDT[4:0]=00000				
		PVD_HYS[1:0]=01; PVDT[4:0]=00000	-	66	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=00000	-	102	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=00000	-	127	-	
		PVD_HYS[1:0]=00; PVDT[4:0]=01111	-	21	-	
		PVD_HYS[1:0]=01; PVDT[4:0]=01111	-	114	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=01111	-	176	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=01111	-	214	-	
		PVD_HYS[1:0]=00; PVDT[4:0]=11111	-	35	-	
		PVD_HYS[1:0]=01; PVDT[4:0]=11111	-	163	-	
		PVD_HYS[1:0]=10; PVDT[4:0]=11111	-	254	-	
		PVD_HYS[1:0]=11; PVDT[4:0]=11111	-	310	-	
V_{hyst_BOR}	Hysteresis of V_{BOR}	BOR_HYS[1:0]=00; BOR_LEV[2:0]=000	-	36	-	mV
		BOR_HYS[1:0]=01; BOR_LEV[2:0]=000	-	72	-	
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=000	-	100	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=000	-	126	-	
		BOR_HYS[1:0]=00; BOR_LEV[2:0]=100	-	62	-	
		BOR_HYS[1:0]=01; BOR_LEV[2:0]=100	-	136	-	
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=100	-	187	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=100	-	227	-	
		BOR_HYS[1:0]=00; BOR_LEV[2:0]=111	-	77	-	
		BOR_HYS[1:0]=01;	-	171	-	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		BOR_LEV[2:0]=111				
		BOR_HYS[1:0]=10; BOR_LEV[2:0]=111	-	236	-	
		BOR_HYS[1:0]=11; BOR_LEV[2:0]=111	-	286	-	
I_{DD_PVD}	PVD consumption from V_{DD}(1)	-	-	32	65	μA
I_{DD_BOR}	BOR consumption from V_{DD}(1)	-	-	32	64	μA

1. Guaranteed by design.

5.3.4 Embedded voltage reference

The parameters given in Table 5-3-4 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-4 Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{VBGO}(1)	Internal reference voltage (VBGO default output value)	-	-	1.23	-	V
$t_{S\_vrefint}$(1)	ADC sampling time when reading the internal reference voltage	-	2.5	-	239.5	f_{adc}
$t_{start\_vrefint}$(1)	Start time of reference voltage buffer when ADC is enable	-	-	300	-	ns
$I_{DD(VBGO)}$ (1)	V_{VBGO} buffer consumption from V_{DD} when converted by ADC	-	67	70	72	μA
$\triangle V_{VBG}$(1)	Internal reference voltage spread over the temperature range (VBG=1.23V)	V_{DD}=5.0V (-40~105℃)	-	12	22	mV
$T_{Coeff\_vrefint}$(1)	V_{VBG} temperature coefficient (VBG=1.23V)	T_A=25℃	44.47	54.47	112.1	ppm/℃
A_{Coeff}	Long term stability	1hour,T_A=25℃	-	1150	-	ppm
$V_{DDCoeff}$(1)	V_{DD} voltage coefficient	2.0V<V_{DD}<5.5V	-	4141	-	ppm/V
V_{BGR}	VBGOS=00	V_{DD}=5.0V (-40~105℃)	1.208	1.234	1.242	V
	VBGOS=01		2.449	2.494	2.513	
	VBGOS=10		2.947	2.999	3.019	
	VBGOS=11		3.925	4.001	4.025	

1. Guaranteed by design.

5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program

location in memory and executed binary code.

The current consumption is measured as described in Figure 5-1-7.

Typical and maximum current consumption:

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode.
- All peripherals are disabled except when explicitly mentioned.
- The Flash memory access time is adjusted with the minimum wait states number, depending on the fHCLK frequency (refer to FLASH_ACR.LATENCY[1:0] in the reference manual)
- When the peripherals are enabled, fPCLK1=fPCLK2=FHCLK
- For Flash memory and shared peripherals, fPCLK1=fPCLK2=FHCLK

Unless otherwise stated, the parameters given in Table 5-3-5-1 to Table 5-3-5-5 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-5-1 Current consumption in Run/Sleep/Stop modes at different die temperatures (VDD=2.3V)

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, HSE enable	18MHz,by pass mode	Flash Memory	5.7	4.6	5.7	5.6	mA
				SRAM	2.2	3.8	2.3	4.9	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, LSE enable	32KHz,by pass mode	Flash Memory	0.3	0.5	0.6	0.6	mA
				SRAM	0.3	0.4	0.5	0.6	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	Flash Memory	8.4	8.3	9.2	8.5	mA
			42MHz		6.3	8.5	7.1	8.7	
			36MHz		6.6	7.4	7.2	7.6	
			30MHz		7.0	7.7	7.4	7.9	
			24MHz		5.8	6.4	6.2	6.6	
			18MHz		4.3	4.8	6.6	4.9	
			9MHz		2.7	3.0	3.8	3.1	
			4.5MHz		2.4	2.6	2.4	2.7	
			2.25MHz		1.4	1.7	1.4	1.7	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	SRAM	5.9	6.2	6.0	6.2	mA
			42MHz		6.8	7.0	6.8	7.1	
			36MHz		4.7	5.1	4.8	5.1	
			30MHz		4.1	4.4	4.1	4.4	
			24MHz		3.4	3.6	3.4	3.7	
			18MHz		3.4	3.7	3.4	3.7	
			9MHz		1.9	2.3	1.9	2.4	
			4.5MHz		1.6	1.9	1.7	2.0	

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
			2.25MHz		1.3	1.6	1.3	1.7	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	Flash Memory	1.7	2.4	1.7	2.5	mA
			9MHz		1.4	1.8	1.4	1.9	
			4.5MHz		1.2	1.5	1.2	1.6	
			2.25MHz		1.1	1.4	1.1	1.4	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	SRAM	1.7	2.0	1.7	2.1	mA
			9MHz		1.4	1.7	1.4	1.8	
			4.5MHz		1.2	1.5	1.2	1.6	
			2.25MHz		1.1	1.4	1.1	1.5	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	Flash Memory	417	624	709	821	µA
			32KHz (LSI)		399	627	422	633	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		74	181	78	183	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	SRAM	421	614	698	804	µA
			32KHz (LSI)		408	666	438	817	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		80	198	90	372	

Table 5-3-5-2 Current consumption in Run/Sleep/Stop modes at different die temperatures (VDD=3.3V)

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, HSE enable	18MHz,by pass mode	Flash Memory	5.7	5.1	5.8	6.0	mA
				SRAM	2.3	4.3	2.4	5.3	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, LSE enable	32KHz,by pass mode	Flash Memory	0.3	0.5	0.7	0.7	mA
				SRAM	0.3	0.5	0.6	0.7	

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	Flash Memory	8.4	8.3	9.2	8.5	mA
			42MHz		6.3	8.4	7.1	8.7	
			36MHz		6.5	7.4	7.2	7.6	
			30MHz		7.0	7.7	7.4	7.9	
			24MHz		5.8	6.4	6.1	6.7	
			18MHz		4.3	4.8	6.5	4.9	
			9MHz		2.7	3.0	3.8	3.1	
			4.5MHz		2.4	2.6	2.4	2.7	
			2.25MHz		1.4	1.7	1.5	1.7	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	SRAM	5.9	6.2	5.9	6.2	mA
			42MHz		6.8	7.1	6.8	7.1	
			36MHz		0.7	5.0	0.8	5.1	
			30MHz		4.1	4.4	4.1	4.4	
			24MHz		3.4	3.7	3.4	3.8	
			18MHz		3.4	3.7	3.4	3.8	
			9MHz		1.9	2.2	2.0	2.4	
			4.5MHz		1.7	1.9	1.7	2.1	
			2.25MHz		1.4	1.6	1.4	1.8	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	Flash Memory	1.7	2.4	1.7	2.5	mA
			9MHz		1.4	1.8	1.4	1.9	
			4.5MHz		1.2	1.5	1.2	1.6	
			2.25MHz		1.1	1.4	1.1	1.4	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	SRAM	1.8	2.0	1.8	2.2	mA
			9MHz		1.4	1.7	1.4	1.9	
			4.5MHz		1.2	1.5	1.2	1.7	
			2.25MHz		1.1	1.4	1.2	1.6	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	Flash Memory	358	574	741	843	µA
			32KHz (LSI)		408	637	433	645	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		106	245	117	249	
$I_{DD(Stop)}$		LDO/LSE/LSI enable	32KHz (LSE)	SRAM	356	567	726	822	µA

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
	Supply current in Stop mode		32KHz (LSI)		426	679	449	903	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		126	270	132	510	

Table 5-3-5-3 Current consumption in Run/Sleep/Stop modes at different die temperatures (VDD=5.0V)

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, HSE enable	18MHz,by pass mode	Flash Memory	6.0	6.3	6.2	6.9	mA
				SRAM	2.6	5.5	2.9	6.3	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, LSE enable	32KHz,by pass mode	Flash Memory	0.3	0.4	0.8	0.8	mA
				SRAM	0.3	0.4	0.8	0.7	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	Flash Memory	8.4	8.2	9.1	8.4	mA
			42MHz		6.3	8.4	7.0	8.6	
			36MHz		6.6	7.4	7.1	7.6	
			30MHz		7.0	7.6	7.4	7.8	
			24MHz		5.8	6.4	6.1	6.5	
			18MHz		4.3	4.8	6.5	4.9	
			9MHz		2.7	3.0	3.8	3.1	
			4.5MHz		2.4	2.6	2.4	2.7	
			2.25MHz		1.5	1.7	1.5	1.8	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	SRAM	5.9	6.2	6.0	6.3	mA
			42MHz		6.8	7.0	6.8	7.1	
			36MHz		4.7	5.0	4.8	5.2	

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
			30MHz		4.1	4.4	4.1	4.5	
			24MHz		3.4	3.7	3.5	3.9	
			18MHz		3.4	3.7	3.5	3.9	
			9MHz		1.9	2.2	2.0	2.5	
			4.5MHz		1.7	1.9	1.7	2.2	
			2.25MHz		1.4	1.6	1.4	2.0	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	Flash Memory	1.9	2.4	2.4	2.5	mA
			9MHz		1.5	1.9	1.8	1.9	
			4.5MHz		1.3	1.6	1.4	1.6	
			2.25MHz		1.3	1.5	1.3	1.5	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	SRAM	1.8	2.0	1.9	2.4	mA
			9MHz		1.5	1.7	1.6	2.0	
			4.5MHz		1.3	1.5	1.4	1.9	
			2.25MHz		1.2	1.5	1.3	1.8	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	Flash Memory	321	407	849	782	µA
			32KHz (LSI)		441	643	459	652	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		152	341	172	419	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	SRAM	301	396	829	762	µA
			32KHz		458	687	477	1030	

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
			(LSI)						
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		326	359	717	720	

Table 5-3-5-4 Current consumption in Run/Sleep/Stop modes at different die temperatures (VDD=5.5V)

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, HSE enable	18MHz,by pass mode	Flash Memory	6.2	6.7	6.4	7.3	mA
				SRAM	2.8	5.9	3.1	6.7	
$I_{DD(Run)}$	Supply current in Run mode	PLL disable, LSE enable	32KHz,by pass mode	Flash Memory	0.4	0.4	0.9	0.8	mA
				SRAM	0.3	0.4	0.9	0.8	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	Flash Memory	8.4	8.2	9.1	8.4	mA
			42MHz		6.4	8.3	7.0	8.6	
			36MHz		6.6	7.3	7.1	7.6	
			30MHz		7.0	7.6	7.4	7.8	
			24MHz		5.9	6.4	6.1	6.6	
			18MHz		4.4	4.8	6.5	4.9	
			9MHz		2.8	3.0	3.8	3.1	
			4.5MHz		2.4	2.6	2.5	2.7	
			2.25MHz		1.5	1.7	1.6	1.8	
$I_{DD(Run)}$	Supply current in Run mode	PLL enable, HSI enable	48MHz	SRAM	5.9	6.2	6.1	6.3	mA
			42MHz		6.8	7.0	6.9	7.2	
			36MHz		3.7	5.0	4.8	5.2	
			30MHz		4.1	4.4	4.2	4.6	
			24MHz		3.4	3.7	3.5	3.9	
			18MHz		3.4	3.7	3.4	3.9	
			9MHz		2.0	2.2	2.1	2.6	

Symbol	Parameter	Conditions			Typ		Max		Unit
		General	f_{HCLK}	Fetch from	25℃	85℃	25℃	85℃	
			4.5MHz		1.7	2.0	1.8	2.3	
			2.25MHz		1.4	1.6	1.6	2.0	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	Flash Memory	2.0	2.5	2.6	2.5	mA
			9MHz		1.6	1.9	1.9	2.0	
			4.5MHz		1.4	1.7	1.5	1.7	
			2.25MHz		1.3	1.5	1.4	1.5	
$I_{DD(Sleep)}$	Supply current in Sleep mode	PLL enable, HSI enable	18MHz	SRAM	1.9	2.1	2.0	2.5	mA
			9MHz		1.5	1.8	1.6	2.1	
			4.5MHz		1.3	1.6	1.4	2.0	
			2.25MHz		1.2	1.5	1.3	1.9	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	Flash Memory	350	383	914	789	µA
			32KHz (LSI)		453	653	499	660	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		171	376	216	378	
$I_{DD(Stop)}$	Supply current in Stop mode	LDO/LSE/LSI enable	32KHz (LSE)	SRAM	325	370	891	777	µA
			32KHz (LSI)		470	694	516	1073	
		LDO/LSE/LSI disable	External interrupt occurs (all clock disabled)		189	388	423	794	

Table 5-3-5-5 Current consumption of peripherals

Peripheral	Bus	µA/MHz			
		Run mode		Sleep mode	
		3.3V	5.0V	3.3V	5.0V
IOPORT Bus	IOPORT	-	-	-	-
GPIOA		2.0	1.6	1.8	1.9
GPIOB		1.7	1.6	1.6	1.7
GPIOC		1.5	1.5	1.5	1.4
GPIOD		1.5	1.4	1.4	1.5
All AHB Peripherals	AHB	-	-	-	-
HDIV		1.2	1.2	1.2	1.2

Peripheral	Bus	μA/MHz			
		Run mode		Sleep mode	
		3.3V	5.0V	3.3V	5.0V
PLA		1.2	1.3	1.2	1.2
CRC		0.6	0.5	0.6	0.5
DMA		13.3	13.2	13.9	13.5
All APB1 Peripherals		-	-	-	-
LPTIM1		2.5	2.7	2.8	2.6
SAC-OPAMP1		19.2	19.1	18.9	-
SAC-OPAMP2		18.9	18.9	18.7	-
SAC-OPAMP3		18.9	18.8	18.7	-
SAC-OPAMP4		18.8	18.8	18.7	-
SAC-DAC		12.2	11.7	12.1	-
SAC-COMP1		12.5	11.7	12.2	-
SAC-COMP2		9.4	9.3	9.0	-
SAC-COMP3		9.1	9.4	9.1	-
SAC-COMP4		9.9	9.8	9.7	-
PWR		0.9	0.9	0.9	1.0
I2C1		8.7	8.6	8.9	8.7
I2C2	APB1	4.7	4.6	4.8	4.6
LPUART		11.4	11.4	11.9	11.6
UART2		7.5	8.4	5.6	6.1
UART3		5.1	5.2	5.2	5.0
ATK		140.4	157.6	140.2	157.2
SPI2		2.1	2.1	2.1	2.1
WWDG		0.6	0.6	0.6	0.6
LCD		0.3	0.5	0.2	0.7
TIM2		10.5	10.3	10.6	10.2
TIM3		10.0	9.7	10.0	9.8
TIM4		9.7	9.7	9.9	9.6
TIM5		1.4	1.4	1.4	1.3
TIM6		1.2	1.4	1.3	1.3
TIM7		1.3	1.3	1.3	1.3
All APB2 Peripherals		-	-	-	-
ADC		12.9	13.9	13.1	13.9
USART1	APB2	24.4	24.2	25.6	24.3
SPI1		2.4	2.3	2.4	2.4
TIM1		14.2	14.0	14.7	14.1

5.3.6 Wakeup time from low-power modes times

The wakeup times given in Table 5-3-6-1 are the latency between the event and the execution of the first user instruction.

Table 5-3-6-1 Low-power mode wakeup times

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WUSLEEP}$	Wakeup time from Sleep to Run mode	-	12	13	CPU cycles
t_{WUSTOP}	Wakeup time from Stop to Run mode	HSIKERON=0, BGR=0 (BGR, LDO, HSI deactivated before entering STOP mode)	3.1	3.3	µs
		HSIKERON=0, BGR=1 (LDO, HSI deactivated before entering STOP mode)	3.2	3.3	
		HSIKERON=1 (BGR, LDO, HSI always activated)	2.1	2.1	

Table 5-3-6-2 Wakeup time using LPUART and LPTIM

Symbol	Parameter	Conditions	Typ	Max	Unit
$t_{WULPUART}$	Wakeup time needed to calculate the maximum LPUART baud rate allowing to wakeup from Stop mode when LPUART clock source is HSI	Stop mode, 125℃	-	28.3(1)	µs
$t_{WULPTIM}$	Wakeup time needed to calculate the maximum allowing to wakeup from Stop mode when LPTIM use external clock source and external counter source.	Stop mode HSIKERON=0 (LDO, HSI deactivated before entering STOP mode, VPULL on)	-	79.2	µs
		Stop mode HSIKERON=1 (LDO, HSI always activated)	-	4.4	µs

1. Guaranteed by design.

5.3.7 External clock source characteristics

High-speed external user clock generated from an external source:

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in Section 5-3-13. See Figure 5-3-7-1 for recommended clock input waveform.

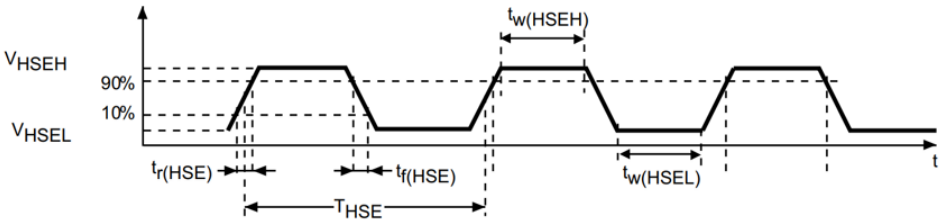


Figure 5-3-7-1 High-speed external clock source AC timing diagram

Table 5-3-7-1 High-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE_EXT}(1)	User external clock source frequency	V_{DD}=5.0V	-	16	50	MHz
V_{HSEH}(1)	OSC_IN input pin high level voltage	-	0.7V_{DD}	-	V_{DD}	V
V_{HSEL}	OSC_IN input pin low level voltage	-	V_{SS}	-	0.3V_{DD}	V
$T_{w(HSEH)}$(1) $T_{w(HSEL)}$	OSC_IN high or low time	V_{DD}=5.0V	3.77	-	-	ns

1. Guaranteed by design

Low-speed external user clock generated from an external source:

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO. The external clock signal has to respect the I/O characteristics in Section 5-3-13. See Figure 5-3-7-2 for recommended clock input waveform.

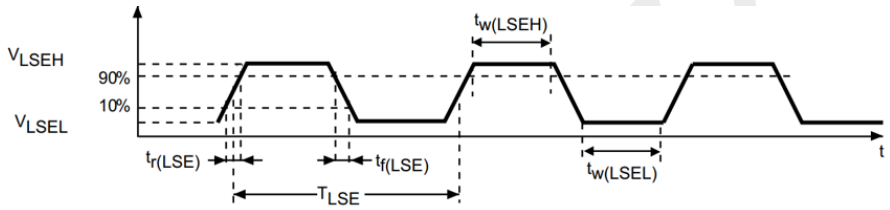


Figure 5-3-7-2 Low-speed external clock source AC timing diagram

Table 5-3-7-2 Low-speed external user clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User external clock source frequency	-	-	32.768	1000	KHz
V_{LSEH}	OSC32_IN input pin high level voltage	-	0.6V_{DDLSE}(1)	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage	-	V_{SS}	-	0.3V_{DDLSE}(1)	V
$T_{w(LSEH)}$ $T_{w(LSEL)}$	OSC32_IN high or low time	-	155	-	-	ns

1. V_{DDLSE} = 1.5V

High-speed external clock generated from a crystal/ceramic resonator:

The high-speed external (HSE) clock can be supplied with a 2 to 24 MHz crystal/ceramic resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 5-3-7-3 HSE oscillator characteristics

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	2	16	24	MHz
R_F(4)	Feedback resistor	-	-	1	-	MΩ
$I_{DD(HSE)}$	HSE current consumption	During startup (2)	-	-	1.95(4)	mA
		G0=0(3)	-	0.70	-	

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
		V_{DD} = 5V, Rm = 600Ω, CL = 20pF@2MHz				
		G0=0(3) V_{DD} = 5V, Rm = 80Ω, CL = 12pF@16MHz	-	1.06	-	
		G0=0(3) V_{DD} = 5V, Rm = 40Ω, CL = 18pF@24MHz	-	1.68	-	
		G0=1(3) V_{DD} = 5V, Rm = Ω, CL = pF@2MHz	-	1.03	-	
		G0=1(3) V_{DD} = 5V, Rm = 80Ω, CL = 12pF@16MHz	-	1.62	-	
		G0=1(3) V_{DD} = 5V, Rm = 40Ω, CL = 18pF@24MHz	-	2.65	-	
G_m(4)	Maximum critical crystal transconductance	G0=0	0.8	1.1	1.7	mA/V
		G0=1	1.6	2.2	3.3	mA/V
$t_{SU(HSE)}$(5)	Startup time	V_{DD} is stabilized	-	2.8	-	ms

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time.
3. G0=0: HSE choose normal drive capability; G0=1: HSE choose high drive capability.
4. Guaranteed by design.
5. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 16 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see Figure 5-3-7-3). C_{L1} and C_{L2} areusually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} 和 C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

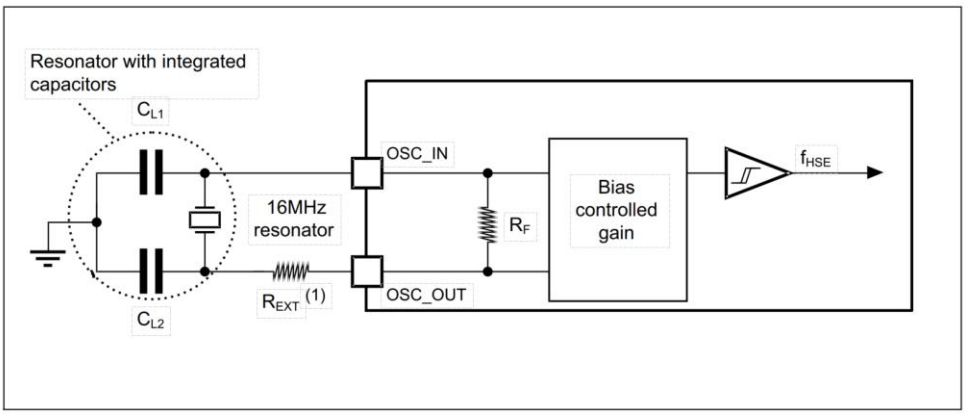


Figure 5-3-7-3 Typical application with an 16 MHz crystal

1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator:

The low-speed external (LSE) clock can be supplied with a 32.768 KHz crystal resonator oscillator. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 5-3-7-4 LSE oscillator characteristics (f_{LSE} = 32.768 KHz)

Symbol	Parameter	Conditions(1)	Min	Typ	Max	Unit
$I_{DD(LSE)}$ (1)	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	0.22	-	μ A
		LSEDRV[1:0] = 01 Medium low drive capability	-	0.27	-	
		LSEDRV[1:0] = 10 Medium low drive capability	-	0.30	-	
		LSEDRV[1:0] = 11 High drive capability	-	0.32	-	
G_m(1)	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	8	μA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	25	
		LSEDRV[1:0] = 10 Medium low drive capability	-	-	48	
		LSEDRV[1:0] = 11 High drive capability	-	-	62	
$t_{SU(LSE)}$(2)	Startup time	V_{DD} is stabilized	-	1	-	s

1. Guaranteed by design.
2. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 KHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer.

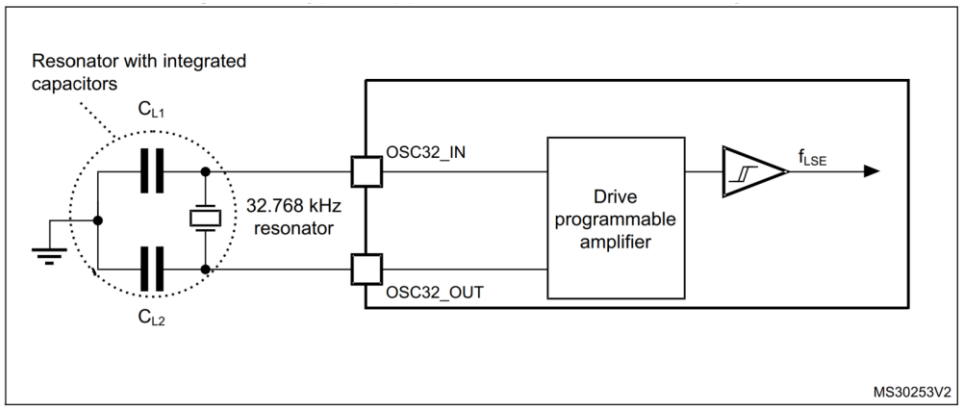


Figure 5-3-7-4 Typical application with a 32.768 KHz crystal

Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

5.3.8 Internal clock source characteristics

The parameters given in Table 5-3-8-1 to Table 5-3-8-3 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions. The provided curves are characterization results, not tested in production.

Table 5-3-8-1 HSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	HSI Frequency	V_{DD}=5.0V,T_A=25℃	7.53	18.00	35.10	f_{HSI}
$\triangle_{Temp(HSI)}$	HSI oscillator frequency drift over temperature	T_A=0 to 85℃	-1.66	-	0.20	%
		T_A=-40 to 105℃	-2.39	-	0.68	%
$\triangle_{VDD(HSI)}$	HSI oscillator frequency drift over V_{DD}	V_{DD}=2.5-6.0V	0.13	-	0.35	%
TRIM	HSI frequency user trimming step	From code 0x15F to 0x160	-	-0.04	-	%
		For all other code increments	0.09	0.21	0.28	
D_{HSI}	Duty Cycle	-	45	-	55	%
$t_{su(HSI)}$ (1)	HSI oscillator start-up time	-	-	0.2	0.2	µs
$t_{stab(HSI)}$ (1)	HSI oscillator stabilization time	-	1.0	1.7	3.0	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	387	437	µA

1. Guaranteed by design.

Table 5-3-8-2 MSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MSI}	MSI Frequency	V_{DD}=5.0V,T_A=25℃	1.57	3.69	7.07	MHz
$\triangle_{Temp(MSI)}$	MSI oscillator frequency drift over temperature	T_A=0 to 85℃	-0.53	-	0.14	%
		T_A=-40 to 105℃	-0.68	-	0.41	%
$\triangle_{VDD(MSI)}$	MSI oscillator frequency drift over V_{DD}	V_{DD}=2.5 to 6.0V	0.24	-	0.36	%
TRIM	MSI frequency user trimming step	From code 0x15F to 0x160	-	-0.01	-	%
		For all other code increments	0.01	0.20	0.31	
D_{MSI}(1)	Duty Cycle	-	45	-	55	%

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(MSI)}$ (1)	MSI oscillator start-up time	-	-	0.21	0.7	μs
$t_{stab(MSI)}$ (1)	MSI oscillator stabilization time	-	0.9	3.4	26.0	μs
$I_{DD(MSI)}$	MSI oscillator power consumption	-	-	80	88	μA

1. Guaranteed by design.

Table 5-3-8-3 LSI oscillator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD}=5.0V,T_A=25℃	31.48	32.77	46.32	KHz
$\triangle_{Temp(LSI)}$	LSI oscillator frequency drift over temperature	T_A=0 to 85℃	-1.04	-	1.66	%
		T_A=-40 to 105℃	-4.14	-	1.66	%
$\triangle_{VDD(LSI)}$	LSI oscillator frequency drift over V_{DD}	V_{DD}=2.5 to 6.0V	5.46	-	5.55	%
TRIM	LSI frequency user trimming step	From code 0x00 to 0x1F	-0.02	-	2.81	%
D_{LSI}(1)	Duty Cycle	-	45	-	55	%
$t_{su(LSI)}$ (1)	LSI oscillator start-up time	-	-	30	60	μs
$t_{stab(LSI)}$ (1)	LSI oscillator stabilization time	-	-	40	80	μs
$I_{DD(LSI)}$	LSI oscillator power consumption	-	-	0.5	-	μA

1. Guaranteed by design.

5.3.9 PLL characteristics

The parameters given in Table 5-3-9 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-9 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock frequency	-	4	-	24	MHz
D_{PLL_IN}	PLL input clock duty cycle	-	45		55	%
$f_{PLL\_Q\_IN}$	PLL multiplier output clock Q	-	9	-	72	MHz
$f_{PLL\_R\_IN}$	PLL multiplier output clock R	-	9	-	72	MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{VCO_OUT}	PLL VCO output	-	24	-	72	MHz
t_{LOCK}(1)	PLL lock time	-	-	20	30	μs
Jitter(1)	RMS period jitter	System clock 48MHz	-	420	-	ps
$I_{DD(PLL)}$ (1)	PLL power consumption on V_{DD}	HSI=18.432MHz as PLL's clock source, VCO freq=24MHz	49	61	102	μA
		HSI=18.432MHz as PLL's clock source, VCO freq=48MHz	71	85	107	
		HSI=18.432MHz as PLL's clock source, VCO freq=72MHz	103	118	157	

1. Guaranteed by design.

5.3.10 Flash memory characteristics

Table 5-3-10-1 Flash memory characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	16-bit programming time	System clock 48MHz	23	23.9	μs
	32-bit programming time		23	23.9	
t_{prog_page}	Page(1Kbytes) programming time (2bytes program each)	System clock 48MHz	11.79	11.94	ms
	Page(1Kbytes) programming time (4bytes program each)		5.85	5.95	
t_{erase_page}	Page(1Kbytes) erase time		2.17	2.22	
t_{prog_bank}	Bank(236Kbytes) programming time (2bytes program each)	System clock 48MHz	2.77	2.81	s
	Bank(236Kbytes) programming time (4bytes program each)		1.38	1.41	
t_{mass_erase}	Mass erase time		515.9	522.3	ms
$I_{DD(FlashA)}$ (1)	Average programming consumption from V_{DD}	programming time 20us	4	5	mA
	Average erase consumption from V_{DD}	Page erase time 2ms	4	5	

Table 5-3-10-2 Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min	Unit
N_{END}	Endurance	T_A=-40 to 85℃	100(1)	kcycles
t_{RET}	Data retention	T_A=-40 to 85℃	10(1)	years

1. Guaranteed by design.

5.3.11 ESD/EFT/EMI characteristics

ESD: Electrostatic discharges (a positive then a negative pulse separated by more than 1 second and 10 times each) are applied to the pins of each sample according to each pin combination, gradually increasing the voltage until it fails. A 100uF/16V and a 0.1uF electrolytic capacitors are connected between VDD pin and VSS pin. This test conforms to the JESD22 standard.

ESD test result as Table 5-3-11-1 shows.

Table 5-3-11-1 ESD absolute maximum ratings

Symbol	Parameter	Conditions	Max	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A=15~35℃, humidity = 30~60%, conforms to JESD22-A114D HBM	4	KV

EFT: A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS}, until a functional disturbance occurs.

EFT test result as Table 5-3-11-2 shows.

Table 5-3-11-2 EFT characteristics

Symbol	Parameter	Conditions	Level	Typ	Unit
V_{EFT}	-	T_A=15~35℃, humidity = 30~60%, conforms to IEC61000-4-4	4	4	KV

EMI: The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 1 LEDs through the I/O ports). This emission test is compliant with EN55014-1 standard which specifies the test board and the pin loading.

EMI test results as Table 5-3-11-3 shows.

Table 5-3-11-3 EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	OverLimit @ [f_{HSE}/f_{HCLK}]	Unit
				8MHz/18.432MHz	
S_{EMI}	QP	V_{DD}=3.3V,f_{HCLK}=18.432MHz,T_A=25℃, compliant with EN55014-1	30MHz to 300MHz	-17	dBuV

5.3.12 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below VSS or above VDDIO1 (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out-of-range parameter: ADC error above a certain limit (higher than 5 LSB TUE), induced leakage current on adjacent pins out of conventional limits (-5 µA/+0 µA range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 5-3-12 I/O current injection susceptibility

Symbol	Parameter		Functional susceptibility		Unit
			Negative injection	Positive injection	
I_{INJ}	Injected current on pin	ALL pins	-0.00017(1)	N/A	mA

1. Positive induced leakage current $V_{IN}>V_{DDIOx}$, Negative induced leakage current $V_{IN}<V_{SS}$.

5.3.13 I/O port characteristics

The parameters given in Table 5-3-13-1 to Table 5-3-13-3 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions. All I/Os are designed as CMOS- and TTL-compliant.

Table 5-3-13-1 I/O static characteristics

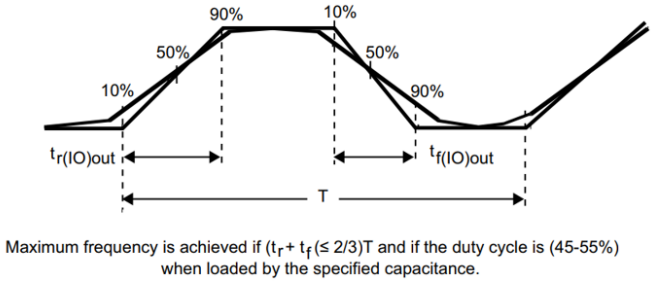
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IL}	I/O input low level voltage	V_{DD}=5.0V All GPIO pins		-	-	0.3V_{DD}	V
V_{IH}	I/O input high level voltage	V_{DD}=5.0V All GPIO pins		0.7V_{DD}	-	-	V
V_{hys}(1)	I/O input hysteresis	V_{DD}=5.0V All GPIO pins		-	-	1570	mV
I_{lkg}(1)	Input leakage current	V_{DD}=5.0V All GPIO pins		-	1	-	nA
R_{PU}	Weak pull-up equivalent resistor	$V_{IN}=V_{SS}$	GL2 type	26	30	33	KΩ
			GLC type	26	30	33	
			GLE type	26	30	33	
R_{PD}	Weak pull-down equivalent resistor(	$V_{IN}=V_{DD}$	GL2 type	12	16	18	KΩ
			GLC type	13	17	19	
			GLE type	15	17	19	
C_{IO}(1)	I/O pin capacitance	-		-	0.2	-	pF

1. Guaranteed by design.

Table 5-3-13-2 I/O voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	V_{DD}=5.0V, $\|I_{IO}\|$=40mA All GPIO pins	-	-	0.4	V
		V_{DD}=5.0V, $\|I_{IO}\|$=115mA All GPIO pins	-	-	1.5	
V_{OH}	Output high level voltage for an I/O pin	V_{DD}=5.0V, $\|I_{IO}\|$=26mA All GPIO pins	3.5	-	-	V
		V_{DD}=5.0V, $\|I_{IO}\|$=8mA All GPIO pins	4.6	-	-	

The definition and values of input/output AC characteristics are given in Figure 5-3-13-1 and Table 5-3-13-3.



Maximum frequency is achieved if (t_r + t_f (≤ 2/3)T and if the duty cycle is (45-55%) when loaded by the specified capacitance.

Figure 5-3-13-1 I/O AC characteristics

Table 5-3-13-3 I/O AC characteristics (1)

Symbol	Parameter	Conditions	Min	Max	Unit
F_{max}	Maximum frequency	V_{DD}=3.3V, C=30pF All GPIO pins	-	75	MHz
		V_{DD}=5.0V, C=30pF All GPIO pins	-	75	
T_r	Output rise time	V_{DD}=3.3V, C=30pF All GPIO pins	2.5	10.0	ns
		V_{DD}=5.0V, C=30pF All GPIO pins			
T_f	Output fall time	V_{DD}=3.3V, C=30pF All GPIO pins	1.0	5.0	ns
		V_{DD}=5.0V, C=30pF All GPIO pins			

1. Guaranteed by design.

5.3.14 NRST input characteristics

NRST input driver uses CMOS technology. It is connected to a permanent pull-up resistor R_{PU}.

The parameters given in Table 5-3-14 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-14 NRST pin characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage	2.0V<V_{DD}<5.5V	-	-	0.3V_{DD}	V
$V_{IH(NRST)}$	NRST input high level voltage	2.0V<V_{DD}<5.5V	0.7V_{DD}	-	-	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	2.0V<V_{DD}<5.5V	-	-	1570	V
R_{PU}	Weak pull-up equivalent resistor	2.0V<V_{DD}<5.5V V_{IN}=V_{SS}	13	16	18	KΩ
$V_{F(NRST)}$	NRST input filtered pulse	-	20.0	-	-	μs

1. Guaranteed by design.

5.3.15 OPAMP characteristics

The parameters given in Table 5-3-15 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-15 OPAMP characteristics (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	V_{DD} = 3.3V	2.4	-	5.5	V
R_{AIN}(1)	External input impedance	V_{DDA}=V_{DD}	-	10^4	-	KΩ
R_{AOUT}(1)	OPAMP output resistance	V_{DDA}=V_{DD}	-	34.6	-	Ω
$V_{OUT(OPAMP)}$	OPAMP output voltage range	V_{DDA}=V_{DD} = 5V	0.00056	-	V_{DDA}-0.02200	V
V_{icm}	Common mode input range	V_{DDA}=V_{DD} = 3.3V	0.0	-	2.1	V
		V_{DDA}=V_{DD} = 5V	0.0	-	3.8	V
Gain	PGA gain	V_{in}=21mV,SOPG[2:0]=000	-	0.5	-	V/V
		V_{in}=21mV,SOPG[2:0]=001	-	0.6	-	
		V_{in}= 21mV,SOPG[2:0]=010	-	0.7	-	
		V_{in}=21mV,SOPG[2:0]=011	-	0.8	-	
		V_{in}=21mV,SOPG[2:0]=100	-	2.1	-	
		V_{in}=21mV,SOPG[2:0]=101	-	2.1	-	
		V_{in}=21mV,SOPG[2:0]=110	-	2.3	-	
		V_{in}=21mV,SOPG[2:0]=111	-	2.3	-	
CMRR(1)	Common mode rejection ratio	V_O=5.0V	100	113	-	dB
PSRR(1)	Power supply rejection ratio	V_O=5.0V	75	142	-	dB
R_{Slew_rate}	Slew rate	SR+,No load	-	2.80	-	V/μs
		SR-,No load	-	1.04	-	
PM(1)	Phase margin	RL=1Mohm,CL=100pF	45	54	-	deg
		RL=1Mohm,CL=10pF	75	81	-	
V_{offset}	Offset voltage	V_{in} = 200mV, not calibrated	-	3.5	-	mV
		V_{in} = 1.7V, not calibrated	-	2.5	-	
		V_{in} = 3.6V, not calibrated	-	4.4	-	
		V_{in} = 200mV, has calibrated	-	0.8	-	
		V_{in} = 1.7V, has calibrated	-	0.9	-	
		V_{in} = 3.6V, has calibrated	-	0.3	-	
GBW	Gain Bandwidth Product	V_{DDA}=V_{DD} = 5V	-	1.2	-	MHz
t_{STAB}	Stable time (from OPAMP enable to stabilized output while jitter less than 0.6%)	V_{DDA}=V_{DD} = 5V, forward amplification mode (SOPM=0x06), PGA gain is 20 times, OPAMP input voltage is 240mV.	-	6.4	-	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(OPAMP)}$	OPAMP consumption from V_{DDA}	VDDA = 5V, forward input voltage = 2.5V, open-loop mode	-	0.6	-	mA

1. Guaranteed by design.
2. Test result under 25℃ condition.

5.3.16 ADC characteristics

The parameters given in Table 5-3-16-1 to Table 5-3-16-3 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-16-1 ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	$V_{DDA}=V_{REF+}$	2.0	-	5.5(1)	V
V_{REF+}	Positive reference voltage	V_{DDA}=5.0V	2.4	-	V_{DDA}	V
f_{ADC}	ADC clock frequency	f_{ADC} use PLL=48MHz	0.6(1)	-	27.0	MHz
		f_{ADC} use HSI=18MHz	0.6(1)	-	18.0	
f_s	Sampling rate	f_{ADC}=27MHz,12bits	-	-	1.80	MSps
f_{TRIG}	External trigger frequency	f_{ADC}=27MHz,12bits	-	-	1.50	MHz
		f_{ADC}=others,12bits	-	-	fadc/18	MHz
V_{AIN}	Conversion voltage range	$V_{DDA}=V_{REF+}$=5.0V	V_{SSA}	-	V_{REF+}	V
R_{AIN}	External input impedance	$V_{DDA}=V_{REF+}$=5.0V,Vin=V_{REF+}/2	-	-	20	KΩ
C_{ADC}(1)	Internal sample and hold capacitor	-	-	9	-	pF
t_{STAB}(1)	ADC power-up time	-	0.8	-	-	µs
t_{CAL}	Calibration time	f_{ADC}=14MHz	5.35			µs
		f_{ADC}=others	75			1/f_{ADC}
t_{LATR}	Trigger conversion latency	EXTEN=00	4			1/f_{ADC}
		EXTEN=01	4			
		EXTEN=10	4			
		EXTEN=11	4			
t_s	Sampling time	f_{ADC}=14MHz,2.4V<V_{DDA}<5.5V	0.179	-	14.607	µs
			2.5	-	240.5	1/f_{ADC}
t_{CONV}	Total conversion time (including sampling time)	f_{ADC}=14MHz,12bits	1.071	-	18.071	µs
		f_{ADC}=others,12bits	15	-	253	1/f_{ADC}
t_{IDLE}	Laps of time allowed between two conversions without rearm	f_{ADC}=14MHz,SMP=2.5cycle	1.0	-	-	µs
$I_{VCC\_ADC(ADC)}$	ADC consumption from V_{VCC_ADC}	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA}	250	460	531	µA
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA}	205	217	269	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA}	250	460	531	

$I_{VREF+(ADC)}$	ADC consumption from V_{REF+}	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA}	58	111	133	μA
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA}	57	109	132	

1. Guaranteed by design.

Table 5-3-16-2 Maximum ADC R_{AIN}

Resolution	Sampling cycle at 48MHz	Sampling time at 14MHz[ns]	Max. R_{AIN}(Ω)
12bits	2.5	179	1.2K
	4.5	321	1.5K
	8.5	607	1.9K
	13.5	964	2.7K
	20.5	1464	3.1K
	40.5	2893	6.9K
	80.5	5750	11.2K
	120.5	8607	17.0K
	160.5	11464	18.0K
	200.5	14321	19.0K
	240.5	17179	20.0K

Table 5-3-16-3 ADC accuracy

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
E_O	Offset error	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-12.0	-4.0	-3.0	LSB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-14.3	-12.3	-7.0	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-13.4	-12.0	-7.9	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-12.0	-3.0	-2.0	
E_{DNL}	Differential linearity error	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-1.0	2.5	2.5	LSB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-1.0	2.7	2.7	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-1.0	0.9	1.5	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-1.0	0.9	1.6	
E_{INL}	Integral linearity error	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-2.9	1.9	2.7	LSB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-3.0	1.9	2.7	

		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-2.1	0.6	2.7	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-1.9	1.3	2.7	
ENOB	Effective number of bits	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	10	11	11	bit
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	10	10	10	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	10	10	10	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	10	11	11	
SINAD	Signal-to-noise and distortion ratio	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	62	65	65	dB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	60	61	63	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	60	61	63	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	63	66	66	
SNR	Signal-to-noise ratio	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	60	65	65	dB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	60	61	63	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	63	65	65	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	63	67	67	
THD	Total harmonic distortion	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-81	-81	-72	dB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-74	-73	-72	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	-76	-63	-62	
		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	-79	-77	-75	
SFDR	Spurious-free Dynamic Range	f_s=1MSps, adc buffer on, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	70	84	84	dB
		f_s=1MSps, adc buffer on, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	71	77	77	
		f_s=1MSps, adc buffer off, V_{DDA} =2.3~2.7v, V_{REF+}<V_{DDA},T_A=25℃	62	64	78	

		f_s=1MSps, adc buffer off, V_{DDA} =2.7~5.5v, V_{REF+}<V_{DDA},T_A=25℃	76	80	83	

ADC accuracy characteristics are defined as Figu 5-3-16-1.

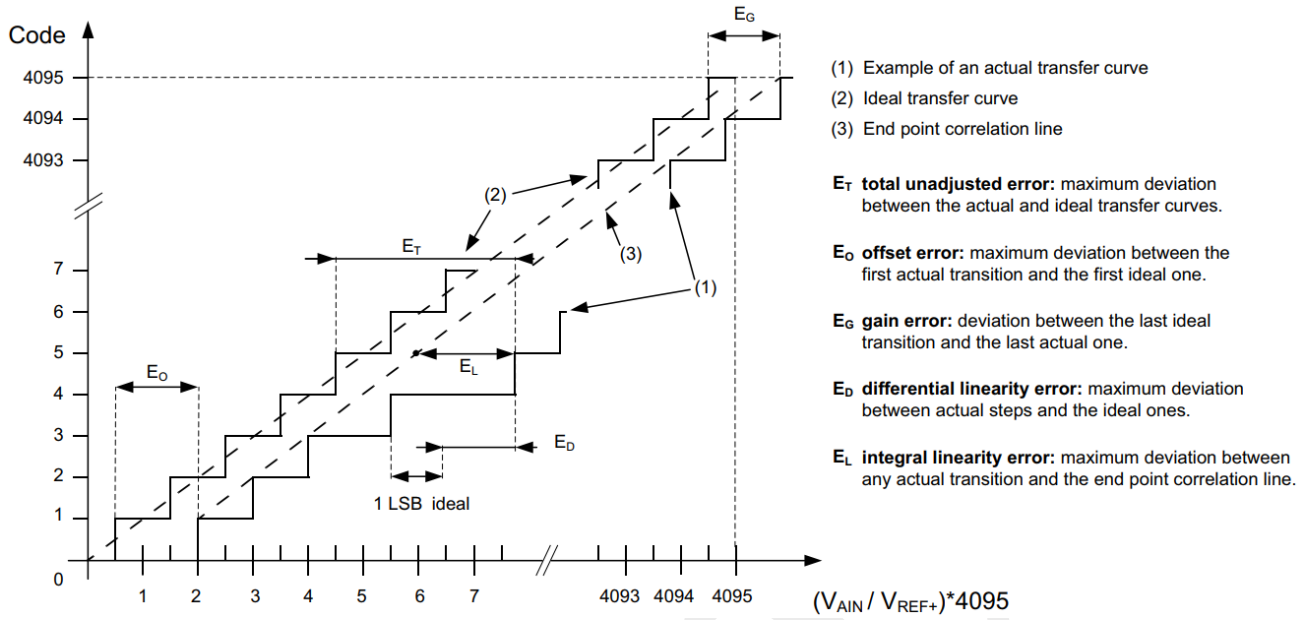


Figure 5-3-16-1 ADC accuracy characteristics

5.3.17 DAC characteristics

The parameters given in Table 5-3-17-1 to Table 5-3-17-2 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-17-1 DAC characteristics (2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	1.6V<V_{DD}<6.0V;DAC output buffer off		1.6	-	6.0	V
		1.6V<V_{DD}<6.0V;DAC output buffer on		1.7	-	6.0	
V_{REF+}	Positive reference voltage	1.6V<V_{DD}<6.0V;DAC output buffer off		1.6	-	6.0	V
		1.6V<V_{DD}<6.0V;DAC output buffer on		1.7	-	6.0	
R_L(1)	Resistive load	DAC output buffer on	Connect to V_{SSA}	-	38	-	KΩ
			Connect to V_{DDA}	-	38	-	
R_O(1)	Output Impedance	DAC output buffer off		5.9	11.3	16.1	KΩ
C_L(1)	Capacitive load	DAC output buffer on		-	-	50	pF
V_{DAC_OUT}	Voltage on DAC_OUT output	VDDA=5.0V, DAC output buffer on		0.008	-	4.410	V
		VDDA=5.0V, DAC output buffer off		0.006	-	4.980	
$t_{SETTLING}$	Settling time		VDDA=2.2V	-	-	3.76	μs

		Buffer on;code value modified from 0x000 to 0xB87; no CL; no RL	VDDA=3.3V	-	-	3.25	
			VDDA=5.0V	-	-	4.18	
		Buffer off;code value modified from 0x000 to 0xE46; no CL;no RL	VDDA=2.2V	-	-	2.82	
			VDDA=3.3V	-	-	2.82	
			VDDA=5.0V	-	-	2.74	
PSRR(1)	V_{DDA} supply rejection ratio	Buffer on		-75	-90	-	dB
SR	Slew rate	VDDA=5.0V;buffer on;SR+		-	2.05	-	V/μs
		VDDA=5.0V;buffer on;SR-		-	0.74	-	
		VDDA=5.0V;buffer off;SR+		-	3.28	-	
		VDDA=5.0V;buffer off;SR-		-	3.13	-	
I_{leak}(1)	Output leakage current	-		-	1	-	nA
V_{offset}	Middle code offset for 1 trim code step	V_{REF+}=5.0V		24	-	1914	μV
		V_{REF+}=3.3V		3	-	1842	
$I_{DDA(DAC)}$	DAC consumption from V_{DDA}	DAC output buffer on	No load, consumption difference between code=0x955 and code=0x000	-	762	-	μA
		DAC output buffer off		-	464	-	
$I_{DDA(BUFFER)}$	DAC's BUFFER consumption from V_{DDA}	DAC output buffer on/off	No load, code=0x000, consumption difference between dac buffer on/off	-	156	-	μA
			No load, code=0x955, consumption difference between dac buffer on/off	-	454	-	

1. Guaranteed by design.
2. Test result under 25℃ condition.

Table 5-3-17-2 DAC accuracy (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	Differential non linearity	V_{DD}=5.0V;DAC output buffer on; CL=0.1uF;no RL	-2.0	-	2.0	LSB

		V_{DD}=5.0V; DAC output buffer off; CL=0.1uF;no RL	-2.0	-	2.0	
INL	Integral non linearity	V_{DD}=5.0V; DAC output buffer on; CL=0.1uF;no RL	-13.0	-	13.0	LSB
		V_{DD}=5.0V; DAC output buffer off; CL=0.1uF;no RL	-13.0	-	13.0	
Offset	Offset error at code 0x800	DAC output buffer on;CL=0.1uF;no RL	-	±4.5	-	LSB
		DAC output buffer off;CL=0.1uF;no RL	-	±4.3	-	
Offset1	Offset error at code 0x001	DAC output buffer on;CL=0.1uF;no RL	-	±8.5	-	LSB
		DAC output buffer off;CL=0.1uF;no RL	-	±7.0	-	
TUE	Total unadjusted error	DAC output buffer on;CL=0.1uF;no RL	-36.8	-	11.4	LSB
		DAC output buffer off;CL=0.1uF;no RL	-35.1	-	8.5	
TUECal	Total unadjusted error after calibration	DAC output buffer on;CL=0.1uF;no RL	-40.0	-	9.8	LSB
		DAC output buffer off;CL=0.1uF;no RL	-38.4	-	8.5	
THD	Total harmonic distortion	DAC output buffer on;CL=0.1uF;no RL;f_{out}=1.22Hz;f_s=2KHz;Dots=8192	-	-61	-	dB
		DAC output buffer off;CL=0.1uF;no RL;f_{out}=1.22Hz;f_s=2KHz;Dots=8192	-	-49	-	

1. Test result under 25℃ condition.

Note: Definitions of parameters in DAC refers to Section 5.3.16.

5.3.18 ATK characteristics

Table 5-3-18-1 ATK characteristics (3)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}(1)	Analog supply voltage	2.0V<V_{DD}<5.5V	2.9(1)	5(1)	5.5(1)	V
$t_{OC(TKx)}$	Time consumption for single channel convert	TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=000	16.22	16.60	16.63	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=000	2.93	2.97	2.98	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=000	5.84	5.92	5.94	ms
		TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=100	8.79	8.99	9.10	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=100	1.58	1.60	1.61	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=100	2.90	3.20	3.21	ms

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=111	4.94	5.04	5.09	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=111	0.89	0.89	0.90	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=111	1.78	1.78	1.79	ms
$t_{AC(TKx)}$	Time consumption for all channels convert	TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=000	380.62	384.83	386.67	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=000	64.56	65.33	65.63	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=000	128.72	130.24	130.82	ms
		TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=100	203.99	207.12	207.73	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=100	34.78	35.329	35.44	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=100	69.34	70.52	70.68	ms
		TKxTMR[11:0]=0x000; TKxJMPVAL[2:0]=111	114.97	115.74	117.26	μs
		TKxTMR[11:0]=0x800; TKxJMPVAL[2:0]=111	19.64	19.68	19.80	ms
		TKxTMR[11:0]=0xFFF; TKxJMPVAL[2:0]=111	38.49	39.16	39.22	ms
I_{lkg}(1)	Leakage current	Ivdda	-	10	1800	nA
		Ivdd	-	5	900	nA
f_{JMPVAL}	Frequency adjustment range	TKxJMPVAL[2:0]=000	1.34	1.38	1.40	MHz
		TKxJMPVAL[2:0]=001	1.54	1.57	1.59	
		TKxJMPVAL[2:0]=010	2.09	2.15	2.15	
		TKxJMPVAL[2:0]=011	2.39	2.44	2.45	
		TKxJMPVAL[2:0]=100	2.49	2.55	2.59	
		TKxJMPVAL[2:0]=101	2.88	2.93	2.97	
		TKxJMPVAL[2:0]=110	3.86	3.96	3.98	
		TKxJMPVAL[2:0]=111	4.45	4.54	4.57	
D_{JMPVAL}	Duty cycle adjustment range	TKxJMPVAL[2:0]=000	50.14	50.17	50.19	%
		TKxJMPVAL[2:0]=001	50.19	50.22	50.24	
		TKxJMPVAL[2:0]=010	50.18	50.29	50.32	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		TKxJMPVAL[2:0]=011	50.18	50.27	50.34	
		TKxJMPVAL[2:0]=100	53.61	53.65	53.85	
		TKxJMPVAL[2:0]=101	53.82	53.83	53.89	
		TKxJMPVAL[2:0]=110	53.99	54.50	54.88	
		TKxJMPVAL[2:0]=111	54.30	54.90	55.20	
L_{cap}[(1)(2)]	External capacitor range	-	3.3	-	21.6	pF
T_{spread}	Spread frequency period	TKxSPEAD=1, TKxJMPVAL[2:0]=000	90.9	92.9	94.9	µs
		TKxSPEAD=1, TKxJMPVAL[2:0]=001	90.9	92.9	94.9	
		TKxSPEAD=1, TKxJMPVAL[2:0]=010	59.3	59.7	61.1	
		TKxSPEAD=1, TKxJMPVAL[2:0]=011	59.3	59.7	61.1	
		TKxSPEAD=1, TKxJMPVAL[2:0]=100	45.7	46.6	47.5	
		TKxSPEAD=1, TKxJMPVAL[2:0]=101	45.7	46.6	47.5	
		TKxSPEAD=1, TKxJMPVAL[2:0]=110	29.8	30.0	30.6	
		TKxSPEAD=1, TKxJMPVAL[2:0]=111	29.8	30.0	30.6	
f_{spread}	Spread frequency width	TKxSPEAD=1, TKxJMPVAL[2:0]=000	0.38	0.38	0.39	MHz
		TKxSPEAD=1, TKxJMPVAL[2:0]=001	0.38	0.38	0.39	
		TKxSPEAD=1, TKxJMPVAL[2:0]=010	0.58	0.58	0.59	
		TKxSPEAD=1, TKxJMPVAL[2:0]=011	0.58	0.58	0.59	
		TKxSPEAD=1, TKxJMPVAL[2:0]=100	0.76	0.80	0.80	
		TKxSPEAD=1, TKxJMPVAL[2:0]=101	0.76	0.80	0.80	
		TKxSPEAD=1, TKxJMPVAL[2:0]=110	1.16	1.20	1.21	
		TKxSPEAD=1, TKxJMPVAL[2:0]=111	1.16	1.20	1.21	
tSU(TKx)	Startup time for TKx			804[(1)]		ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ITRIM	Trimming	TKxIVCS=0; Cload = 0pF	0x65	0x6C	0x6E	--
		TKxIVCS=1; Cload = 0pF	0x68	0x6E	0x70	--
I_{start}	TKx's current consumption from V_{DDA}	V_{DD}=5.0V, START=1, TKxJMPVAL[2:0]=000	2.69	3.05	3.09	mA
I_{stop}		V_{DD}=5.0V, START=0, TKxJMPVAL[2:0]=000	2.78	3.13	3.19	

1. Guaranteed by design.
2. TK value in the RKx RAM refers to Table 5-3-18-2 TKx when connect to different capacitors.
3. Test result under 25℃ condition.

Table 5-3-18-2 ATK value when connect to different capacitors (4)

Symbol	Parameter(3)	Conditions	TKxTMR max scan length(1)	TK value in RAM	Difference between adjancent 0.5pF(2)
TKxRAM Code	TKxJMPVAL[2:0]=000	Cload=3.5pF	1517	15005	327
		Cload=4.0pF		14678	
		Cload=5.0pF	1577	15027	326
		Cload=5.5pF		14701	
		Cload=10.0pF	1776	15025	290
		Cload=10.5pF		14735	
		Cload=15.0pF	1967	15016	255
		Cload=15.5pF		14761	
		Cload=20.0pF	2155	15015	205
		Cload=20.5pF		14810	
		Cload=25.0pF	2330	15022	182
		Cload=25.5pF		14840	
		Cload=30.0pF	2500	15008	169
		Cload=30.5pF		14839	
		Cload=35.0pF	2639	15012	145
		Cload=35.5pF		14867	
		Cload=40.0pF	2841	15002	115
		Cload=40.5pF		14887	
		Cload=45.0pF	2967	15000	98
		Cload=45.5pF		14902	
		Cload=50.0pF	3095	15000	85
		Cload=50.5pF		14915	
	TKxJMPVAL[2:0]=111	Cload=3.5pF	4095	12482	242
		Cload=4.0pF	4095	12240	
		Cload=5.0pF	4095	12055	217
		Cload=5.5pF	4095	11838	

Symbol	Parameter[3]	Conditions	TKxTMR max scan length[1]	TK value in RAM	Difference between adjancent 0.5pF[2]
		Cload=10.0pF	4095	10991	143
		Cload=10.5pF	4095	10848	
		Cload=15.0pF	4095	10327	93
		Cload=15.5pF	4095	10234	
		Cload=20.0pF	4095	9908	78
		Cload=20.5pF	4095	9830	
		Cload=25.0pF	4095	9618	50
		Cload=25.5pF	4095	9568	
		Cload=30.0pF	4095	9408	24
		Cload=30.5pF	4095	9384	
		Cload=35.0pF	4095	9308	14
		Cload=35.5pF	4095	9294	

1. Max scan length: It means under current capacitor, in case of TK value not overflow, the max length TKxTMR can achieve. If TKxTMR value configured more than the max length, then overflow will occurs.
2. The difference between adjancent 0.5pF: It represents the sensitivity in touch key's recognition. The bigger the value is, the high sensitivity the touch key has; The smaller the value is, the low sensitivity the touch key has.
3. The smaller the value of JMPVAL[2:0] is, the lower the TK's clock frequency is, the higher the TK sensitivity is; The bigger the value of JMPVAL[2:0] is, the higher the TK's clock frequency is, the lower the TK sensitivity is. Customer can configure the JMPVAL[2:0] according to application.
4. Test result under 25℃ condition.

5.3.19 LCD/LED characteristics

The parameters given in Table 5-3-19-1 to Table 5-3-19-2 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-19-1 LCD characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power voltage	-	2.5	5.0	6.0	V
I_{DD}	Current consumption from V_{DD}	V_{DD}=5.0V	10.7	18.6	337.7	μA
DUTY	Duty cycle	1/4 duty	24.59	25.03	25.45	%
		1/5 duty	19.81	19.90	20.16	
		1/6 duty	16.51	16.76	16.87	
		1/8 duty	12.20	12.56	12.80	
VLCD	Highest voltage at COM	V_{DD}=5.0V Brightness level=0	2.95	2.98	2.99	V
		V_{DD}=5.0V Brightness level=4	3.92	3.96	3.97	
		V_{DD}=5.0V Brightness level=7	4.93	4.95	4.98	

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
1/3VLCD	Third of highest voltage at COM	V_{DD}=5.0V Brightness level=0	0.95	0.96	0.98	V
		V_{DD}=5.0V Brightness level=4	1.27	1.28	1.29	
		V_{DD}=5.0V Brightness level=7	1.58	1.60	1.63	
2/3VLCD	Two thirds of highest voltage at COM	V_{DD}=5.0V Brightness level=0	1.97	2.00	2.02	V
		V_{DD}=5.0V Brightness level=4	2.62	2.65	2.67	
		V_{DD}=5.0V Brightness level=7	3.28	3.31	3.36	
t_{set}(1)	Setup time	<0.1%	-	-	0.1	ms
t_{change}(1)	Change time	<0.1%	1.40	3.54	7.00	μs
t_{tran}(1)	Transfer time	<0.1%	1.00	1.95	3.00	μs
PSRR(1)	VHS supply rejection ratio	Freq=48MHz	-	-	-45	dB
		Freq=24MHz	-	-	-50	
		Freq=18.43MHz	-	-	-55	
		Freq=1Hz	-	-	-140	
	VLS supply rejection ratio	Freq=48MHz	-	-	-40	dB
		Freq=24MHz	-	-	-50	
		Freq=18.43MHz	-	-	-50	
		Freq=1Hz	-	-	-140	
	VHC supply rejection ratio	Freq=48MHz	-	-	-40	dB
		Freq=24MHz	-	-	-45	
		Freq=18.43MHz	-	-	-50	
		Freq=1Hz	-	-	-140	
	VLC supply rejection ratio	Freq=48MHz	-	-	-40	dB
		Freq=24MHz	-	-	-45	
		Freq=18.43MHz	-	-	-45	
		Freq=1Hz	-	-	-110	

1. Test result under 25℃ condition.

Table 5-3-19-2 LED characteristics (1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	Power voltage	-	2.5	5.0	6.0	V
I_{DD}	Current consumption from V_{DD}	Brightness level=0, constant current mode	-	0.30	-	mA
		Brightness level=1, constant current mode	-	2.48	-	
		Brightness level=2, constant current mode	-	4.97	-	
		Brightness level=3, constant current mode	-	9.95	-	
		Brightness level=4, constant current mode	-	19.65	-	

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
		Brightness level=5, constant current mode		-	38.95	-	
		Brightness level=6, constant current mode		-	82.45	-	
		Brightness level=7, constant current mode		-	161.65	-	
DUTY	Duty cycle	1/2 duty		49.21	49.33	50.04	%
		1/3 duty		32.81	32.88	33.35	
		1/4 duty		24.60	24.66	25.02	
		1/5 duty		19.27	19.73	20.02	
		1/6 duty		16.40	16.44	16.68	
		1/7 duty		14.06	14.09	14.29	
		1/8 duty		12.30	12.33	12.51	
I_{drive}	Drive current	Constant voltage mode	COM voltage: 2V	-	43.86	-	mA
			COM voltage: 3.5V	-	30.04	-	
			COM voltage: 4V	-	21.44	-	
			COM voltage: 4.6V	-	8.67	-	
		Constant current mode	COM voltage: 2.31V	-	23.26	-	
			COM voltage: 3.56V	-	20.94	-	
			COM voltage: 3.96V	-	19.76	-	

1. Test result under 25℃ condition.

5.3.20 COMP characteristics

The parameters given in Table 5-3-20 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

Table 5-3-20 COMP characteristics (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	2.0V<V_{DD}<5.5V	1.6	-	6.0	V
V_{IN}	Comparator input voltage range	V_{DDA}=V_{DD}=5.0V	0.0	-	5.3	V
Vicm1	CMP common mode input range	V_{DDA}=5.0V	0.0	-	4.6	V
Tsetup1(1)	CMP setup time after PD on	PD=0	-	1	42	ns
Trespond1	CMP response time after input change	cip/cin change	29.4	-	36.0	ns
R_{Slew_rate}	Slew rate	SR+,No load	-	969	-	V/μs
		SR-,No load	-	1367	-	
t_{START}(1)	Comparator startup time to reach propagation delay specification	V_{DDA}=V_{DD}	-	-	2	μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_D(1)	Propagation delay	200mV step, 100mV overdrive	-	17	35	ns
V_{hys}	Comparator hysteresis	V_{DDA}=V_{DD}	-	22	-	mV
I_d(1)	Current consumption after PD off	PD=1	-	30	-	nA
$I_{DDA(COMP)}$	Comparator consumption from V_{DDA}	Static	-	54	-	µA
		50KHz, ±100mV overdrive square signal	-	74	-	

1. Guaranteed by design
2. Test result under 25℃ condition.

5.3.21 Temperature sensor characteristics

Table 5-3-21 TS characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	V_{DD}=5.0V	-	±1	±2	℃
Avg_Slope	Average slope	V_{DD}=5.0V	-1.6872	-1.6368	-1.5466	mV/℃
$V_{25℃}$	Voltage at 25℃ (±5℃)	V_{DD}=5.0V	711.56	716.44	743.16	mV
$t_{START(TS\_BUF)}$	Sensor Buffer Start-up time in continuous mode	-	-	400	-	ns
t_{S_temp}	ADC sampling time when reading the temperature	-	2.5	-	239.5	f_{adc}
$I_{DDA(TS)}$	Temperature sensor consumption from V_{DDA}, when selected by ADC	V_{DD}=5.0V	-	26	40	µA

1. Guaranteed by design.

5.3.22 TIMx characteristics

The parameters given in the following tables are guaranteed by design. Refer to Section 5.3.13 for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 5-3-22-1 TIMx (1) characteristics

Symbol	Parameter	Conditions	Min	Typ	Max
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz	20.83	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	其他	-	$f_{TIMxCLK}$/2	MHz
		$f_{TIMxCLK}$=48MHz	-	24	
Res_{TIM}	Timer resolution	TIMx	-	16	bit
$t_{COUNTER}$	16-bit counter clock period	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=48MHz	0.02083	1365	µs

1. TIMx, is used as a general term in which x stands for 1,2, 3, 4, 5, 6 or 7.

Table 5-3-22-2 IWDG min/max timeout period at LSI=32KHz

Prescaler divider	PR[2:0]bits	Min timeout RLR[11:0]=0x000	Max timeout RLR[11:0]=0xFFF	Unit
/4	0	0.125	512	ms
/8	1	0.250	1024	
/16	2	0.500	2048	
/32	3	1.0	4096	
/64	4	2.0	8192	
/128	5	4.0	16384	
/256	6 或 7	8.0	32768	

5.3.23 Characteristics of communication interfaces

The parameters given in Table 5-3-23-1 to Table 5-3-23-3 are derived from tests performed under the ambient temperature condition summarized in Table 5-3-1: General operating conditions.

I2C-bus interface characteristics:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s.
- Fast-mode (Fm): with a bit rate up to 400 kbit/s.
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

Table 5-3-23-1 Minimum I2CCLK frequency

Symbol	Parameter	Conditions		Typ	Unit
$f_{I2CCLK(min)}$	Minimum I2CCLK frequency for correct operation of I2C peripheral	Standard-mode		2.2	MHz
		Fast-mode	DNF=0	8.8	
			DNF=1	8.8	
		Fast-mode Plus	DNF=0	22.1	
			DNF=1	23.9	

SPI's additional general conditions are:

- BR[2:0]=010(DIV8).
- Capacitive load C=30pF.
- Measurement points at CMOS levels: $0.5 \times V_{DD}$.

Refer to Section 5.3.13 for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 5-3-23-2 SPI characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$f_{SCK(max)}$	SPI clock frequency	SYSCLK=48MHz;DMA mode (transfer only); Master mode	-	-	24	MHz
		SYSCLK=48MHz;DMA mode (receive only); Slave mode			8	
		SYSCLK=48MHz;DMA mode (receive only); Master mode			6	
		SYSCLK=48MHz;DMA mode (receive only); Slave mode			10	
		SYSCLK=48MHz;DMA mode (transfer and receive); Master mode			6	
		SYSCLK=48MHz;DMA mode (transfer and receive); Slave mode			8	
$t_{SU(NSS)}$(1)	NSS setup time	Slave mode	1	-	-	ns
$t_{W(SCKH)}$	SCK high time	Master mode	$1 / f_{SCK} / 2 - 1.5$	$1 / f_{SCK} / 2$	$1 / f_{SCK} / 2 + 1.5$	ns
$t_{W(SCKHL)}$	SCK low time	Master mode				
$t_{SU(MI)}$(1)	Master data input setup time	Master mode	1	-	-	ns
$t_{SU(SI)}$(1)	Slave data input setup time	Slave mode	1	-	-	ns
$t_{h(MI)}$(1)	Master data input hold time	Master mode	3	-	-	ns
$t_{h(SI)}$(1)	Slave data input hold time	Slave mode	1	-	-	ns
$t_{a(SO)}$(1)	Data output access time	Slave mode	9	-	54	ns
$t_{dis(SO)}$(1)	Data output disable time	Slave mode	9	-	22	ns
$t_{v(SO)}$(1)	Slave data output valid time	$2.0V<V_{DD}<5.5V$	-	11	24	ns
$t_{v(MO)}$(1)	Master data output valid time	-	-	5	8	ns
$t_{h(SO)}$(1)	Slave data output hold time	-	5	-	-	ns
$t_{h(MO)}$(1)	Master data output hold time	-	1	-	-	ns

USART's additional general conditions are:

- BRR[15:0]=Max baudrate.
- Capacitive load C=30pF.
- Measurement points at CMOS levels: $0.5 \times V_{DD}$.

Refer to Section 5.3.13 for more details on the input/output alternate function characteristics (NSS, CK, TX, and

RX for USART).

Table 5-3-23-3 USART characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	USART clock frequency	Master mode	-	-	6	MHz
		Slave mode	-	-	5(1)	
$t_{SU(NSS)}$ (1)	NSS setup time	Slave mode	Tker+1.4	-	-	ns
$t_{h(NSS)}$ (1)	NSS hold time	Slave mode	-1.4	-	-	ns
$t_{W(CKH)}$	CK high time	Master mode	1 / f_{CK} / 2 -10	1 / f_{CK} / 2	1 / f_{CK} / 2 +10	ns
$t_{W(CKHL)}$	CK low time					
$t_{SU(RX)}$ (1)	Data input setup time	Master mode	Tker+0.7	-	-	ns
		Slave mode	Tker+0.6	-	-	
$t_{h(RX)}$ (1)	Data input hold time	Master mode	-0.7	-	-	ns
		Slave mode	-0.6	-	-	
$t_{V(TX)}$ (1)	Data output valid time	Master mode	-	127	135	ns
		Slave mode	-	216	242	
$t_{h(TX)}$ (1)	Data output hold time	Master mode	0.03	-	-	ns
		Slave mode	0.89	-	-	

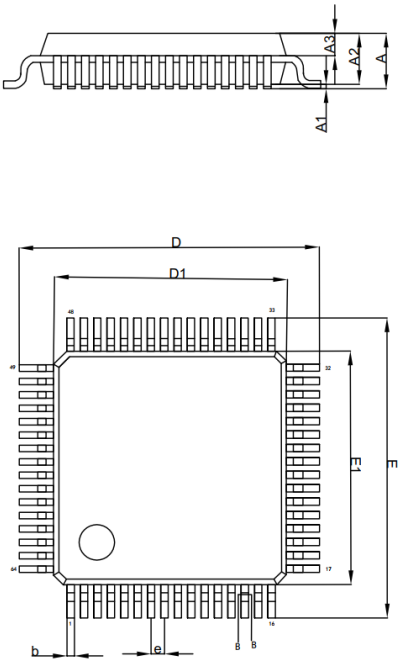
1. Guaranteed by design.

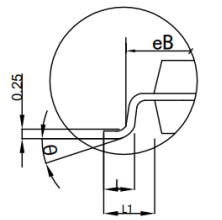
6 Package information

TM32G078 offers two package types including LQFP64 and LQFP48, each of them meet the JEDEC Standard. Package information as described below.

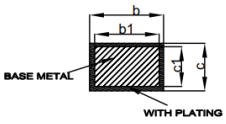
6.1 LQFP64 package information

LQFP64 is a 64-pin, 7 x 7 mm low-profile quad flat package.





DETAIL F



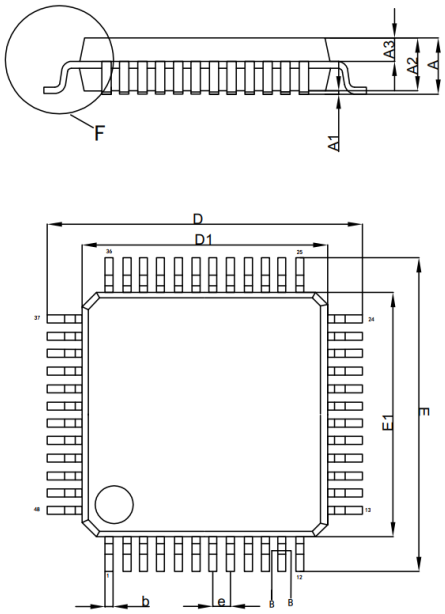
SECTION B-B

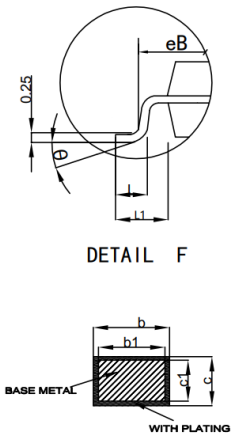
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	----	----	1.60
A1	0.05	----	0.15
A2	1.35	1.40	1.45
A3	0.60	----	0.64
b	0.16	----	0.24
c	0.13	----	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	----	8.25
e	0.40BSC		
L	0.40	----	0.65
L1	1.0REF		
θ	0°	----	8°

Figure 6-1 LQFP64-7x7mm package outline

6.2 LQFP48 package information

LQFP48 is a 48-pin, 7 x 7 mm low-profile quad flat package.





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	-----	-----	1.60
A1	0.05	-----	0.15
A2	1.35	1.40	1.45
A3	0.60	-----	0.64
b	0.18	-----	0.26
c	0.13	-----	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
eB	8.10	-----	8.25
e	0.50BSC		
L	0.40	-----	0.65
L1	1.0REF		
θ	0°	-----	8°

Figure 6-2 LQFP48-7x7mm package outline

7 Ordering information

Ordering information described as Figure 7-1.

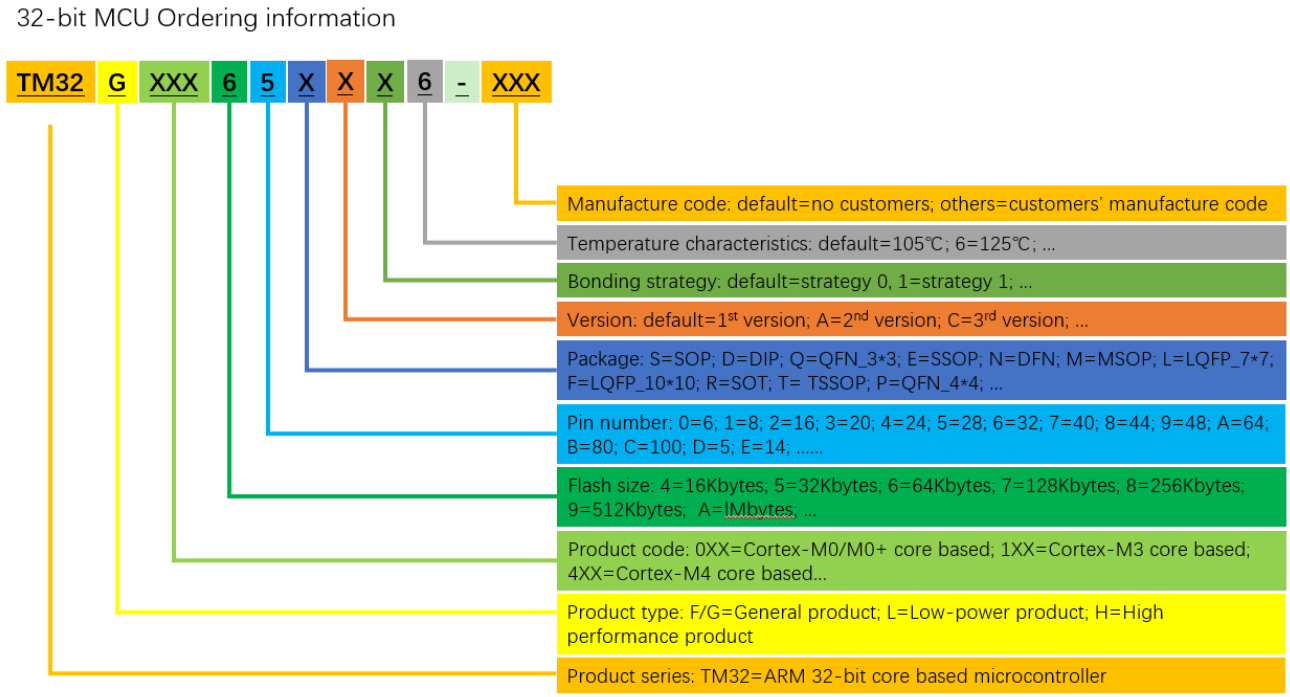


Figure 7-1 Ordering information