TM52E5223

DATA SHEET

Rev 0.91

(Please read the precautions on the second page before use)

PRECAUTIONS

1. Before entering the stop/pause mode, the system clock source must be switched to 16-division or slow clock if it is a fast clock**.**

ADMENDMENT HISTORY

Version	Date	Description
V0.90	Nov, 2024	New Release
V0.91	Jun, 2025	1. Modify DC Characteristics 2. Update SOP16 3. Remove I2C related description 4. Update Block Diagram Flash to MTP 5. Add enter Stop/Halt/Idle mode use guideline 6. Add enter Stop/Halt/Idle mode use description

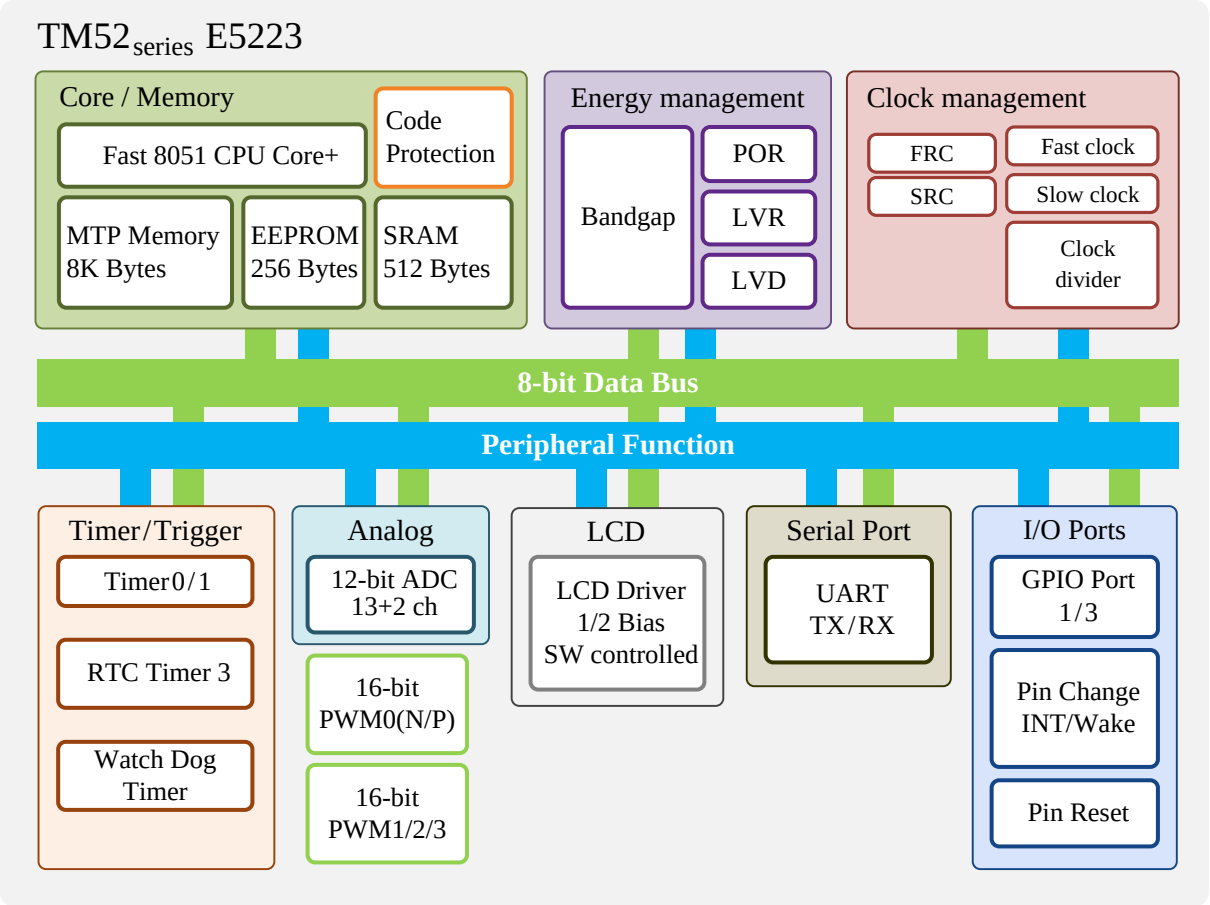
CONTENTS

GENERAL DESCRIPTION

The TM52 series E5223 is a new fast and low-voltage power-saving 8051 architecture, an 8-bit microcontroller that is fully compatible with the industry standard 8051 instruction set, and maintains the 8051 peripheral's functional block. Typically, the **TM52** executes instructions six times faster than the standard 8051 architecture.

The **TM52E5223** provides higher performance, lower cost, and can quickly enter the market by integrating multiple functions on the chip, including 8K bytes of MTP program memory, 512 bytes of SRAM, low voltage reset (LVR), and low voltage detection. (LVD), dual-clock power-saving operating mode, and timer Timer0/Timer1, real-time timer Timer3, 12-bit ADC, 16-bit pulse width modulator PWM0 (N/P), 16-bit pulse width modulator (PWM1/2 /3) and watchdog timer (WDT). Its high reliability and low power consumption make it widely applicable to consumer electronics products.。

BLOCK DIAGRAM



FEATURES

1. **Standard 8051 Instruction set, fast machine cycle**
   - Executes instructions six times faster than the standard 8051
2. **MTP Program Memory**
   - 8K Bytes
   - Code Protection Capability
   - 100 erase times at least
   - 10 years data retention at least
3. **256 Bytes EEPROM**
   - 30K erase times at least（2.5V<VCC<5.5V，-20℃~85℃）
   - 10 years data retention at least
4. **Total 512 Bytes SRAM (IRAM + XRAM)**
   - 256 Bytes IRAM in the 8051 internal data memory area
   - 256 Bytes XRAM in the 8051 external data memory area (accessed by MOVX Instruction)
5. **Two System Clock type selections**
   - Fast clock from Internal RC (FRC, 16.5888 MHz) (trim 7-bit) (5-bit fine-tuning)
   - Atomization frequency tracking fine-tuning 16.5888MHz±1KHz, 108KHz@0.5KHz fine-tuning
   - low clock from Internal RC (SRC, 131 KHz) (trim 5-bit) deviation ±2%
   - Slow clock timing uses SRC, 131 KHz/, 0~40 degree error (±1.5%)
   - System Clock can be divided by 1/2/4/16 option
6. **8051 Standard Timer – Timer0/1**
   - 16-bit Timer0, also supports T0O clock output for Buzzer application
   - 16-bit Timer1, supports T1O clock output for Buzzer application
7. **15-bit Timer3**
   - The clock source can be slow clock. (131K/4 = 32K), 0~40 degree deviation (±1.5%)
   - Interrupt period can be clock divided by 65536/32768/16384/8192/4096/2048/1024/512 option
8. **UART**
   - With UART pin selection option, baud rate clock can be set
9. **Two independent 16 bits PWMs with period-adjustment:**
   - 16-bit PWM0
     - ✧ **16-bit period/duty cycle setting**
     - ✧ PWM0(N/P) dead zone complementary, period center aligned (PPD) mode
     - ✧ Highest frequency FRC*2 or FRC or FRC/256 or SRC
   - 16-bit PWM1/2/3
     - ✧ 16-bit shared period, 16-bit independent duty cycle can be set
     - ✧ Highest frequency FRC*2 or FRC or FRC/256 or SRC

- 2 set output

10. LCD Driver

- All GPIOs can set the pull-up resistor and pull-down resistor 33KΩ@5V
- The pull-up resistor and pull-down resistor are turned on at the same time to 1/2 LCD bias voltage
- Software controlled SCOM0~13

11. 12-bit ADC with 12 channels external Pin input and 2 channels Internal Reference Voltage

- Built-in reference source output VCC or LDOV: 1.18V
- Internal Reference Voltage VBG 1.18V±1%@VCC=5V~3V, 25℃
- Internal Reference Voltage: 1/4$V_{CC,}$ V_{CC}/201

12. 11 Sources**, 4-level priority Interrupt**

- Timer0 /Timer1 /Timer3 Interrupt
- Port1/Port 3 Pin change Interrupt
- LVD Interrupt
- ADC Interrupt
- PWM0/1 Interrupt
- EEP write finish Interrupt
- UART Interrupt

13. Pin Interrupt can Wake up CPU from Halt/Stop mode

- Each pin can be defined as Wake up interrupt pin (by pin change)

14. Max. **14** Programmable **I/O** Pins

- CMOS output
- Pseudo-Open-Drain, or Open-Drain Output
- Schmitt Trigger Input
- Pin Pull-up / Pull-down can be Enabled or Disabled
- All pin with sink 40mA@VDD=5V， VOL=0.1VDD
- All pin with drive 12mA@VDD=5V， VOH=0.9VDD
- Schmitt Trigger Input VITH(0) : VIH 0.7VDD , VIL : 0.3VDD
- Schmitt Trigger Input VITH(1) : VIH 0.4VDD , VIL : 0.2VDD (not support in ICE emulation)

15. Independent RC Oscillating Watch Dog Timer

- 480ms/240ms/120ms/60ms selectable WDT timeout options

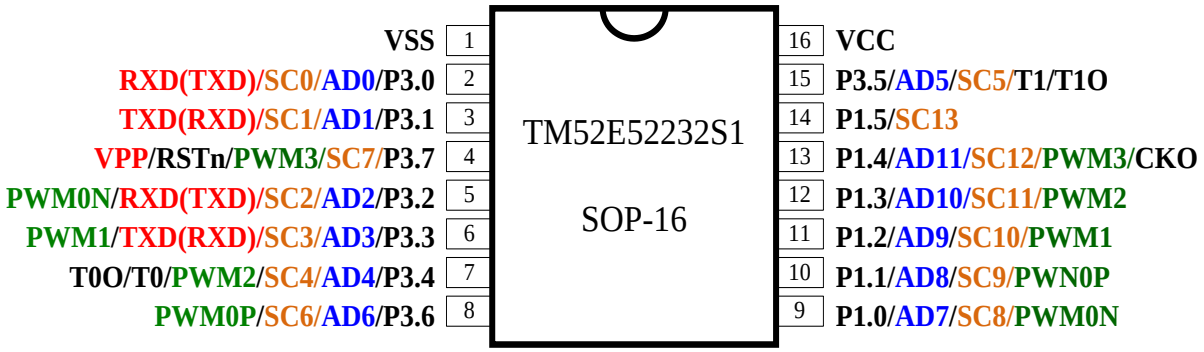
16. Five types Reset

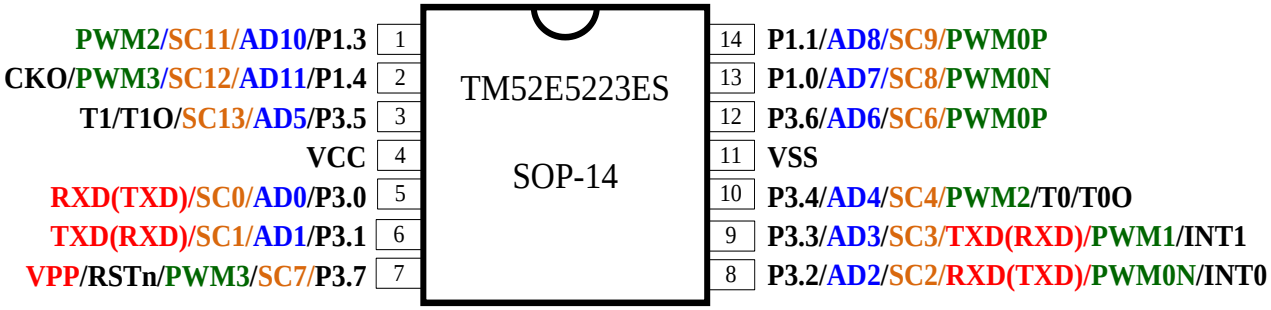
- Power on Reset
- Selectable External Pin Reset
- Selectable Watch Dog Reset
- Software Command Reset
- Selectable Low Voltage Reset

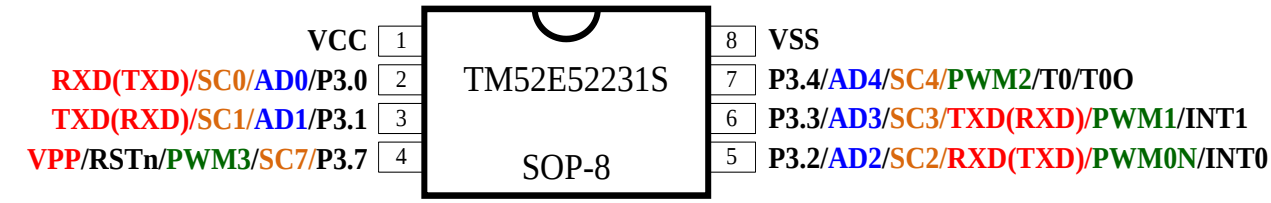
17. **16-level Low Voltage Reset (LVR)**
    - 1.6V ~3.5V
18. **15-level Low level Detect(LVD)**
    - 1.6V ~ 3.5V
19. **Five Power Operation Modes**
    - Fast/ Slow/ Idle/ Halt/ Stop mode
20. **Integrated 16-bit Cyclic Redundancy Check function**
21. **On-chip Debug/ICE interface**
    - Use P3.7(VPP)/P3.0/P3.1 pin
    - Share with ICP programming pin
22. **Operating Voltage and Current**
    - VCC =2.4V ~ 5.5V (@Fsys = FRC/1=16.5888MHz)
    - VCC =1.8V ~ 5.5V (@Fsys <= FRC/2= 8.2944MHz)
    - Normal mode 8.2944MHz, I_{CC} = 4mA@5V
    - Normal mode 16.5888MHz, I_{CC} = 6mA@5V
    - Stop mode I_{CC} =0.7μA@5V
    - I_{CC} = 4.3μA @Halt mode，PWRSAV=1，V_{CC}=3V
    - I_{CC} = 6μA @Idle mode，PWRSAV=1，V_{CC}=3V
    - Operating Temperature Range –40℃ ~ +105℃
23. **Package Types**
    - 16-pin SOP (150 mil)
    - 14-pin SOP (150 mil)
    - 8-pin SOP (150 mil)

PIN ASSIGNMENT

For low power applications, all digital I/Os (includingunbonding or unused) should avoid high-impedance settings.







PIN DESCRIPTION

Name	In/Out	Pin Description
P1.0~P1.5 P3.0~P3.7	I/O	Bit-programmable I/O port for Schmitt-trigger input, CMOS push-pull output or "open-drain" output. Pull-up and Pull-down resistors are assignable by software, so it can also be set to LCD 1/2 bias output. These pin's level change can interrupt/wake up CPU from Halt/Stop mode。
INT0, INT1	I	External low level or falling edge Interrupt input, Idle/Halt/Stop mode wake up input.
T0,T1	I	Timer0, Timer1 vent count pin input.
T0O	O	Timer0 overflow divided by 64 output
T1O	O	Timer1 overflow divided by 2 output
CKO	O	System clock divided by 2 output
RXD	I/O	UART transmit。
TXD	I/O	UART transmit。
PWM0N,PWM0P	O	16 位PWM complementary output
PWM1,2,3	O	16 位PWM output
SC0~SC13	O	The pull-up resistor and pull-down resistor are turned on at the same time as LCD COM 1/2 bias output
AD0~12	I	ADC input
RSTn / VPP	I/P	External active low reset input, Pull-up resistor is fixed enable/ External High Voltage
VCC,VSS	P	Power input pin and ground

PIN SUMMERY

TM52E5223

Pin number			Pin Name	Type	Initial State	Input				Output		Alternate			other
SOP-16	SOP-14	SOP-8				Pull-up	Pull_down	Wakeup	Ext. Interrupt	CMOS	Open-Drain	LCD	UART	PWM	
2	5	2	RXD(TXD)/SC0/AD0/P3.0	I/O	Hi-Z	●	●	●	●	●	●	●	●		
3	6	3	TXD(RXD)/SC1/AD1/P3.1	I/O	Hi-Z	●	●	●	●	●	●	●	●		
5	8	5	INT0/RXD(TXD)/PWM0N/SC2/AD2/P3.2	I/O	Hi-Z	●	●	●	●	●	●	●	●	●	VBGO
6	9	6	INT1/TXD(RXD)/PWM1/SC3/AD3/P3.3	I/O	Hi-Z	●	●	●	●	●	●	●	●	●	
7	10	7	T0/PWM2/SC4/AD4/P3.4	I/O	Hi-Z	●	●	●	●	●	●	●		●	T0O
15	3	–	T1/SC5/AD5/P3.5	I/O	Hi-Z	●	●	●	●	●	●	●			T1O
8	12	–	TXD2(RXD2)/PWM0P/SC6/AD6/P3.6	I/O	Hi-Z	●	●	●	●	●	●	●		●	
4	7	4	VPP/RSTn/PWM3/SC7/P3.7	I/O/P	Hi-Z	●	●	●	●	●	●	●		●	Reset VPP
9	13	–	PWM0N/SC8/AD7/P1.0	I/O	Hi-Z	●	●	●	●	●	●	●		●	
10	14	–	/PWM0P/SC9/AD8/P1.1	I/O	Hi-Z	●	●	●	●	●	●	●		●	
11	–	–	PWM1/SC10/AD9/P1.2	I/O	Hi-Z	●	●	●	●	●	●	●		●	
12	1	–	PWM2/SC11/AD10/P1.3	I/O	Hi-Z	●	●	●	●	●	●	●		●	
13	2	–	CKO/PWM3/SC12/AD11/P1.4	I/O	Hi-Z	●	●	●	●	●	●	●		●	
14	–	–	SC13/P1.5	I/O	Hi-Z	●	●	●	●	●	●	●			
1	11	8	VSS	P											
16	4	1	VCC	P											

FUNCTIONAL DESCRIPTION

1. CPU Core

In the 8051 architecture, the C programming language is used as a development platform. The TM52 device features a fast 8051 core in a highly integrated microcontroller, allowing designers to be able to achieve improved performance compared to a classic 8051 device. TM52 series microcontrollers provide a complete binary code with standard 8051 instruction set compatibility, ensuring an easy migration path to accelerate the development speed of system products. The CPU core includes an ALU, a program status word (PSW), an accumulator (ACC), a B register, a stack point (SP), DPTRs, a program counter, an instruction decoder, and core special function registers (SFRs).

1.1 Accumulator (ACC)

This register provides one of the operands for most ALU operations. Accumulators are generally referred to as A or Acc and sometimes referred to as Register A. In this document, the accumulator is represented as "A" or "ACC" including the instruction table. The accumulator, as its name suggests, is used as a general register to accumulate the intermediate results of a large number of instructions. The accumulator is the most important and frequently used register to complete arithmetic and logical operations. It holds the intermediate results of most arithmetic and logic operations and assists in data transportation.

SFR **E0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ACC	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

E0h.7~0 **ACC:** Accumulator

1.2 B Register (B)

The "B" register is very similar to the ACC and may hold a 1 Byte value. This register provides the second operand for multiply or divide instructions. Otherwise, it may be used as a scratch pad register. The B register is only used by two 8051 instructions, MUL and DIV. When A is to be multiplied or divided by another number, the other number is stored in B. For MUL and DIV instructions, it is necessary that the two operands are in A and B

ex: DIV AB

When this instruction is executed, data inside A and B are divided, and the answer is stored in A

SFR **F0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
B	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0h.7~0 **B:** Bregister

1.3 Stack Pointer (SP)

The SP register contains the Stack Pointer. The Stack Pointer is used to load the program counter into memory during LCALL and ACALL instructions and is used to retrieve the program counter from memory in RET and RETI instructions. The stack may also be saved or loaded using PUSH and POP instructions, which also increment and decrement the Stack Pointer.

SFR **81h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SP	SP							
R/W	R/W							
Reset	0	0	0	0	0	1	1	1

81h.7~0 **SP:** Stack Point

1.4 Dual Data Pointer(DPTRs)

TM52 device has two DPTRs, which share the same SFR address. Each DPTR is 16 bits in size and consists of two registers: the DPTR high byte (DPH) and the DPTR low byte (DPL). The DPTR is used for 16-bit-address external memory accesses, for offset code byte fetches, and for offset program jumps. Setting the DPSEL control bit allows the program code to switch between the two physical DPTRs

SFR **82h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

82h.7~0 **DPL:** Data Point low byte

SFR **83h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	DPH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

83h.7~0 **DPH:** Data Point high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	–	ADSOC	LVRPD	–	T1SEL	DPSEL
R/W	R/W	R/W	–	R/W	R/W	–	R/W	R/W
Reset	0	0	–	0	0	–	0	0

F8h.0 **DPSEL:** Active DPTR Select

1.5 Program Status Word (PSW)

This register contains status information resulting from CPU and ALU operations. The instructions that affect the PSW are listed below

Instruction	Flag		
	C	OV	AC
ADD	X	X	X
ADDC	X	X	X
SUBB	X	X	X
MUL	0	X	
DIV	0	X	
DA	X		
RRC	X		
RLC	X		
SETB C	1		

Instruction	Flag		
	C	OV	AC
CLR C	0		
CPL C	X		
ANL C, bit	X		
ANL C, /bit	X		
ORL C, bit	X		
ORL C, /bit	X		
MOV C, bit	X		
CJNE	X		

A “0” means the flag is always cleared, a “1” means the flag is always set and an “X” means that the state of the flag depends on the result of the operation.

SFR **D0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

D0h.7 **CY:** ALU carry flag

D0h.6 **AC:** ALU auxiliary carry flag

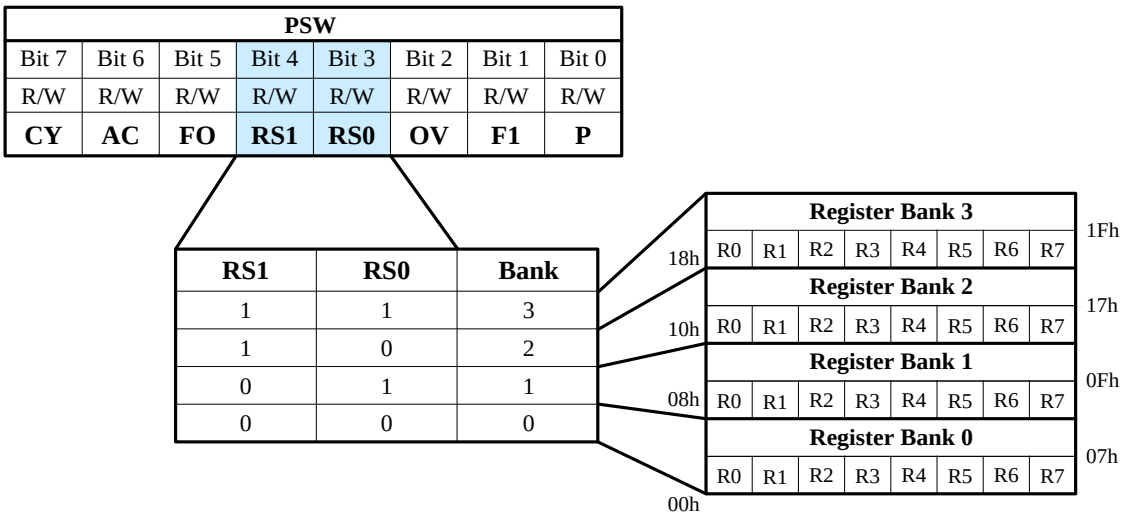
D0h.5 **F0:** General purpose user-definable flag

D0h.4~3 **RS1, RS0:** The contents of (RS1, RS0) enable the working register banks as:
- 00: Bank 0 (00h~07h)
- 01: Bank 1 (08h~0Fh)
- 10: Bank 2 (10h~17h)
- 11: Bank 3 (18h~1Fh)

D0h.2 **OV:** ALU overflow flag

D0h.1 **F1:** General purpose user-definable flag

D0h.0 **P:** Parity flag. Set/cleared by hardware each instruction cycle to indicate odd/even number of “one” bits in the accumulator.



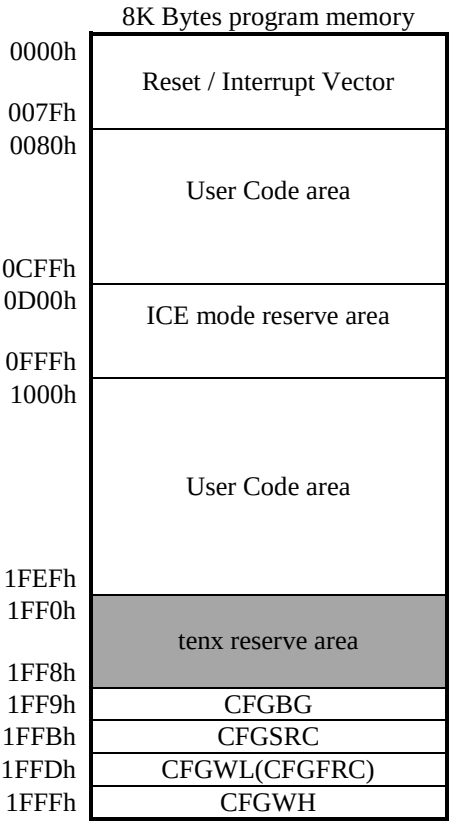
2. Memory

2.1 Program Memory

TM52E5223 has 8K bytes of flash program memory and supports in-circuit programming (ICP) functional mode. This flash memory can be erased and written repeatedly at least 100 times. The continuous address space (0000h~1FFFh) of the flash program memory is divided into multiple sectors for device operation.

2.1.1 Program Memory Functional Partition

The last 16 bytes (1FF0h~1FFFh) of program memory is defined as the chip Configuration Word (CFGW). During power-on reset (POR), the last 8 bytes (1FF8h~1FFFh) will be loaded into the device control register. The 0000h~007Fh is defined as reset/interrupt vector by standard 8051. In online emulation (ICE) mode, users also need to reserve the address space of 0D00h~0FFFh for ICE system communication.



TM52E5223

SFR **DFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDCTL	–	–	–	–	–	ATDEN	ATDT	
R/W	–	–	–	–	–	R/W	R/W	
Reset	–	–	–	–	–	1	0	1

DFh.2 **ATDEN:** Read signal delay control for PROGRAM ROM
0: Disable(Read always=1); for EFT consideration , must disable ATDEN (ATDEN=0)
1: Enable (when the system clock use SRC, setting this register can reduce power consumption)

DFh.1~0 **ATDT:** Read signal delay time control of program ROM (ATD timing controlwhen ATDEN=1)
00: Program ROM read signal delay 6.8ns@5V or 10.7ns@3V
01: Program ROM read signal delay 12.2ns@5V or 19.4ns@3V (recommended setting value)
10: Program ROM read signal delay 17.6ns@5V or 28ns@3V
11: Program ROM read signal delay 23ns@5V or 37ns@3V

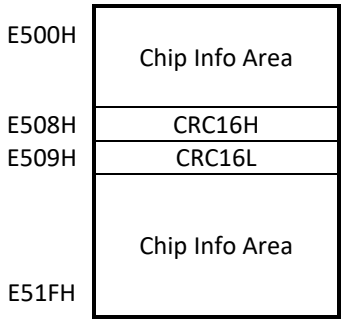
2.1.2 FLASH ICP Mode

Flash memory can be programmed via tenx's proprietary writer (HTLINK), which requires at least five wires (VCC, VSS, VPP, P3.0, and P3.1 pins) connected to the chip. If the user wants to program the flash memory on the target circuit board (In-Circuit Programming, ICP), these pins must be left free enough to connect to the writer, preferably not to the circuit; if you want to connect the circuit, please refer to the related AP information。

Writer wire number	Pin connection
5-Wire	VCC, VSS, P3.0, P3.1, P3.7(VPP)

2.2 Information Memory

The Chip has a 32-word information memory. The information memory address contiguous space (E500h~E51Fh) is divided into multiple sectors for device operations. The chip information area is a reserved area that defines production information, such as ID, special regulations, encoding number, and verification. CRC16H/L is the reserved area of the checksum. Tenx can provide a CRC verification subroutine. The user can calculate the checksum by the CRC verification subroutine to compare with CRC16H/L and check the validity of the ROM code



Info ROM

2.3 EEPROM Memory

TM52E5223 contains 256 bytes of data EEPROM memory. It is organized as a separate data space, in which single bytes can be read and written. The EEPROM has an endurance of at least 30K write/erase cycles (2.5V < VCC < 5.5V, -20℃~85℃).

	EEPROM Memory
EE00h	EEPROM[0]
EE01h	EEPROM[1]
EE02h	. . .
EEFEh	EEPROM[254]
EEFFh	EEPROM[255]

2.3.1 The Precaution of EEPROM Programming

2.3.1.1 The Programming Characteristics of EEPROM

(1) The EEPROM programming time is not fixed. Programming different data requires different times

(2) The programming time is affected by voltage, temperature, and whether the data is inverted. The programming time is longer for higher temperatures, lower VCC and larger number of data inversion.

(3) This chip has a built-in EEPROM write time-out function to ensure that the system can execute the program normally when write time-out occurred.

2.3.1.2 EEPROM Write Endurance

The number of times of EEPROM programming is related to voltage and temperature. The write endurance is at least 30,000(2.5V < VCC < 5.5V, -20℃~85℃). Please refer to the table of "EEPROM Characteristics" in the chapter of "ELECTRICAL CHARACTERISTICS"

2.3.1.3 EEPROM Write Validation

Depending on the specific application, it is generally required to read back the data written into EEPROM for verification

2.3.1.4 Protection against Miswriting

When a write operation is initiated, the following operations can prevent miswriting:

(1) Low voltage detection: when writing EEPROM, VCC must be >3.0V@16.5888MHz, you can use the LVD function to monitor the voltage. (LVD monitoring voltage is recommended to be 3.5V to prevent power outage and allow sufficient time for writing EEPROM)

(2) Clear the watchdog (WDT) every time a byte is written to prevent the watchdog from being reset when multiple bytes are written sequentially.

(3) When writing data, temporarily turn off all of the interrupt and resume them after the completion of writing.

(4) Software failure: add EEPROM read-back mechanism to the program to ensure that data is written correctly.

(5) Timeout protection: enable the write timeout function (EEPTE) in the program to protect the system from getting stuck when write time-out occurred.

(6) To reduce power supply glitches: connect capacitors between VCC and GND to stabilize the system power supply.

(7) Must confirm EEPBUSY=0 before writing the next byte.

The EEPROM Write: is simply achieved by a "MOVX @DPTR, A" instruction while the DPTR contains the target EEPROM address (EE00h~EEFFh), and the ACC contains the data being written. EEPROM writing requires approximately 6 ms @V_{CC}=2.7V, 1.2 ms @V_{CC}=5V. Meanwhile, the CPU and all peripheral modules (Timers and others) continue running during the writing time。

After the writing is completed, the interrupt flag EEPIF will be generated. The software can use this interrupt or poll EEPBUSY to know whether the EEPROM writing is completed. EEPIF is automatically cleared when the program executes the interrupt service routine. At the same time, TM52E5223 has a built-in EEPROM dedicated watchdog timer (non-MCU WDT) to get out of the stuck state when writing fails. EEPROM data writing requires VCC > 3.0V and WDT is turned off to avoid accidental writing

The EEPROM Read can be performed by the "MOVX A, @DPTR" instruction as long as the target address points to the EE00h~EEFEh area. The EEPROM read does require approximately 300ns

```
; EEPROM example code
; 3.0V < VCC < 5.5V
ANL     AUX2, #3Fh          ; WDT function disable
ORL     AUX2, #04h          ; EEPROM Time-Out function enable
MOV     DPTR, #0EE00h       ; DPTR=EE00h=target EEPROM[0] address
MOV     A, #0A5h            ; A=A5h=target EEPROM[0] write data
MOV     EEPCON, #0E2h       ; EEPROM write enable
MOVX    @DPTR, A            ; EEPROM[0]=A5h, after EEPROM write
                            ; 1ms~6ms H/W writing time, CPU does not need wait
MOV     A, INTFLG           ; Need to wait for EEP F=1 or EEP BUSY=0 ,
JB      ACC.5, $-2          ; before setting EEPCON =00h

MOV     EEPCON, #000h       ; EEPROM write disable, after EEPROM write finish
CLR     A                   ; A=0
MOVX    A, @DPTR            ; A=A5h
```

Note: Writing and reading EEPROM can only be used outside or inside the interrupt. If the writing and reading EEPROM functions are used both inside and outside the interrupt, it may cause errors.

SFR **C9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EEPCON	EEPCON							
			EEPWE		EEPTO	–		
R/W			R		R	W		
Reset			0		0	–		

C9h.7~0 **EEPCON(W):**

Write E2h to set EEPWE flag; Write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write。

C9h.5 **EEPWE(R):** Flag indicates EEPROM can be written by IAP or not, 1=Write EEPROM enable.

C9h.3 **EEPTO (R):** EEPROM write Time-Out flag, Set by H/W when EEPROM write Time-out occurs. Cleared by H/W when EEPWE=0

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT		EEPTE		
R/W	R/W	R/W	R/W	R/W		R/W		
Reset	0	0	0	0		1	1	

F7h.7~6 **WDTE:** Watchdog Timer Reset control

0x: Watchdog Timer Reset disable

10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Halt/Stop mode

11: Watchdog Timer Reset always enable

F7h.2~1 **EEPTE:** EEPROM write watchdog timer enable

00: Disable

01: wait 6.9 ms trigger watchdog time-out flag, and escape the write fail state

10: wait 27 ms trigger watchdog time-out flag, and escape the write fail state

11: wait 55 ms trigger watchdog time-out flag, and escape the write fail state

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	EEPIF	EEPBUSY	ADIF	-	-	PCIF	TF3
R/W	R/W	R/W	R	R/W	-	-	R/W	R/W
Reset	0	0	0	0	-	-	0	0

95h.6 **EEPIF:** EEP write finish Interrupt

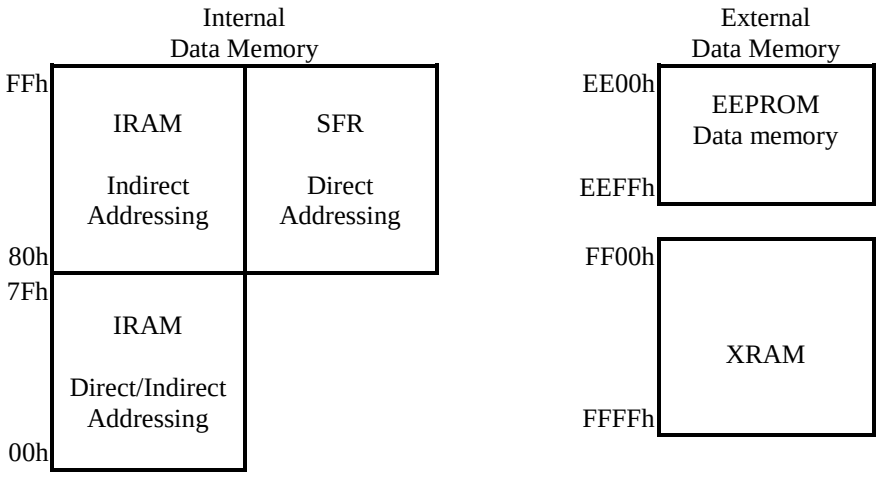
Set by H/W. S/W writes BFh to INTFLG to clear this flag.

95h.5 **EEPBUSY:** EEP Busy Flag

EEP Busy Flag is set high when write EEP

2.4 Data Memory

As the standard 8051, the Chip has both Internal and External Data Memory space. The Internal Data Memory space consists of 256 Bytes IRAM and SFRs, which are accessible through a rich instruction set. The External Data Memory space consists of 256 Bytes XRAM and 256 Bytes EEPROM, which can be only accessed by MOVX instruction.。



2.4.1 IRAM

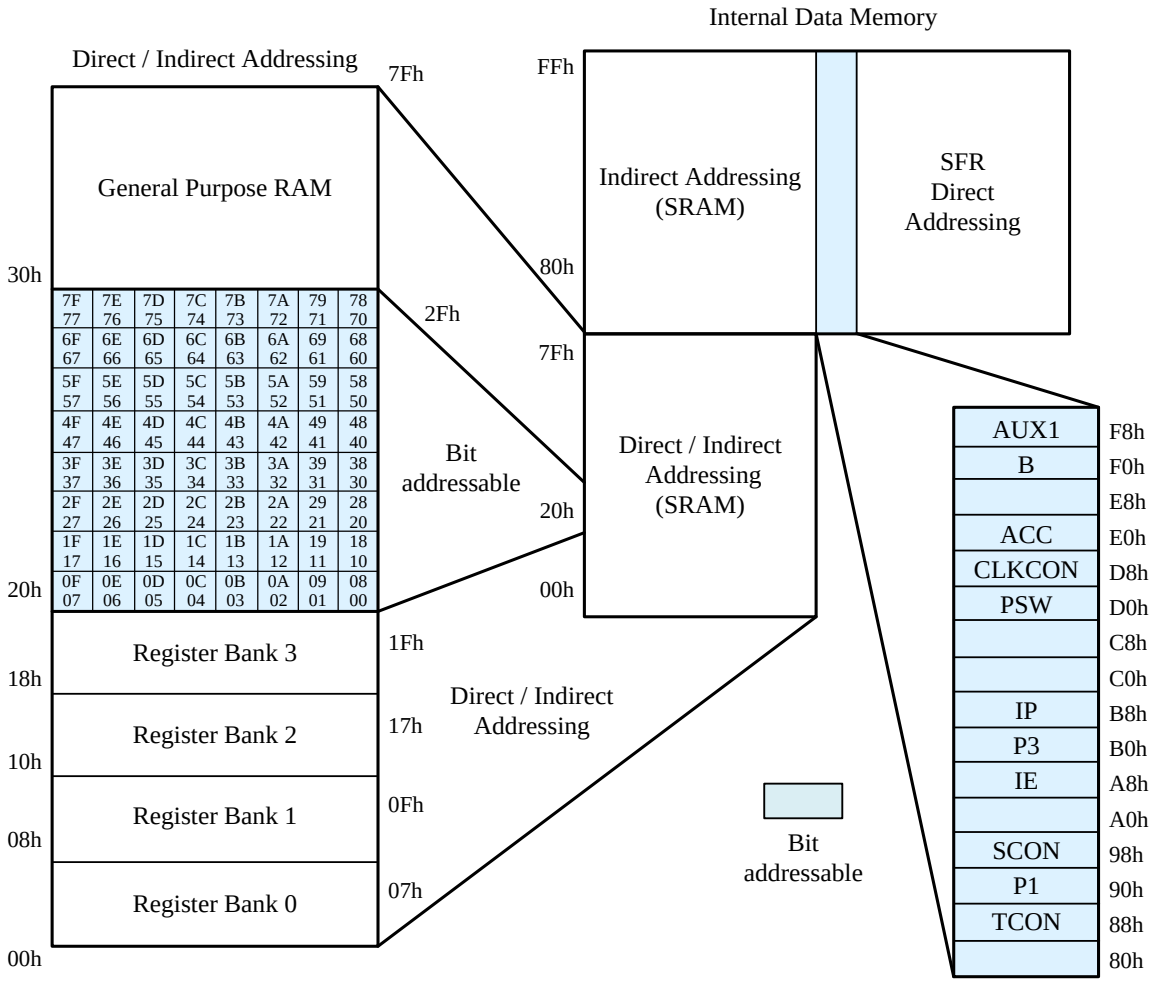
IRAM is located in the 8051 internal data memory space. The whole 256 Bytes IRAM are accessible using indirect addressing but only the lower 128 Bytes are accessible using direct addressing. There are four directly addressable register banks (switching by PSW), which occupy IRAM space from 00h to 1Fh. The address 20h to 2Fh 16 Bytes IRAM space is bit-addressable. IRAM can be used as scratch pad registers or program stack.

2.4.2 XRAM

XRAM is located in the 8051 external data memory space (address from FF00h to FFFFh). The 256 Bytes XRAM can be only accessed by “MOVX” instruction.

2.4.3 SFRs

All peripheral functional modules such as I/O ports, Timers and UART operations for the chip are accessed via Special Function Registers (SFRs). These registers occupy upper 128 Bytes of direct Data Memory space locations in the range 80h to FFh. There are 14 bit-addressable SFRs (which means that eight individual bits inside a single byte are addressable), such as ACC, B register, PSW, TCON, SCON, and others. The remaining SFRs are only byte addressable. SFRs provide control and data exchange with the resources and peripherals of the Chip. The TM52 series of microcontrollers provides complete binary code with standard 8051 instruction set compatibility. Beside the standard 8051 SFRs, the Chip implements additional SFRs used to configure and access subsystems such as the ADC/LCD, which are unique to the Chip.



	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
F8h	AUX1							
F0h	B	CRCDL	CRCDH	CRCIN		CFGBG	CFGWL	AUX2
E8h			CFGSRC					AUX3
E0h	ACC			LVRCON		EFTCON		
D8h	CLKCON	PWM0PRDH	PWM0PRDL	PWM1PRDH	PWM1PRDL	PWM3DH	PWM3DL	RDCTL
D0h	PSW	PWM0DH	PWM0DL	PWM1DH	PWM1DL	PWM2DH	PWM2DL	FRCFT
C8h	T2CON	EEPCON						
C0h								
B8h	IP	IPH	IP1	IP1H				LVDS
B0h	P3						ADCHSEL	
A8h	IE	INTE	ADCDL	ADCDH	ADCDLYT			
A0h	P2	PWMCON						PWMCON2
98h	SCON	SBUF	P1MOD54	P3MOD10	P3MOD32	P3MOD54	P3MOD76	UARTBRP
90h	P1	P1MOD10	P1MOD32	UARTCON	OPTION	INTFLG		SWCMD
88h	TCON	TMOD	TL0	TL1	TH0	TH1		
80h	P0	SP	DPL	DPH	INTE2		INTPWM	PCON

3. LVR and LVD setting

The chip provides low voltage reset (LVR) and low voltage detection (LVD) functions. CFGWH can select 16-level LVD. CFGWH will be loaded into the device control register LVDSEL (SFR BFh.3~0) during power-on reset. LVRSEL(SFR E3h.3~0) can select 16 levels of LVR. The SFR PWRSAV and LVRPD bits will also affect the LVR function, as shown in the following table. After the program STARTUP, the first instruction in main requires a new LVR setting.

Operation Mode	SFR			LVR	Function	Note
	LVRPD	PWRSAV	LVRESEL			
Fast Slow	0	X	0000	ON	LV Reset 1.62V	
	0	X	0001	ON	LV Reset 1.69V	
	0	X	0010	ON	LV Reset 1.82V	
	0	X	0011	ON	LV Reset 1.94V	
	0	X	0100	ON	LV Reset 2.06V	
	0	X	0101	ON	LV Reset 2.17V	
	0	X	0110	ON	LV Reset 2.29V	
	0	X	0111	ON	LV Reset 2.41V	
	0	X	1000	ON	LV Reset 2.54V	
	0	X	1001	ON	LV Reset 2.66V	
	0	X	1010	ON	LV Reset 2.78V	
	0	X	1011	ON	LV Reset 2.90V	
	0	X	1100	ON	LV Reset 3.03V	
	0	X	1101	ON	LV Reset 3.15V	
	0	X	1110	ON	LV Reset 3.27V	
	0	X	1111	ON	LV Reset 3.39V	
Idle Stop Halt	0	0	0000	ON	LV Reset 1.62V	Current consumption about 70uA
	0	0	0001	ON	LV Reset 1.71V	
	0	0	0010	ON	LV Reset 1.83V	
	0	0	0011	ON	LV Reset 1.95V	
	0	0	0100	ON	LV Reset 2.07V	
	0	0	0101	ON	LV Reset 2.19V	
	0	0	0110	ON	LV Reset 2.31V	
	0	0	0111	ON	LV Reset 2.43V	
	0	0	1000	ON	LV Reset 2.56V	
	0	0	1001	ON	LV Reset 2.68V	
	0	0	1010	ON	LV Reset 2.81V	
	0	0	1011	ON	LV Reset 2.93V	
	0	0	1100	ON	LV Reset 3.05V	
	0	0	1101	ON	LV Reset 3.17V	
	0	0	1110	ON	LV Reset 3.30V	
	0	0	1111	ON	LV Reset 3.42V	
Idle	0	1	XXXX	ON	Disable LVR Enable POR 1.6V	Current consumption about 16uA
Stop Halt	0	1	XXXX	OFF	Disable	* Minimum Current consumption 0.7uA
Fast Slow Idle	1	X	XXXX	ON	Disable LVR Enable POR 1.6V	Current consumption about 16uA
Stop Halt	1	X	XXXX	OFF	Disable	* Minimum Current consumption 0.7uA

Note: *The current consumption of Halt mode is more than Stop mode about 5.5~23uA, because SRC is enabled*

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT		EEPTE		
R/W	R/W	R/W	R/W	R/W		R/W	R/W	
Reset	0	0	0	0		0	0	

F7h.5 **PWRSAV**：chip power-saving option

Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRCON	–			LVRPD	LVRSEL			
R/W	–			R/W	R/W	R/W	R/W	R/W
Reset	–			0	0	0	0	0

E3h.3~0 **LVRSEL**：Low voltage Reset sleect

0000: set LVR at 1.62V
0001: set LVR at 1.69V
0010: set LVR at 1.82V
0011: set LVR at 1.94V
0100: set LVR at 2.06V
0101: set LVR at 2.17V
0110: set LVR at 2.29V
0111: set LVR at 2.41V
1000: set LVR at 2.54V
1001: set LVR at 2.66V
1010: set LVR at 2.78V
1011: set LVR at 2.90V
1100: set LVR at 3.03V
1101: set LVR at 3.15V
1110: set LVR at 3.27V
1111: set LVR at 3.39V

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDS	LVDM	LVDO	LVDHYS	LVDPD	LVDSESL			
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0			

BFh.7 **LVDM:**
0: VCC< VLVD(LVDIF=1 while LVDO=1)
1: VCC> VLVD(LVDIF=1 while LVDO=0)

BFh.6 **LVDO:** Low Voltage Detect output

BFh.5 **LVDHYS:** LVD Hysteresis Enable.
0: LVD Hysteresis disable
1: LVD Hysteresis enable

BFh.4 **LVDPD:** Low Voltage Detect function select (Auto disable in Idle/Halt/Stop mode)
0: LVD enable
1: LVD disable

BFh.3~0 **LVDSEL:** Low voltage detect (LVD) select
0000: set LVD at 1.62V
0001: set LVD at 1.71V
0010: set LVD at 1.83V
0011: set LVD at 1.95V
0100: set LVD at 2.07V
0101: set LVD at 2.19V
0110: set LVD at 2.31V
0111: set LVD at 2.43V
1000: set LVD at 2.56V
1001: set LVD at 2.68V
1010: set LVD at 2.81V
1011: set LVD at 2.93V
1100: set LVD at 3.05V
1101: set LVD at 3.17V
1110: set LVD at 3.30V
1111: set LVD at 3.42V

4. Reset

The Chip has five types of reset methods. Resets can be caused by Power on Reset (POR), External Pin Reset (XRST), Software Command Reset (SWRST), Watchdog Timer Reset (WDTR), or Low Voltage Reset (LVR). The CFGWH controls the Reset functionality. The SFRs are returned to their default value after Reset.

4.1 Power on Reset

After Power on Reset, the device stays on Reset state for 40 ms as chip warm up time, then downloads the CFGW register from ROM's last six bytes. The Power on Reset needs VCC pin's voltage first discharge to near V_{SS} level, then rise beyond 2.2V. Power On Reset is always Enable.

4.2 External Pin Reset

External Pin Reset is active low. It needs to keep at least 2 SRC clock cycle long to be seen by the Chip. External Pin Reset can be disabled or enabled by CFGW.

4.3 Software Command Reset

Software Reset is activated by writing the SFR 97h with data 56h.

4.4 Watchdog Timer Reset

WDT overflow Reset is disabled or enabled by SFR F7h. The WDT uses SRC as its counting time base. It runs in Fast/Slow mode and runs or stops in Idle/Halt/Stop mode. WDT overflow speed can be defined by WDTPSC SFR. WDT is cleared by device Reset or CLRWDT SFR bit.

4.5 Low Voltage Reset

The Chip provides LVR and Low Voltage Detection (LVD) functions. There are 16-level LVR can be selected by LVRCON (E3h.3~0) and 16-level LVD can be selected by SFR LVDS (B3h.3~0). When PWRSAV (SFR F7h.5) = 1, LVR will be disabled when enter IDLE/HALT/STOP mode. After power-on, the LVR defaults to the lowest 1.62V. Before switching to the fast clock, the appropriate LVR voltage point corresponding to the frequency should be selected.

SFR **E3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVRCON	–			LVRPD	LVRSEL			
R/W	–			R/W	R/W	R/W	R/W	R/W
Reset	–			0	0	0	0	0

E3h.3~0 **LVRSEL:** Low voltage Reset sleect

0000: set LVR at 1.62V
0001: set LVR at 1.69V
0010: set LVR at 1.82V
0011: set LVR at 1.94V
0100: set LVR at 2.06V
0101: set LVR at 2.17V
0110: set LVR at 2.29V
0111: set LVR at 2.41V
1000: set LVR at 2.54V
1001: set LVR at 2.66V
1010: set LVR at 2.78V
1011: set LVR at 2.90V
1100: set LVR at 3.03V
1101: set LVR at 3.15V
1110: set LVR at 3.27V
1111: set LVR at 3.39V

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	–	TM3CKS	WDTPSC		ADCKS		-	–
R/W	–	R/W	R/W		R/W		-	-
Reset	–	0	0	0	0	0	-	-

94h.5~4 **WDTPSC:** Watchdog Timer pre-scalar time select
00: 480 ms WDT overflow rate
01: 240 ms WDT overflow rate
10: 120 ms WDT overflow rate
11: 60 ms WDT overflow rate

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	EEPIF	EEPBUSY	ADIF	–	–	PCIF	TF3
R/W	R/W	R/W	R	R/W	–	–	R/W	R/W
Reset	0	0	0	0	–	–	0	0

95h.7 **LVDIF:** Low Voltage Detect interrupt flag
Set by H/W. S/W writes 7Fh to INTFLG to clear this flag.

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **97h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWCMD	SWRST							
R/W	W						R/W	W
Reset	–						–	0

97h.7~0 **SWRST:** Write 56h to generate S/W Reset

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT	-	EEPTE		-
R/W	R/W	R/W	R/W	R/W	-	R/W		-
Reset	0	0	0	0	-	1	1	-

F7h.7~6 **WDTE:** Watchdog Timer Reset control
0x: Watchdog Timer Reset disable
10: Watchdog Timer Reset enable in Fast/Slow mode, disable in Idle/Halt/Stop mode
11: Watchdog Timer Reset always enable

F7h.5 **PWRSAV:** chip power-saving option
Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	CLRPWM0	ADSOC	CLRPWM1	T0SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	1	0	0	0

F8h.7 **CLRWDT:** Set to clear WDT, H/W auto clear it at next clock cycle.

5. Clock Circuitry & Operation Mode

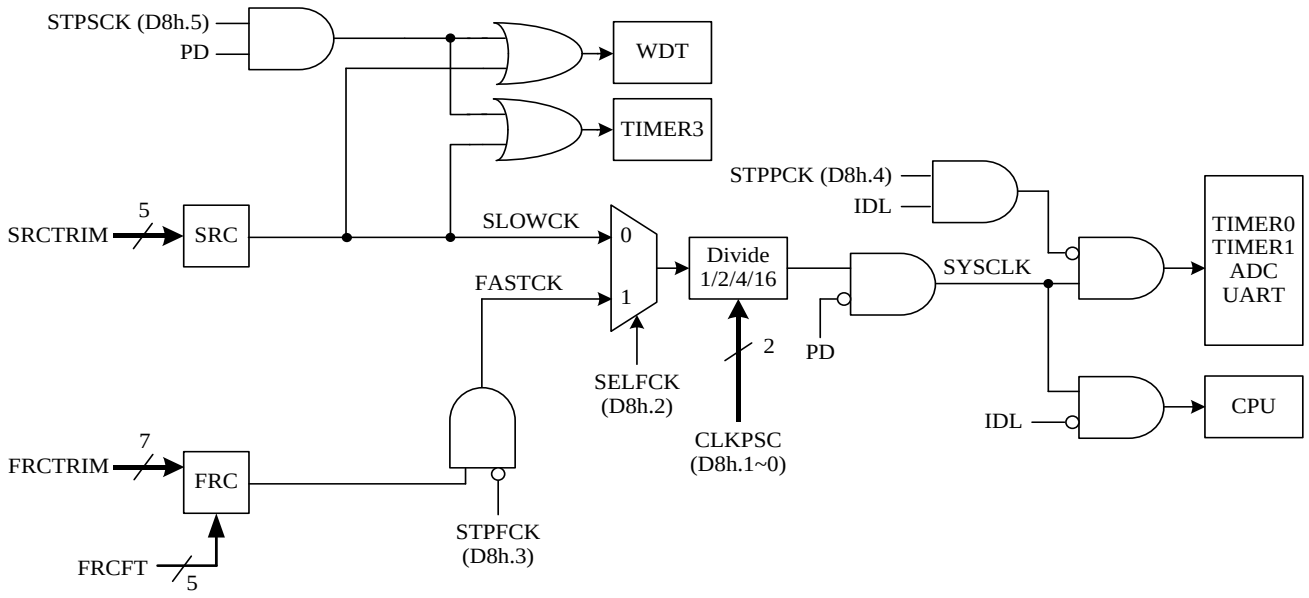
5.1 System Clock

The chip is designed with a dual clock system. At runtime, the user can directly switch from fast clock to slow clock or from slow to fast. It has a choice of clock dividers by 1, 2, 4 or 16. Fast clock uses FRC (fast internal RC, 16.5888 MHz). The slow clock uses SRC (slow internal RC, 131 KHz). Fast clock mode and slow clock mode are defined as fast/slow clock CPU operating speeds. The fast clock FRC is calibrated to the preset value (16.5888MHz) before leaving the factory. This default value will be loaded into the register SFR F6h when power is turned on. In addition, the fast clock FRC can also be used to make fine adjustments using the register FRCFT (SFR. D7h). . The slow clock SRC is also calibrated to the preset value (131KHz) before leaving the factory, and is loaded into the register SFR EAh when powered on.。

After Reset, the device is running at Slow mode with 131 KHz SRC. S/W should select the proper clock rate for chip operation safety. The higher V_{CC} allows the chip to run at a higher System clock frequency.

The **CLKCON** SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow clock type in Fast mode and change the Fast clock type in Slow mode. Never to write both STPFCK=1 & SELFCK=1. It is recommended to write this SFR bit by bit.

The chip can also output the "system clock divided by 2" signal (CKO) to the P1.4 pin. The output setting of the CKO pin is controlled by the P1MOD54 SFR (see Section 7)



注: Because of the CLKPSC delay, it needs to wait for 16 clock cycles (max.) before switching Slow clock to Fast clock.

SYSCLK	CLKCON (D8h)	
	bit3 STPFCK	bit2 SELFCK
Fast FRC	0	1
Slow SRC	0/1	0
Stop FRC	0 → 1	0
Switch to FRC	0	0 → 1
Switch to SRC	0	1 → 0

Flash	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGWL		FRCTRIM						

CFGWL **FRCTRIM:** FRC frequency adjustment
FRC is trimmed to 16.5888MHz in chip manufacturing. FRCF records the adjustment data. After Power on, CFGWL will be uploaded to SFR F6h

SFR **F6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRCF	–	FRCF						
R/W	–	R/W						
Reset	–	–	–	–	–	–	–	–

F6h.6~0 **FRCF:** FRC frequency adjustment
00h= lowest frequency，7Fh= highest frequency

SFR **D7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRCFT	–	–	–	FRCFT				
R/W	–	–	–	R/W				
Reset	–	–	–	0	0	0	0	0

D7h.4~0 **FRCFT:** FRC frequency fine-tune

Flash	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CFGSRC				SRCTRIM				

CFGSRC **SRCTRIM:** SRC frequency adjustment
SRC is trimmed to 131KHz. SRCTRIM records the adjustment data. After Power on, CFGSRC will be uploaded to SFR EAh

SFR **EAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SRCTRIM	–	–	–	SRCTRIM				
R/W	–	–	–	R/W				
Reset	–	–	–	–	–	–	–	–

EAh.4~0 **SRCTRIM:** SRC frequency adjustment
00h= lowest frequency，1Fh= highest frequency

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON			STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W			R/W	R/W	R/W	R/W	R/W	
Reset			1	0	0	0	1	1

D8h.5 **STPSCK:** Set 1 to stop Slow clock in PDOWN mode.

D8h.4 **STPPCK:** Set 1 to stop UARTs/Timer0/Timer1/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.

D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.

D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock

D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

5.2 Operation Modes

There are five operation modes for this device. **Fast Mode** is defined as the CPU running at Fast clock speed. **Slow Mode** is defined as the CPU running at Slow clock speed. When the System clock speed is lower, the power consumption is lower.

Idle Mode is entered by setting the IDL bit in PCON SFR. Both Fast and Slow clock can be set as the System clock source in Idle Mode, but Slow clock is better for power saving. In Idle mode, the CPU puts itself to sleep while the on-chip peripherals stay active. The "STPPCK" bit in CLKCON SFR can be set to furthermore reduce Idle mode current. If STPPCK is set, only Timer3 and pin interrupts are alive in Idle Mode, others peripherals such as Timer0/1/2, UARTs and ADC are stop. The slower System clock rate also helps current saving. It can be achieved by setup the CLKPSC SFR to divide System clock frequency. Idle mode is terminated by Reset or enabled Interrupts wake up.

Stop Mode is entered by setting the PD bit in PCON SFR and STPSCK is set. This mode is the so-called "Power Down" mode in standard 8051. In Stop mode, all clocks stop except the WDT could be alive if it is enabled. Stop Mode is terminated by Reset or pin wake up.

Halt Mode is entered by setting the PD bit in PCON SFR and STPSCK is cleared. In Halt mode, all clocks stop except the Timer3 and WDT could be alive if they are enabled. Halt Mode is terminated by Reset, pin wake up or Timer3 interrupt. In this mode, Timer3 clock source can only choose Slow clock, not FRC/512.

Before entering the stop/pause mode, the system clock source must be switched to 16-division or slow clock if it is a fast clock**.**

Note: *Chip cannot enter Halt/Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~1)*

Note: *FW must turn off Bandgap to obtain Tiny Current (VBGOUT=0)*

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode.
87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode.

SFR **D8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCON	–	–	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
R/W	–	–	R/W	R/W	R/W	R/W	R/W	
Reset	–	–	1	0	0	0	1	1

D8h.5 **STPSCK:** Set 1 to stop Slow clock in PDOWN mode.
D8h.4 **STPPCK:** Set 1 to stop UARTs/Timer0/Timer1/ADC clock in Idle mode for current reducing. If set, only Timer3 and pin interrupts are alive in Idle Mode.
D8h.3 **STPFCK:** Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
D8h.2 **SELFCK:** System clock source selection. This bit can be changed only when STPFCK=0.
0: Slow clock
1: Fast clock
D8h.1~0 **CLKPSC:** System clock prescaler. Effective after 16 clock cycles (Max.) delay
00: System clock is Fast/Slow clock divided by 16
01: System clock is Fast/Slow clock divided by 4
10: System clock is Fast/Slow clock divided by 2
11: System clock is Fast/Slow clock divided by 1

SFR 94h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	–	TM3CKS	WDTPSC		ADCKS		–	–
R/W	–	R/W	R/W		R/W		–	–
Reset	–	0	0	0	0	0	–	–

94h.6 **TM3CKS:** Timer3 Clock Source select
0: SRC/4
1: FRC/512

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT		EEPTE		
R/W	R/W	R/W	R/W	R/W		R/W		
Reset	0	0	0	0		1	1	

F7h.4 **VBGOUT: VBG** Bandgap voltage output to P3.2
0: Disable
1: Enable

6. Interrupt & Wake-up

This Chip has a 11-source four-level priority interrupt structure. Only the Pin Interrupts can wake up CPU from Halt/Stop mode. Each interrupt source has its own enable control bit. An interrupt event will set its individual Interrupt Flag, no matter whether its interrupt enable control bit is 0 or 1. The Interrupt vectors and flags are list below.

Vector	INT Num C51	Flag	Description
0003	0	IE0	INT0 external pin Interrupt (can wake up Halt/Stop mode)
000B	1	TF0	Timer0 Interrupt
0013	2	IE1	INT1 external pin Interrupt (can wake up Halt/Stop mode)
001B	3	TF1	Timer1 Interrupt
0023	4	RI+TI	Serial Port (UART) Interrupt
002B		-	Reserved
0033	6	-	Reserved for ICE mode use
003B	7	TF3	Timer3 Interrupt
0043	8	PCIF	Port0/Port3 external pin change Interrupt (can wake up Halt/Stop mode)
004B	9	LVDIF	LVD interrupt
0053	10	ADIF	ADC interrupt
005B	11	EEPIF	EEP Write Finish Interrupt
0063		-	Reserved
006B		-	Reserved
0073	14	PWM0IF+PWM1IF	PWM0~1 Interrupt

Interrupt Vector & Flag

INT Vector	INT Num C51	Flag	INT Enable	Sub INT enable	INT Flag
0003	0	IE0	IE A8.0		TCON 88.1
000B	1	TF0	IE A8.1		TCON 88.5
0013	2	IE1	IE A8.2		TCON 88.3
001B	3	TF1	IE A8.3		TCON 88.7
0023	4	RI+TI	IE A8.4		SCON 98.1~0
002B	5				
0033	6				
003B	7	TF3	INTE1 A9.0		INTFLG 95.0
0043	8	PCIF	INTE1 A9.1		INTFLG 95.1
004B	9	LVDIF	INTE1 A9.2		INTFLG 95.7
0053	10	ADIF	INTE1 A9.3		INTFLG 95.4
005B	11	EEPIF	INTE1 A9.4		INTFLG 95.6
0063	12				
006B	13				
0073	14	PWM0IF+PWM1IF	INTE1 A9.4	INTE2 84.0 INTE2 84.1	INTPWM 86.0 INTPWM 86.1

Interrupt related SFR

6.1 Interrupt Enable and Priority Control

The IE and INTE1 SFRs decide whether the pending interrupt is serviced by CPU. The IP, IPH, IP1 and IP1H SFRs decide the interrupt priority. An interrupt will be serviced as long as an interrupt of equal or higher priority is not already being serviced. If an interrupt of equal or higher level priority is being serviced, the new interrupt will wait until it is finished before being serviced. If a lower priority level interrupt is being serviced, it will be stopped and the new interrupt serviced. When the new interrupt is finished, the lower priority level interrupt that was stopped will be completed.

6.2 Suggestions on interrupting subroutines

When entering the interrupt program, in addition to the traditionally known SFR A or PSW that should be PUSH, POP, some SFRs used for indexing should also be added to the ranks of PUSH POP, such as PORTIDX. To avoid writing and reading these SFRs before and after the interruption may cause inconsistencies. In addition, PWMDH, PWMDL, PWMPRDH or PWMPRDL is a 16-bit operation, and the program should avoid interrupts when writing and reading the high byte and low byte. If you are reading and writing these 16-bit SFRs in the meantime an interrupt occurs. And these SFRs are read and written in the interrupt. It is easy to cause read and write errors. For the 16-bit PWM period and duty to read and write, it is recommended to update the data only in the main program, or update the data only in the interrupt to avoid possible errors.

SFR 84**h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	–	–	–	–		PWM1IE	PWM0IE
R/W	–	–	–	–	–		W	W
Reset	–	–	–	–	–		0	0

84h.1 **PWM1IE:** PWM1 Interrupt Enable
0: disable
1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)

84h.0 **PWM0IE:** PWM0 Interrupt Enable
0: disable
1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–		ES	ET1	EX1	ET0	EX0
R/W	R/W	–		R/W	R/W	R/W	R/W	R/W
Reset	0	–		0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control
0: Disable all Interrupts
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.4 **ES:** Serial Port (UART) interrupt enable
0: Disable Serial Port (UART) interrupt
1: Enable Serial Port (UART) interrupt

A8h.3 **ET1:** Timer1 interrupt enable
0: Disable Timer1 interrupt
1: Enable Timer1 interrupt

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

A8h.1 **ET0:** Timer0 interrupt enable
0: Disable Timer0 interrupt
1: Enable Timer0 interrupt

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1.

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE			EEPIE	ADIE	LVDIE	PCIE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

A9h.7 **PWMIE:** PWM0~PWM1 interrupt enable
0: Disable PWM0~PWM1 interrupt
1: Enable PWM0~PWM1 interrupt

A9h.4 **EEPIE:** EEP write finish interrupt enable
0: Disable ADC interrupt
1: Enable ADC interrupt

A9h.3 **ADIE:** ADC interrupt enable
0: Disable ADC interrupt
1: Enable ADC interrupt

A9h.2 **LVDIE:** LVD interrupt enable
0: Disable LVD interrupt
1: Enable LVD interrupt

A9h.1 **PCIE:** Port1, Port3 pin change interrupt enable. This bit does not affect Halt/Stop mode wake up capability.
0: Disable Port1, Port3 pin change interrupt
1: Enable Port1, Port3 pin change interrupt

A9h.0 **TM3IE:**Timer3 interrupt enable
0: Disable Timer3 interrupt
1: Enable Timer3 interrupt

SFR **B9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IPH	–	–		PSH	PT1H	PX1H	PT0H	PX0H
R/W	–	–		R/W	R/W	R/W	R/W	R/W
Reset	–	–		0	0	0	0	0

SFR **B8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP	–	–		PS	PT1	PX1	PT0	PX0
R/W	–	–		R/W	R/W	R/W	R/W	R/W
Reset	–	–		0	0	0	0	0

B9h.4, B8h.4 **PSH,PS:** Serial Port (UART) Interrupt Priority control. Definition as above
B9h.3, B8h.3 **PT1H,PT1:** Timer1 Timer1 Interrupt Priority control. Definition as above.
B9h.2, B8h.2 **PX1H,PX1:** External INT1 pin Interrupt Priority control. Definition as above
B9h.1, B8h.1 **PT0H,PT0:** Timer0 Interrupt Priority control. Definition as above.
B9h.0, B8h.0 **PX0H,PX0:** External INT0 pin Interrupt Priority control. Definition as above.

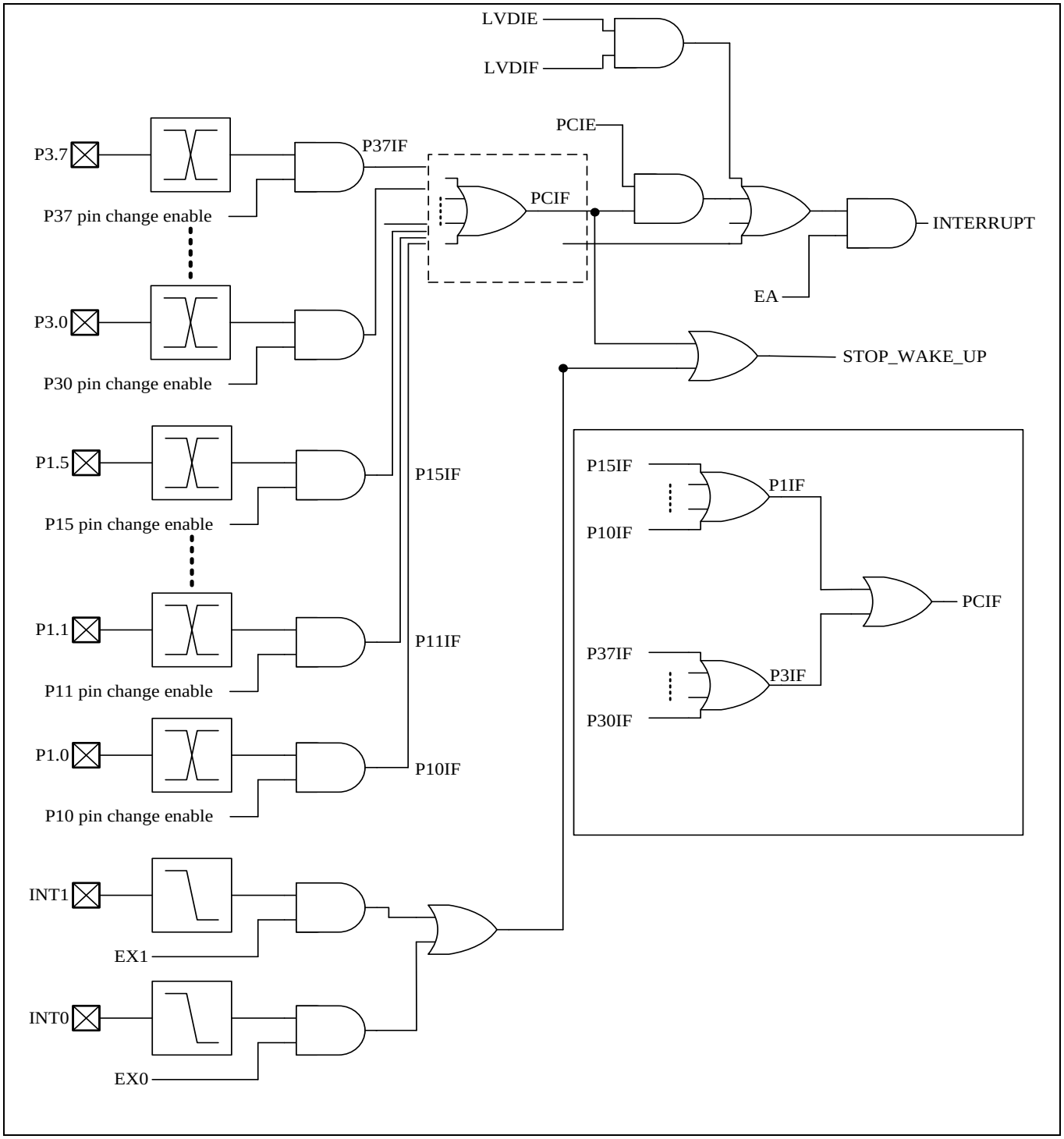
SFR **BBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1H	PPWMH			PEEPH	PADIH	PLVDH	PPCH	PT3H
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

SFR **BAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IP1	PPWM			PEEP	PADI	PLVD	PPC	PT3
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

BBh.7, BAh.7 **PPWMH,PPWM:** PWM0~PWM1 Interrupt Priority control. Definition as above.
BBh.4, BAh.4 **PEEPH,PEEP:** EEP write finish Interrupt Priority control. Definition as above
BBh.3, BAh.3 **PADIH,PADI:** ADC Interrupt Priority control. Definition as above.
BBh.2, BAh.2 **PLVDH,PLVD:** LVD Interrupt Priority control. Definition as above.
BBh.1, BAh.1 **PPCH,PPC:** 端口 0 / 端口 3 Pin Change Interrupt Priority control. Definition as above.
BBh.0, BAh.0 **PT3,PT3:** Timer3 Interrupt Priority control. Definition as above.

6.3 Pin Interrupt and LVD interrupt

Pin interrupts include INT0~INT1 and Port1, Port3 pin level change interrupts. The pin changes of INT0~INT1 and Port1, Port3 also have wake-up function. INT0 and INT1 are the falling edge or low level triggered by the 8051 standard. Port1, Port3 pin change interrupt is triggered by IO status change. PORT1 pin change enable are setting by P1MOD10/P1MOD32/P1MOD54. And PORT3 pin change enable are setting by P3MOD10/P3MOD32/P3MOD54/P3MOD76. For details, see Chapter 7. The LVD interrupt can be used to detect the VCC voltage level and generate an interrupt.



Pin interrupt/Wake up & LVD interrupt

Note: *Chip cannot enter Halt/Stop Mode if INTn pin is low and wakeup is enabled. (INTn=0 and EXn=1, n=0~1)*

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	EEPIF	EEPBUSY	ADIF	–	–	PCIF	TF3
R/W	R/W	R/W	R	R/W	–	–	R/W	R/W
Reset	0	0	0	0	–	–	0	0

95h.7 **LVDIF:** Low Voltage Detect interrupt flag
Set by H/W. S/W writes 7Fh to INTFLG to clear this flag.

95h.1 **PCIF:** Port1/Port3 Pin change interrupt flag
Set by H/W when Port1~Port3 pin state change is detected and its interrupt enable bit is set.
Cleared automatically when the program performs the interrupt service routine.
S/W can write 0 to clear all pin change interrupt flags

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect..*

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.3 **IE1:** External Interrupt 1 (INT1 pin) edge flag
Set by H/W when an INT1 pin falling edge is detected, no matter the EX1 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine

88h.2 **IT1:** External Interrupt 1 control bit
0: Low level active (level triggered) for INT1 pin
1: Falling edge active (edge triggered) for INT1 pin

88h.1 **IE0:** External Interrupt 0 (INT0 pin) edge flag
Set by H/W when an INT0 pin falling edge is detected, no matter the EX0 is 0 or 1.
It is cleared automatically when the program performs the interrupt service routine.

88h.0 **IT0:** External Interrupt 0 control bit
0: Low level active (level triggered) for INT0 pin
1: Falling edge active (edge triggered) for INT0 pin

SFR **A8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IE	EA	–	–	ES	ET1	EX1	ET0	EX0
R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W
Reset	0	–	–	0	0	0	0	0

A8h.7 **EA:** Global interrupt enable control.
0: Disable all Interrupts
1: Each interrupt is enabled or disabled by its individual interrupt control bit

A8h.2 **EX1:** External INT1 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT1 pin Interrupt and Halt/Stop mode wake up
1: Enable INT1 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1

A8h.0 **EX0:** External INT0 pin Interrupt enable and Halt/Stop mode wake up enable
0: Disable INT0 pin Interrupt and Halt/Stop mode wake up
1: Enable INT0 pin Interrupt and Halt/Stop mode wake up, it can wake up CPU from Halt/Stop mode no matter EA is 0 or 1

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE	–	–	EEPIE	ADIE	LVDIE	PCIE	TM3IE
R/W	R/W	–	–	R/W	R/W	R/W	R/W	R/W
Reset	0	–	–	0	0	0	0	0

A9h.2 **LVDIE:** LVD interrupt enable
0: Disable LVD interrupt
1: Enable LVD interrupt

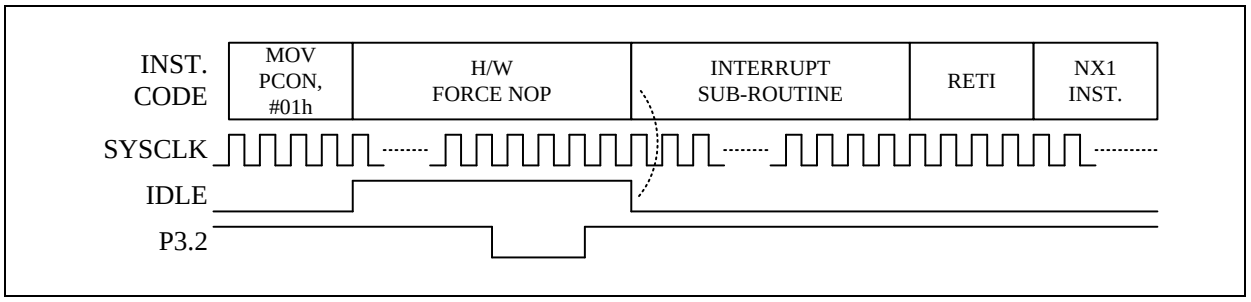
A9h.1 **PCIE:** Port1, Port3 pin change interrupt enable. This bit does not affect Halt/Stop mode wake up capability.
0: Disable Port1, Port pin change interrupt
1: Enable Port1, Port3 pin change interrupt

SFR **BFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LVDS	LVDM	LVDO	–	LVDPD	LVDSEL			
R/W	R/W	R	–	R/W	R/W	R/W	R/W	R/W
Reset	0	0	–	0	0	0	0	0

BFh.3~0 **LVDSEL:** Low Voltage Detect select
0000: set LVD at 1.62V
0001: set LVD at 1.71V
0010: set LVD at 1.83V
0011: set LVD at 1.95V
0100: set LVD at 2.07V
0101: set LVD at 2.19V
0110: set LVD at 2.31V
0111: set LVD at 2.43V
1000: set LVD at 2.56V
1001: set LVD at 2.68V
1010: set LVD at 2.81V
1011: set LVD at 2.93V
1100: set LVD at 3.05V
1101: set LVD at 3.17V
1110: set LVD at 3.30V
1111: set LVD at 3.42V

6.4 Idle mode Wake up and Interrupt

Idle mode is waked up by enabled Interrupts, which means individual interrupt enable bit (ex: EX0) and EA bit must be both set to 1 to establish Idle mode wake up capability. All enabled Interrupts change (INT0~INT1, Timers, PWM, ADC, and UARTs) can wake up CPU from Idle mode. Upon Idle wake-up, Interrupt service routine is entered immediately. “The first instruction behind IDL (PCON.0) setting” is executed after interrupt service routine return.



EA=EX0=1, Idle mode wake-up and Interrupt by P3.2 (INT0)

SFR **87h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCON	SMOD	–	–	–	GF1	GF0	PD	IDL
R/W	R/W	–	–	–	R/W	R/W	R/W	R/W
Reset	0	–	–	–	0	0	0	0

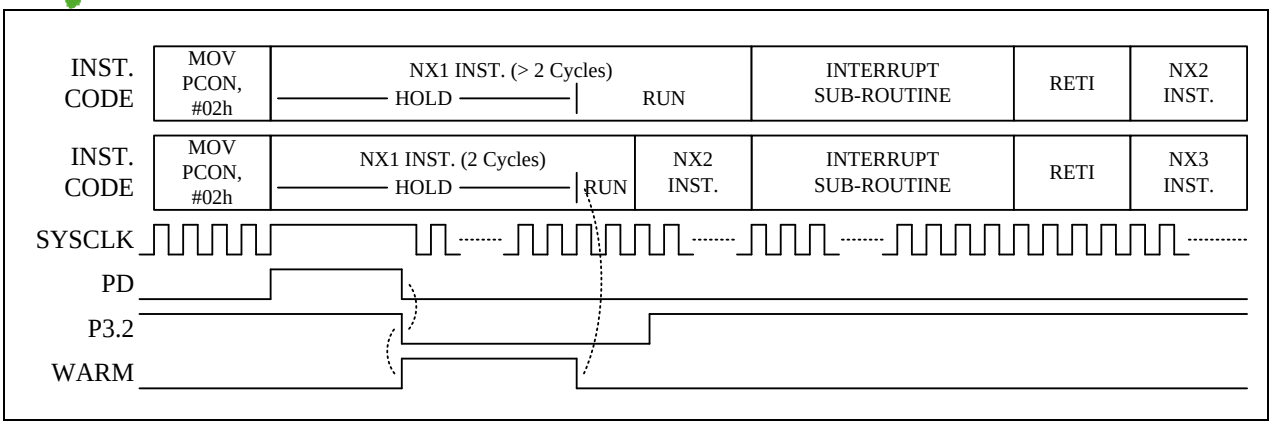
87h.1 **PD:** Power down control bit, set 1 to enter Halt/Stop mode

87h.0 **IDL:** Idle mode control bit, set 1 to enter Idle mode

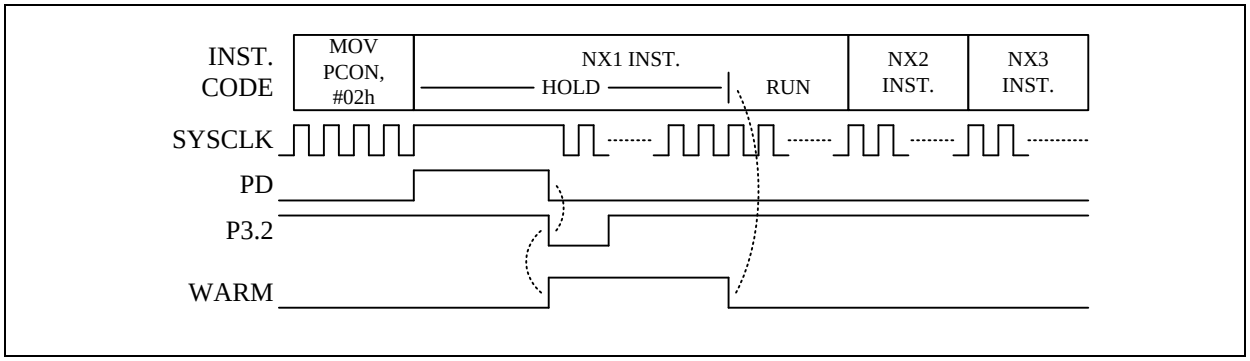
6.5 Halt/Stop mode Wake up and Interrupt

Halt/Stop mode wake up is simple, as long as the individual pin interrupt enable bit (ex: EX0) is set, the pin wake up capability is asserted. Set EX0/EX1 can enable INT0/INT1 pins’ Halt/Stop mode wake up capability. Set P1MOD10/P1MOD32/P1MOD54, P3MOD10/P3MOD32/P3MOD54/P3MOD76 can enable Port0, Port3 Halt/Stop mode wake up capability. Upon Halt/Stop wake up, “the first instruction behind PD setting (PCON.1)” is executed immediately before Interrupt service. Interrupt entry requires EA=1 and trigger state of the pin staying sufficiently long to be observed by the System clock. This feature allows CPU to enter or not enter Interrupt sub-routine after Halt/Stop mode wake up.

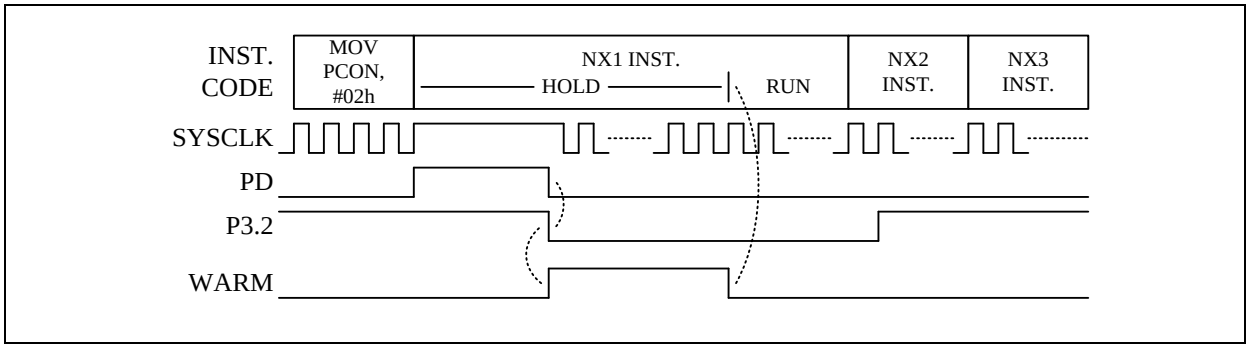
Note: *It is recommended to place the NX1/NX2 with NOP Instruction in figures below.*



EA=EX0=1, P3.2 (INT0) is sampled after warm-up, Halt/Stop mode wake-up and Interrupt



EA=EX0=1, Halt/Stop mode wake-up but not Interrupt. P3.2 (INT0) pulse too narrow



EX0= 1, EA=0, P3.2 (INT0) Halt/Stop mode wake-up but not Interrupt

7. I/O Ports

The Chip has total 14 multi-function I/O pins. All I/O pins follow the standard 8051 “Read-Modify-Write” feature. The instructions that read the SFR rather than the Pin State are the ones that read a port or port bit value, possibly change it, and then rewrite it to the SFR (ex: ANL P1, A; INC P2; CPL P3.0).

When entering the interrupt program, in addition to the traditionally known SFR A or PSW that should be PUSH, POP, some SFRs used for indexing should also be added to the ranks of PUSH POP, such as PORTIDX. To avoid writing and reading these SFRs before and after the interruption may cause inconsistencies.

7.1 Port1, Port3

These pins can operate in four different modes as below.

P3MOD76 P1MOD54/ P3MOD54 P1MOD32/ P3MOD32 P1MOD10/ P3MOD10					Pin State	Interrupt	Wake-up
MODE 0	0	0	0	0	Open Drain with pull-up (for INT0/INT1)	Y	Y
MODE 1	0	0	0	1	Open Drain **(Default)** (for INT0/INT1)	Y	Y
MODE 2	0	0	1	0	CMOS Output	-	-
MODE 3	0	0	1	1	ADC channel	-	-
MODE 4	0	1	0	0	Open Drain with pull-down	Y	Y
MODE 5	0	1	0	1	Open Drain	Y	Y
MODE 6	0	1	1	0	CMOS Output	-	-
MODE 7	0	1	1	1	-	-	-
MODE 8	1	0	0	0	Open Drain with pull-up (for pin change from Halt/Stop)	Y	Y
MODE 9	1	0	0	1	Open Drain (for pin change from Halt/Stop)	Y	Y
MODE 10	1	0	1	0	CMOS Output	-	-
MODE 11	1	0	1	1	PWMO	-	-
MODE 12	1	1	0	0	Open Drain with pull-down (for pin change from Halt/Stop)	Y	Y
MODE 13	1	1	0	1	Open Drain (for pin change from Halt/Stop)	Y	Y
MODE 14	1	1	1	0	T0OE/T1OE/TCOE CMOS Output	-	-
MODE 15	1	1	1	1	LCD 1/2 Vcc bias	-	-

Table 7.1 Port1/Port3 I/O Pin Function Table

P1MOD10 is set to P1.1 and P1.0，high 4 bits are set to P1.1, low 4 bits are set to P1.0
P1MOD32 is set to P1.3 and P1.2，high 4 bits are set to P1.3, low 4 bits are set to P1.2
P1MOD54 is set to P1.5 and P1.4，high 4 bits are set to P1.5, low 4 bits are set to P1.4

P3MOD10 is set to P3.1 and P3.0，high 4 bits are set to P3.1, low 4 bits are set to P3.0
P3MOD32 is set to P3.3 and P3.2，high 4 bits are set to P3.3, low 4 bits are set to P3.2
P3MOD54 is set to P3.5 and P3.4，high 4 bits are set to P3.5, low 4 bits are set to P3.4
P3MOD76 is set to P3.7 and P3.6，high 4 bits are set to P3.7, low 4 bits are set to P3.6

Mode	Port0~Port3 pin function	Px.n SFR data	Pin State	Resistor Pull-up	Resistor Pull-down	Digital Input
MODE0 MODE 8	Open Drain with pull-up	0	Drive Low	N	N	N
		1	Pull-up	Y	N	Y
MODE 4 MODE 12	Open Drain with pull-down	0	Drive Low	N	N	N
		1	Pull-down	N	Y	Y
MODE 1 MODE 5 MODE 9 MODE 13	Open Drain	0	Drive Low	N	N	N
		1	Hi-Z	N	N	Y
MODE 2 MODE 6 MODE 10	CMOS Output	0	Drive Low	N	N	N
		1	Drive High	N	N	N
MODE 3	ADC channel	X (don't care)	–	N	N	N
MODE 7	-	–	–	–	–	–
MODE 11	PWMO	X (don't care)	–	N	N	N
MODE 14	T0OE/T1OE/TCOE	X (don't care)	–	N	N	N
MODE 15	LCD 1/2 Vcc bias output	X (don't care)	–	Y	Y	N

I/O Pin Function Table

If a Port0, Port3 pin is used for Schmitt-trigger input, S/W must set the I/O pin to MODE0, MODE1, MODE4, MODE5, MODE8, MODE9, MODE12 or MODE13 (Open Drain, Open Drain with pull-up or Open Drain with pull-down), and set the corresponding Port Data SFR to 1 to disable the pin's output driving circuitry.

By setting IOVIS (SFR EFh.2), there are two different input level options input high level (VIH) and input low level (VIL) for port 1 and port 3.

Beside I/O port function, each Port0, Port3 has one or more alternative functions, such as ADC and LCD. Most of the functions are activated by setting the individual pin mode control SFR to MODE3, MODE7, MODE11 or MODE15. Port1/Port3 pins have standard 8051 auxiliary definition such as INT0/INT1, T0/T1, or RXD/TXD. These pin functions need to set the pin mode SFR to MODE0, MODE1, MODE5, MODE8, MODE9 or MODE13 (Open Drain or Open Drain with pull-up), and keep the P1.n/P3.n SFR at 1.

Pin Name	Wake-up Interrupt	CKO	ADC	LCD	PWM	UART	others
P1.5	Y		AD13	Y			
P1.4	Y	CKO	AD11	Y	PWM3		
P1.3	Y		AD10	Y	PWM2		
P1.2	Y		AD09	Y	PWM1		
P1.1	Y		AD08	Y	PWM0P		
P1.0	Y		AD07	Y	PWM0N		

Port1 multi-function Table

Pin Name	Wake-up Interrupt	CKO	ADC	LCD	PWM	UART	others
P3.7	Y			Y	PWM3		RSTn/VPP
P3.6	Y		AD06	Y	PWM0P		
P3.5	Y	T1O	AD05	Y			T1
P3.4	Y	T0O	AD04	Y	PWM2		T0
P3.3	Y		AD03	Y	PWM1	TXD (RXD)	INT1
P3.2	Y		AD01	Y	PWM0N	RXD (TXD)	INT0 VBGO
P3.1	Y		AD01	Y		TXD (RXD)	
P3.0	Y		AD00	Y		RXD (TXD)	

Port3 multi-function Table

The necessary SFR setting for Port0~Port3 pin's alternative function is list below.

Alternative Function	PINMODxx	Px.n SFR data	Pin State	Other necessary SFR setting
INT0, INT1	**0000**	1	Input with Pull-up	
	0001	1	Input	
T0, T1	**x000**	1	Input with Pull-up	
	xx01	1	Input	
RXD	**x000**	1	UART RX (Input with Pull-up)	UARTCON
	xx01	1	UART RX(Input)	
TXD	**x000**	1	UART TX 输出(Open Drain Output, Pull-up)	
	xx01	1	UART TX 输出(Open Drain Output)	
VBGO	**0011**	X	Bandgap Voltage output	VBGOUT
AD0~AD6 AD7~AD11, AD13	**0011**	X	ADC Channel	ADCHS
LCD	**1111**	X	LCD 1/2 V_{CC} bias Output	
T0O,T1O, CKO	**xx10**	X	Clock Output (CMOS Push-Pull)	T0OE T1OE TCOE
PWM0P~PWM0N PWM1~PWM3	**1011**	X	PWM Output (CMOS Push-Pull)	

For tables above, a "**CMOS Output**" pin means it can sink and drive at least 4 mA current. It is not recommended to use such pin as input function.

An "**Open Drain**" pin means it can sink at least 4 mA current but only drive a small current (<20 μA). It can be used as input or output function and typically needs an external pull up resistor.

SFR **90h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1	-	-	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset	-	-	1	1	1	1	1	1

90h.7~0 **P0:** Port0 data

SFR **B0h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

B0h.7~0 **P3:** Port3 data

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD10	P1MOD1				P1MOD0			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

91h.7~4 **P1MOD1:** P1.1 pin control
0000~1111: see table 7.1

91h.3~0 **PINMOD0:** P1.0 pin control
0000~1111: see table 7.1

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD32	P1MOD3				P1MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

92h.7~4 **P1MOD3:** P1.3 pin control
0000~1111: see table 7.1

92h.3~0 **P1MOD2:** P1.2 pin control
0000~1111: see table 7.1

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD54	P1MOD5				P1MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ah.7~4 **P1MOD5:** P1.5 pin control
0000~1111: see table 7.1

9Ah.3~0 **P1MOD4:** P1.4 pin control
0000~1111: see table 7.1

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD10	P3MOD1				P3MOD0			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Bh.7~4 **P3MOD1:** P3.1 pin control
0000~1111: see table 7.1

9Bh.3~0 **P3MOD0:** P3.0 pin control
0000~1111: see table 7.1

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD32	P3MOD3				P3MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ch.7~4 **P3MOD3:** P3.3 pin control
0000~1111: see table 7.1

9Ch.3~0 **P3MOD2:** P3.2 pin control
0000~1111: see table 7.1

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD54	P3MOD5				P3MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Dh.7~4 **P3MOD5:** P3.5 pin control
0000~1111: see table 7.1

9Dh.3~0 **P3MOD4:** P3.4 pin control
0000~1111: see table 7.1

SFR **9Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD76	P3MOD7				P3MOD6			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Eh.7~4 **P3MOD7:** P3.7 pin control
0000~1111: see table 7.1

9Eh.3~0 **P3MOD6:** P3.6 pin control
0000~1111: see table 7.1

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UARTCON					-	UARTPS		
R/W					-	R/W		
					-	0	0	1

93h.2~0 **UARTPS:** UART pin select
0000: RXD/TXD = P3.0/P3.1
0001: RXD/TXD = P3.2/P3.3
0010: RXD/TXD = P3.1/P3.0
0011: RXD/TXD = P3.3/P3.2
0100: RXD/TXD = P3.1/P3.1, 1-wire mode
0101: RXD/TXD = P3.3/P3.3, 1-wire mode
0110: RXD/TXD = P3.0/P3.0, 1-wire mode
0111: RXD/TXD = P3.2/P3.2, 1-wire mode

SFR **F7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX2	WDTE		PWRSAV	VBGOUT		EEPTE		
R/W	R/W	R/W	R/W	R/W		R/W		
Reset	0	0	0	0		1	1	

F7h.4 **VBGOUT:** Bandgap voltage output control
0: Disable Bandgap voltage output to P3.2 pin
1: Enable Bandgap voltage output to P3.2 pin

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCHSEL	ADCHS					ADCVREFS	VBGSEL	
R/W	R/W					R/W	R/W	
Reset				1	1	0	0	0

B6h.4~0 **ADCHS:** ADC Channel Selecttion

00000: CH0（P3.0）
00001: CH1（P3.1）
00010: CH2（P3.2）
00011: CH3（P3.3）
00100: CH4（P3.4）
00101: CH5（P3.5）
00110: CH6（P3.6）
00111: CH7（P1.0）
01000: CH8（P1.1）
01001: CH9（P1.2）
01010: CH10（P1.3）
01011: CH11（P1.4）
01100: CH12 VBG（Bandgap Boltage)
01001: CH13（P1.5）
others: Reserved
11110: VCC/201
11111: VCC/4

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX3	Warmtime	TM3PSC			-	IOVIS	-	-
R/W	R/W	R/W			-	R/W	-	-
Reset	0	0	0	0	-	0	-	-

EFh.2 **IOVIS:** IO Port input voltage level select
0: VIH=0.7VDD, VIL=0.3VDD
1: VIH=0.4VDD, VIL=0.2VDD (Not support in ICE emulation)

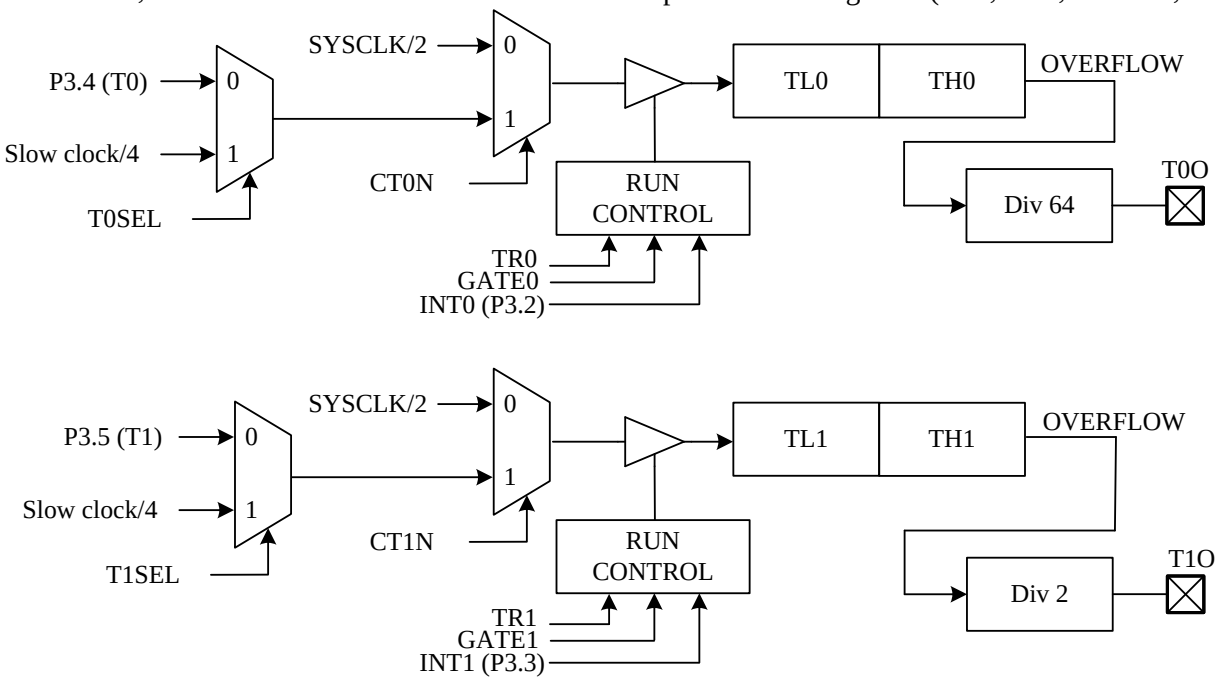
8. Timers

Timer0 and Timer1are provided as standard 8051 compatible timer/counter. Compare to the traditional 12T 8051, the Chip's Timer0/1 use 2 System clock cycle as the time base unit. That is, in timer mode, these timers increase at every “2 System clock” rate; in counter mode, T0/T1 pin input pulse must be wider than 2 System clock to be seen by this device. In addition to the standard 8051 timers function

The device can generate various frequency waveform pin outputs for the buzzer. The T0O pin outputs a "Timer0 overflow divided by 64" signal, while the T1O pin outputs a "Timer1 overflow divided by 2" signal. Set the pin mode of P3.4 or P3.5 to mode 14 to output T0O or T1O, see Table 7.1 for more details.

8.1 Timer0/1

TCON and TMOD are used to set the mode of operation and to control the running and interrupt generation of the Timer0/1, with the timer/counter values stored in two pairs of 8-bit registers (TL0, TH0, and TL1, TH1).



Timer0 and Timer1 Structure

SFR **88h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TCON	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

88h.7 **TF1:** Timer1 overflow flag
Set by H/W when Timer/Counter 1 overflows.
Cleared by H/W when CPU vectors into the interrupt service routine

88h.6 **TR1:** Timer1 run control
0: Timer1 stops
1: Timer1 runs

88h.5 **TF0:** Timer0 overflow flag
Set by H/W when Timer/Counter 0 overflows
Cleared by H/W when CPU vectors into the interrupt service routine.

88h.4 **TR0:** Timer0 run control
0: Timer0 stops
1: Timer0 runs

SFR **89h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMOD	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
R/W	R/W	R/W	R/W		R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

89h.7 **GATE1:** Timer1 gating control bit
0: Timer1 enable when TR1 bit is set
1: Timer1 enable only while the INT1 pin is high and TR1 bit is set

89h.6 **CT1N:** Timer1 Counter/Timer select bit
0: Timer mode, Timer1 data increases at 2 System clock cycle rate
1: Counter mode, Timer1 data increases at T1 pin's negative edge

89h.5~4 **TMOD1:** Timer1 mode select
00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow.
11: Timer1 stops

89h.3 **GATE0:** Timer0 gating control bit
0: Timer0 enable when TR0 bit is set
1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

89h.2 **CT0N:** Timer0 Counter/Timer select bit
0: Timer mode, Timer0 data increases at 2 System clock cycle rate
1: Counter mode, Timer0 data increases at T0 pin's negative edge

89h.1~0 **TMOD0:** Timer0 mode select
00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0)
01: 16-bit timer/counter
10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow.
11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.

SFR **8Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL0	TL0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ah.7~0 **TL0:** Timer0 data low byte

SFR **8Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TL1	TL1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Bh.7~0 **TL1:** Timer1 data low byte

SFR **8Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH0	TH0							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Ch.7~0 **TH0:** Timer0 data high byte

SFR **8Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TH1	TH1							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

8Dh.7~0 **TH1:** Timer1 data high byte

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	CLRPWM0	ADSOC	CLRPWM1	T0SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.2 **T0SEL:** Timer0 counter mode（CT0N = 1）input select
0: P3.4(T1) pin(8051standard)
1: Slow clock divide by 4（SLOWCLK/4）

F8h.1 **T1SEL:** Timer1 counter mode（CT1N = 1）input select
0: P3.5(T1) pin (8051standard)
1: Slow clock divide by 4（SLOWCLK/4）

***Note**: See also Chapter 6 for more information on Timer0/1 interrupt enable and priority.*
***Note**: See also Chapter 7 for details on T0O pin output settings.*

8.2 Timer3

Timer3 works as a time-base counter, which generates interrupts periodically. It generates an interrupt flag (TF3) with the clock divided by 65536, 32768, 8192, … or 8 depending on the TM3PSC SFR. The Timer3 clock source is Slow clock SRC/4 or FRC/512.

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	–	TM3CKS	WDTPSC		ADCKS		-	-
R/W	–	R/W	R/W		R/W		-	-
Reset	–	0	0	0	-	-	0	0

94h.6 **TM3CKS:** Timer3 Clock Source select
0: SRC/4
1: FRC/512

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	EEPIF	EEPBUSY–	ADIF	–	–	PCIF	TF3
R/W	R/W	R/W	R	R/W	–	–	R/W	R/W
Reset	0	0	0	0	–	–	0	0

95h.0 **TF3:** Timer3 Interrupt Flag
Set by H/W when Timer3 reaches TM3PSC setting cycles. Cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect*

SFR **EFh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX3	Warmtime	TM3PSC			-	IOVIS	-	-
R/W	R/W	R/W			-	R/W	-	-
Reset	0	0	0	0	-	0	-	-

EFh.6~3 **TM3PSC:** Timer3 Interrupt rate
000: Timer3 Interrupt rate is 65536 Timer3 clock cycle
001: Timer3 Interrupt rate is 32768 Timer3 clock cycle
010: Timer3 Interrupt rate is 16384 Timer3 clock cycle
011: Timer3 Interrupt rate is 8192 Timer3 clock cycle
100: Timer3 Interrupt rate is 4096 Timer3 clock cycle
101: Timer3 Interrupt rate is 2048 Timer3 clock cycle
110: Timer3 Interrupt rate is 1024 Timer3 clock cycle
111: Timer3 Interrupt rate is 512 Timer3 clock cycle

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	CLRPWM0	ADSOC	CLRPWM1	T0SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F8h.6 **CLRTM3:** Set 1 to clear Timer3, H/W auto clear it at next clock cycle

Note: *also refer to Section 6 for more information about Timer3 Interrupt enable and priority.*

9. UART

The chip has a UART module

The UART is an 8051 full-duplex UART, and the UART uses the SFR of SCON and SBUF. SCON is the control register and SBUF is the data register. Data is written to SBUF for transmission, and when SBUF is read, receive data is available. The received data and transmit data registers are completely independent. Mode0 and Mode2 are not supported, and UART always enables UARTBRP to define a new baud rate.

By setting the register UARTCON, the UART can provide different TXD and RXD pin options. TXD and RXD are also interchangeable. The chip also offers single-wire mode. If single-wire mode is set, the same pin is used for both sending and receiving data, it provides more flexibility in application.

SFR **98h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SCON	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

98h.7~6 **SM0,SM1:** UART serial port mode select bit 0,1
00: mode0: Not support
01: mode1: 8 bit UART, Baud Rate is variable
10: mode2: Not support
11: mode3: 9 bit UART, Baud Rate is variable

98h.5 **SM2:** Serial port mode select bit 2
M2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.

98h.4 **REN:** UART reception enable
0: Disable reception
1: Enable reception

98h.3 **TB8:** Transmit Bit 8, the ninth bit to be transmitted in Mode 2 and 3

98h.2 **RB8:** Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0

98h.1 **TI:** Transmit interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W.

98h.0 **RI:** Receive interrupt flag
Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.

SFR **99h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SBUF	SBUF							
R/W	R/W							
Reset	–	–	–	–	–	–	–	–

99h.7~0 **SBUF:** UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.

SFR **9Fh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UARTBRP	UARTBRP							
R/W	W							
Reset	0	0	0	0	0	0	0	0

9Fh.7~0 **UARTBRP:** Define UART baud rate prescaler.
UART baud rate = Fsys/16/UARTBRP

SFR **93h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
UARTCON	-	-	-	-	-	UARTPS		
R/W	-	-	-	-	-	R/W		
Reset	-	-	-	-	-	0	0	1

93h.2~0 **UARTPS:** UART pin select
0000: RXD/TXD = P3.0/P3.1
0001: RXD/TXD = P3.2/P3.3
0010: RXD/TXD = P3.1/P3.0
0011: RXD/TXD = P3.3/P3.2
0100: RXD/TXD = P3.1/P3.1, 1-wire mode
0101: RXD/TXD = P3.3/P3.3, 1-wire mode
0110: RXD/TXD = P3.0/P3.0, 1-wire mode
0111: RXD/TXD = P3.2/P3.2, 1-wire mode

FSYSCLK represents the system clock frequency.

The UART baud rate is set as follows

Mode 1, 3: Baud rate = Fsys/16/UARTBRP

- Mode 1, 3: Baud rate = Fsys/16/UARTBRP
- Mode 0, 2: Not supported

Note: *also refer to Section 6 for more information about UART Interrupt enable and priority.*
Note: *also refer to Section 8 for more information about how Timer2 controls UART clock.*

Fsys (Hz)	Expect Baud rate (bps)	UARTBRP	Generated Baud rate	Frequency offset (%)
16588800	19200	54	19200	0
16588800	28800	36	28800	0
16588800	38400	27	38400	0
16588800	57600	18	57600	0
16588800	115200	9	115200	0

When using UARTcommunication, Fsys needs to be calibrated to 16.5888±1% MHz

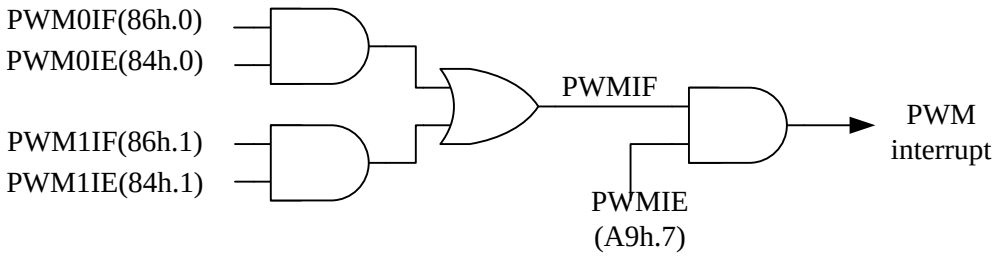
10. PWMs

The chip has two independent 16-bit PWM modules PWM0 and 16-bit PWM module PWM1. PWM0 has an independent 16-bit period and duty cycle, while the PWM1 module has an independent 16-bit period and 3 independent duty cycles to produce PWM1O/PWM2O/PWM3O. PWM0 can generate a varying frequency waveform with 65536 duty cycle resolution based on the PWM0 clock.

The PWM0 clock can select FRC double frequency (FRC x 2), FRC, FRC/256 or SRC as its clock source. PWM1 is based on the PWM1 clock and generates a changing frequency waveform with a duty cycle resolution of 65536. The PWM1 clock can select FRC double frequency (FRC x 2), FRC, FRC/256 or SRC as its clock source. Users need to pay attention to the setting, the period of PWM must be greater than the duty.

Set SFR PxMOD10, PxMOD32, PxMOD54 and PxMOD76 (x=1 or 3) to control PWM output. If PxMODX is set to mode 1011, relative PWM will be output automatically. For example, P1MOD10 = BBh, then PWM0P and PWM0N will be output to P1.1 and P1.0. (See Section 7)

The 16-bit period (PWM0PRD, PWM1PRD) and duty cycle (PWM0D~PWM3D) registers have low byte and high byte structures. The high byte can be accessed directly, but the low byte can only be accessed through the internal 8-bit buffer, and these register pairs must be read and written in a specific way. An important thing to note is that data transfers with an 8-bit buffer and its associated low byte are only performed when a write or read operation is performed on its corresponding high byte. ***Briefly speaking, write the low byte first, then the high byte. The high byte is read first, then the low byte.***

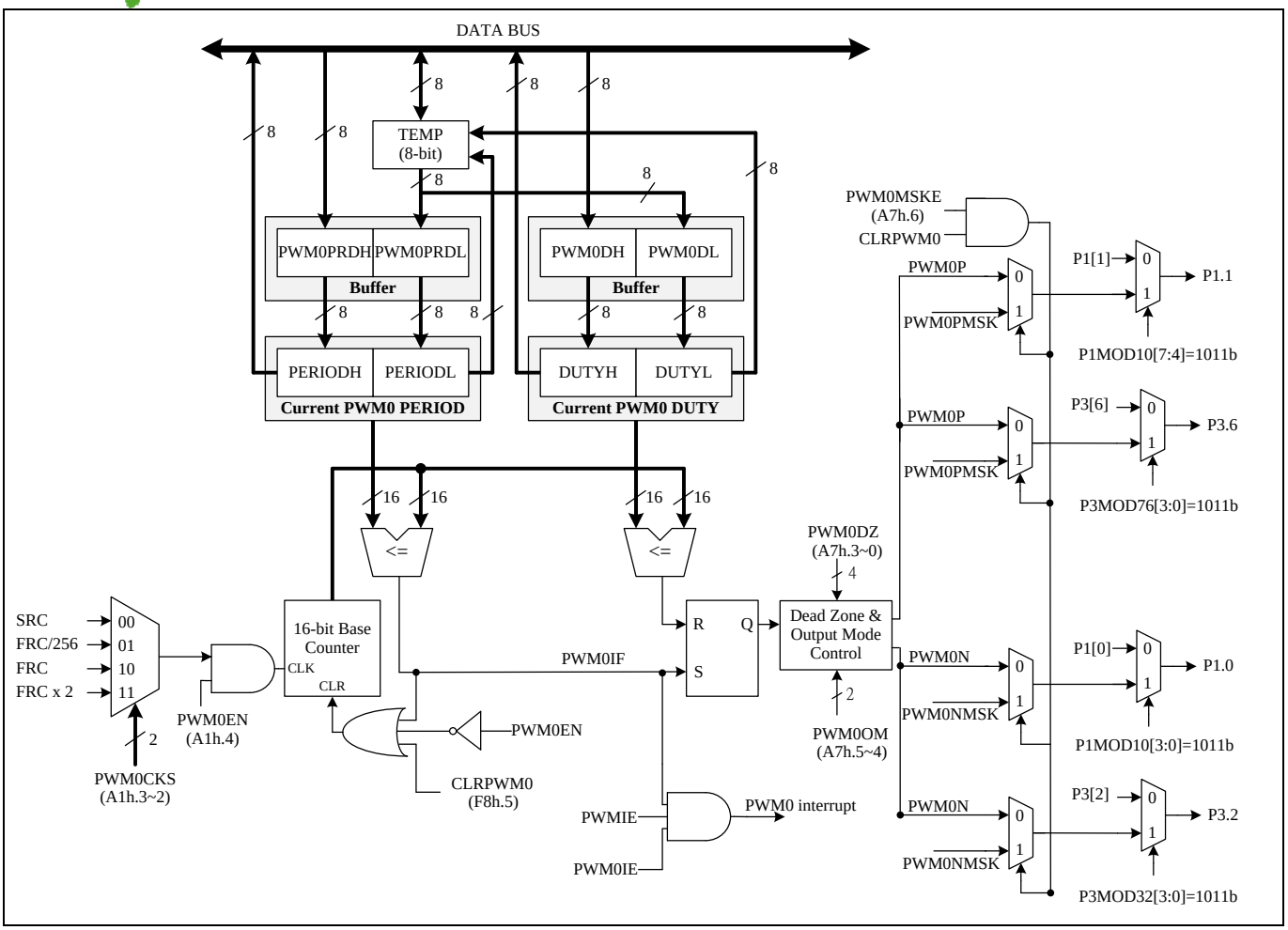


PWM Interrupt structure

10.1 PWM0 (PWM0P/PWM0N)

When CLRPWM0 is set to 1, PWM0 will be cleared and held, otherwise PWM0 will remain running. The structure of PWM0 is shown below. The PWM0 duty cycle can be changed by writing to SFRs PWM0DH and PWM0DL. Whenever the 16-bit radix counter matches the 16-bit PWM0 duty cycle register {PWM0DH, PWM0DL}, the PWM0 output signal is reset to low level. The period of PWM0 can be set by writing to SFRs PWM0PRDH and PWM0PRDL. As soon as a PWM duty cycle or period register is written, the new value is saved to its own buffer. H/W will update these values at the end of the current cycle or when PWM0 is cleared. PWM0 has a corresponding interrupt flag, which will be generated at the end of the cycle.

PWMDH, PWMDL, PWM0PRDH or PWM0PRDL is a 16-bit operation, and the program should avoid interrupts when writing and reading the high byte and low byte. If you are reading and writing these 16-bit SFRs in the meantime an interrupt occurs. And these SFRs are read and written in the interrupt. It is easy to cause read and write errors. For the 16-bit PWM period and duty to read and write, it is recommended to update the data only in the main program, or update the data only in the interrupt to avoid possible errors. PWM0 structure is shown as follow.

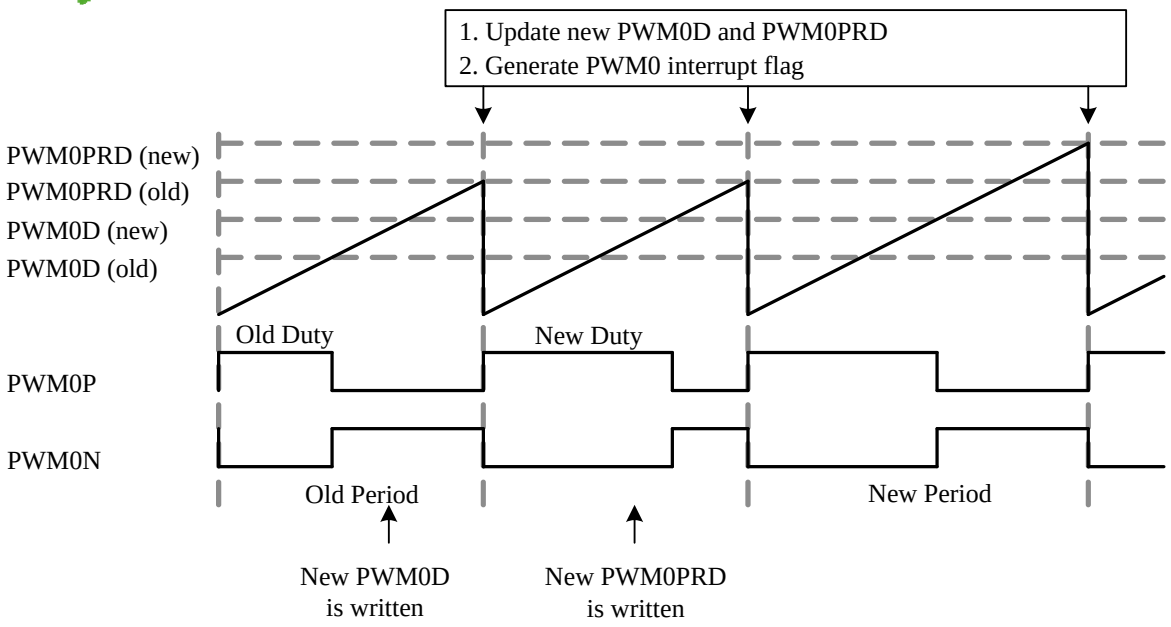


PWM0 Structure

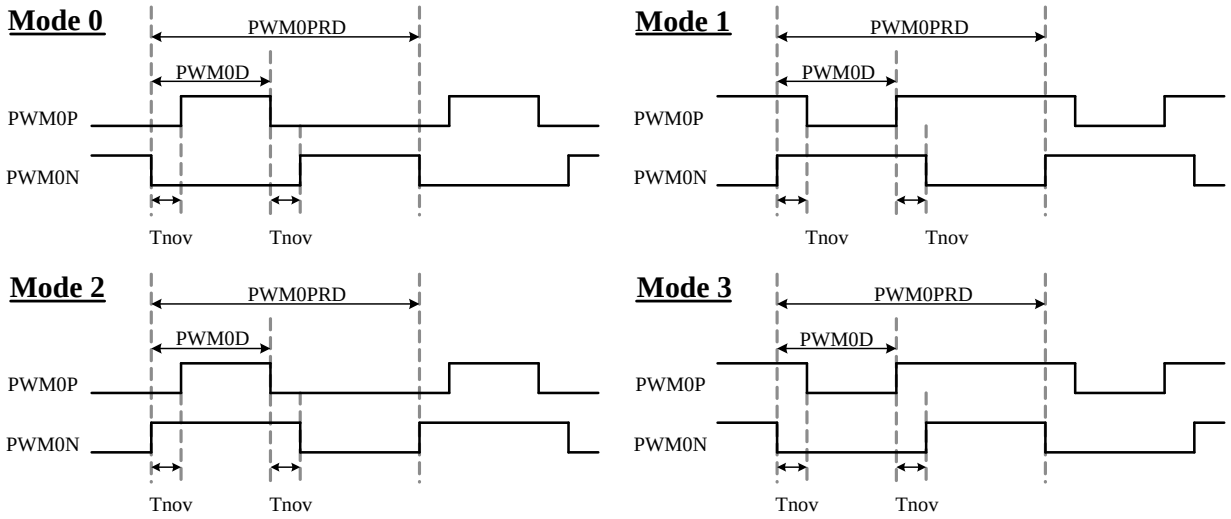
The PWM0 has two operation modes, normal mode and half-bridge mode. The PWM0 output signal can be output through PWM0P and PWM0N, with four different modes. These two outputs do not overlap with the time interval Tnov. Non-overlapping intervals are also called dead zones. Tnov is determined by setting the PWM0DZ bit. The 0~15 values of PWM0DZ are mapped to 0~15, 16 PWM0CLK cycles respectively. If PWM0DZ = 0, the PWM0 output is passed directly to PWM0P and PWM0N, so their waveforms have the same duty cycle. Note that if the high pulse width or low pulse width of the PWM0 output is shorter than Tnov, the actual waveform of these two outputs will be different from the expected waveform. If the PWM0MSKE bit is set, the output can be masked to force a fixed signal while S/W sets the CLRPWM0 bit set by H/W.

Normal Mode

The normal mode PWM0 is a simple structure, which switches its output high and low at uniform repeatable intervals. The PWM0D is the output duty cycle, and the output period is PWM0PRD+1. The output waveform of PWM0 is shown below.



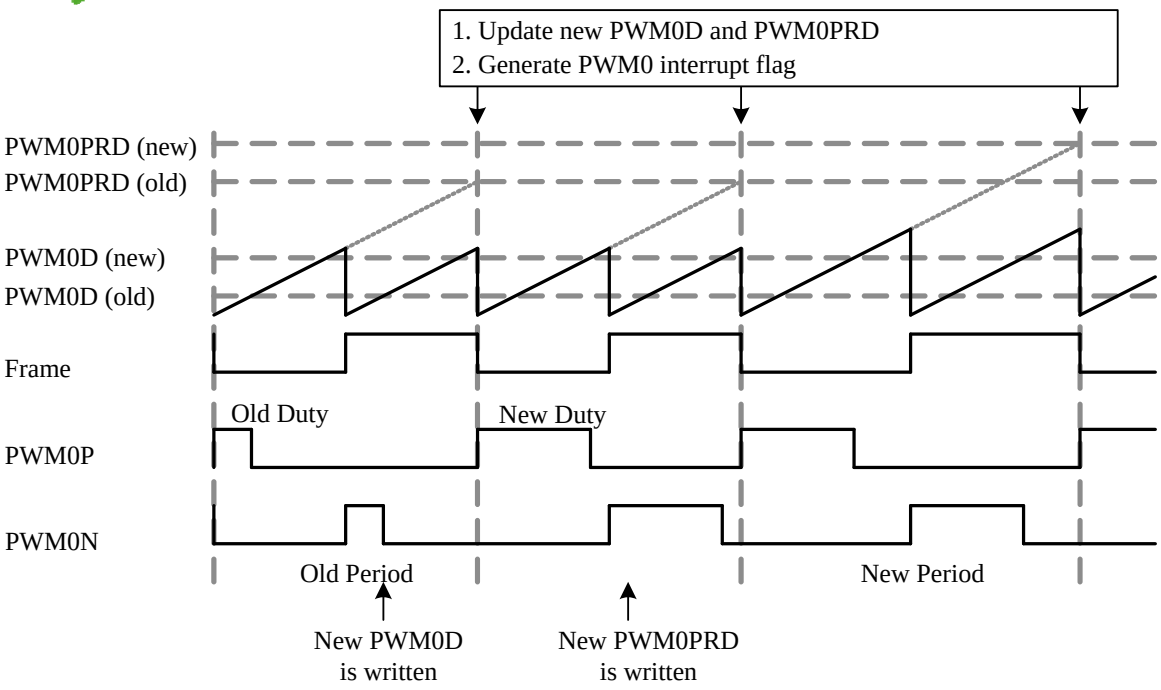
PWM0 normal mode output waveform (PWM0OM=0, PWM0DZ=0)



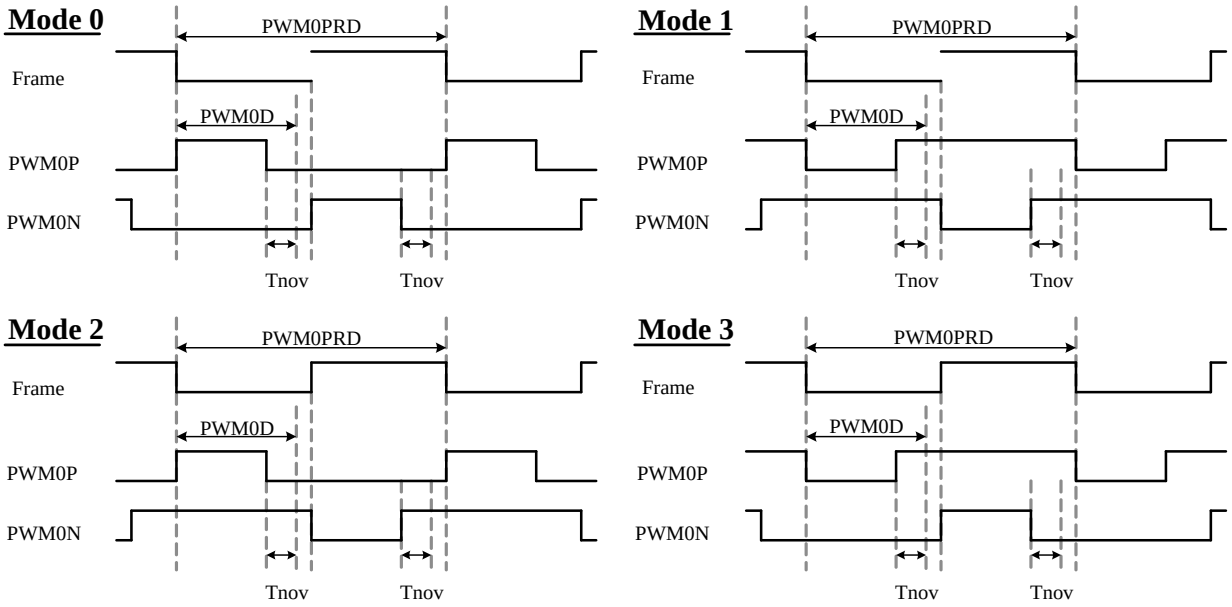
PWM0 normal mode output mode

Half-Bridge Mode

The half-bridge mode PWM is similar to the normal mode but Dead zone is prohibited in half-bridge mode (SFR PWM0DZ must be 0). It has two frames in a period, PWM0P only output in the first frame, PWM0N only output in the second frame. The width of these two frames must be same, so their width is the integer part of PWM0PRD/2. Because each output channel only output in one frame, the maximum duty cycle is same as the width of a frame. If the PWM0D is larger than PWM0PRD/2, H/W will force set the duty cycle to PWM0PRD/2. Following figure shows the output waveform and the output modes.



PWM0 half-bridge mode output waveform (PWM0OM=0, PWM0DZ=0)



PWM0 half-bridge mode output modes

10.2 PWM1 (PWM1, PWM2 and PWM3)

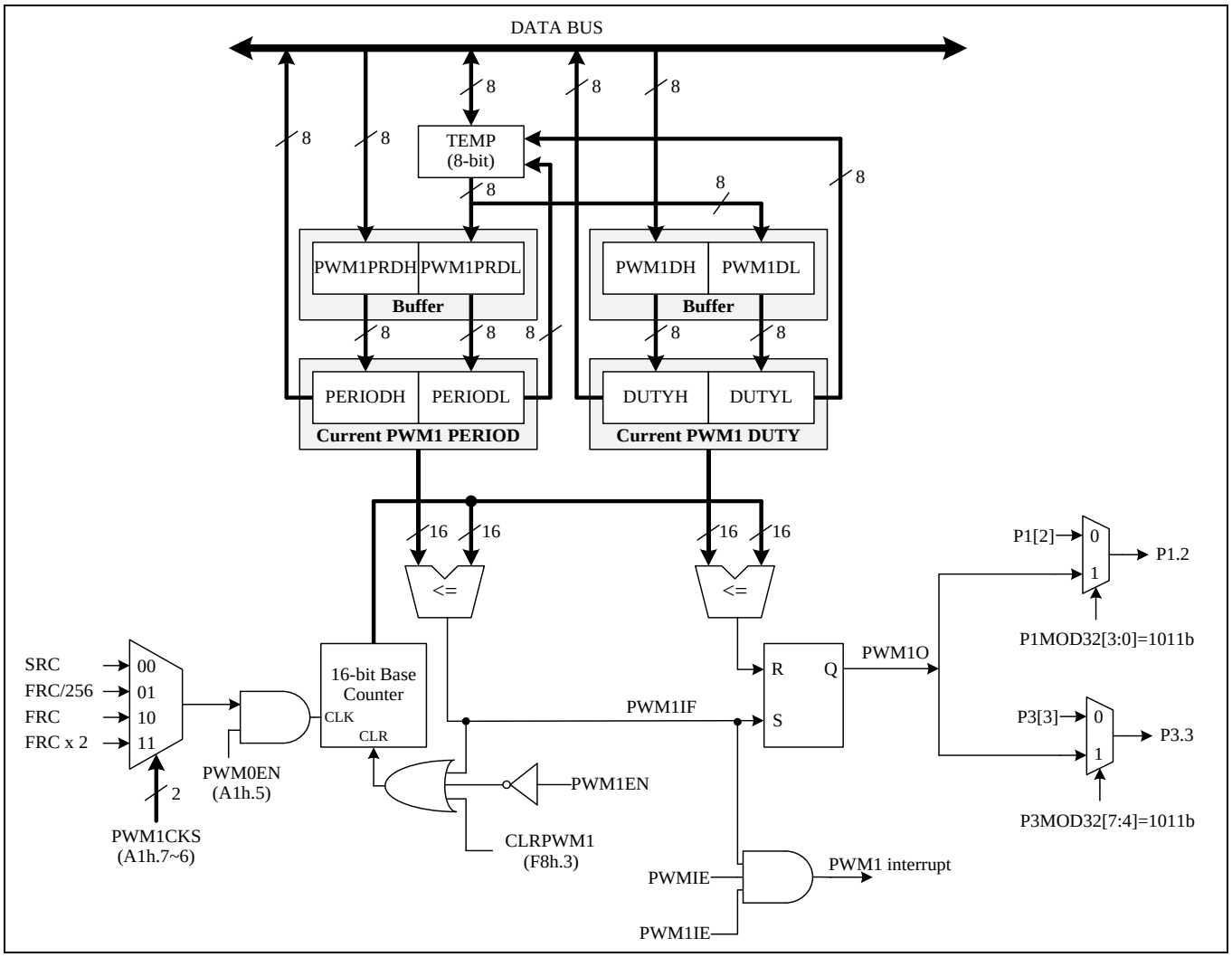
The 16-bit PWM1 module has three outputs PWM1/PWM2/PWM3 that share the same 16-bit period, but have independent duty cycles and no dead zone settings. When CLRPWM1 is set to 1, PWM1/PWM2/PWM3 will be cleared and held, otherwise PWM1/PWM2/PWM3 will remain running. PWM1/2/3 is based on the PWM1 clock. PWM1/2/3 can generate a changing frequency waveform with a duty cycle resolution of 65536 based on the PWM1 clock.

The following takes PWM1 as an example to illustrate the structure of PWM1 module. PWM1 duty cycle can be changed by writing to SFR PWM1DUTY. Whenever the 16-bit radix counter matches the 16-bit PWM1 duty cycle

register {PWM1DH, PWM1DL}, the PWM1 output signal is reset to low level. The period of PWM1 can be set by writing to SFR PWM1PRD. As soon as a PWM duty cycle or period register is written, the new value is saved to its own buffer. H/W will update these values at the end of the current cycle or when PWM1 is cleared. PWM1 has a corresponding interrupt flag, which will be generated at the end of the cycle.

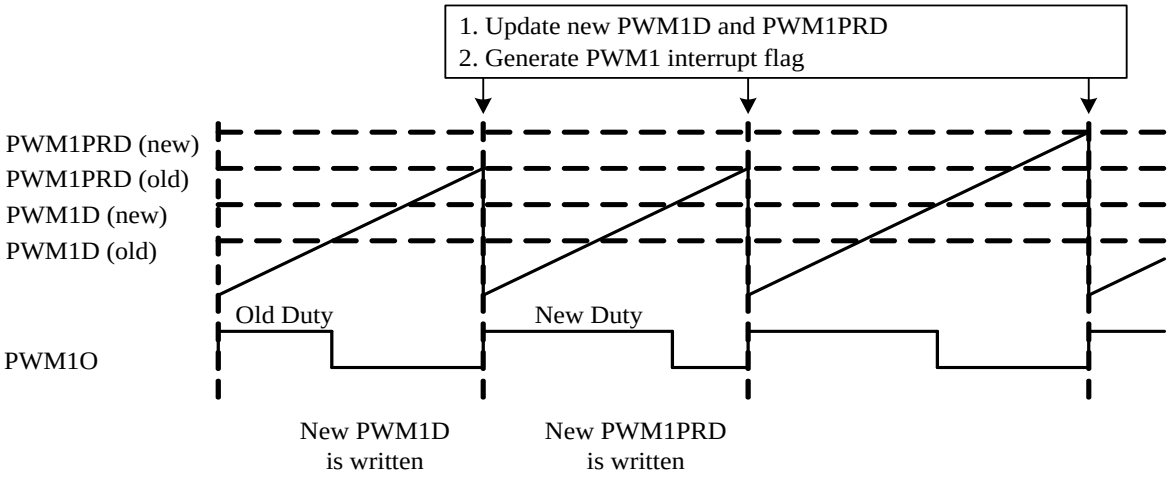
{PWM1DH, PWM1DL} or PWM1PRD are 16-bit operations. The program should avoid interrupts when writing and reading the high byte and low byte. If an interrupt occurs during reading and writing these 16-bit registers and these registers are read and written within the interrupt, it is easy to cause reading and writing errors. For reading and writing of 16-bit PWM period and duty cycle, it is recommended to update data only in the main program or only in interrupts to avoid possible errors.

The PWM1 structure is as follows



PWM1 structure

PWM1 is a simple structure that switches its output high and low at even repeatable intervals. PWM2/PWM3 have the same architecture as PWM1, sharing the PWM1 interrupt, clock source and period, but have their own independent duty cycles.



PWM1 output waveform

SFR **A9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE			EEPIE	ADIE	LVDIE	PCIE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

A9h.7 **PWMIE:** PWM0~1 Interrupt Enable
0: Disable PWM0～1 interrupt
1: Enable PWM0～1 interrupt

SFR **84h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE2	–	–	–	–	–	–	PWM1IE	PWM0IE
R/W	–	–	–	–	–	–	W	W
Reset	–	–	–	–	–	–	0	0

84h.6 **PWM1IE:** PWM1 Interrupt Enable
0: Disable
1: Enable

84h.5 **PWM0IE:** PWM0 Interrupt Enable
0: Disable
1: Enable

SFR **86h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTPWM	–	–	–	–	–	-	PWM1IF	PWM0IF
R/W	–	–	–	–	–	-	R/W	R/W
Reset	–	–	–	–	–	-	0	0

86h.1 **PWM1IF:** PWM1 interrupt flag
0: S/W write 0 to clear it
1: Set by H/W at the end of PWM1 period

86h.0 **PWM0IF:** PWM0 interrupt flag
0: write 0 to clear it
1: Set by H/W at the end of PWM1 period

SFR **A1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON	PWM1CKS		PWM1EN	PWM0EN	PWM0CKS		PWM0NMSK	PWM0PMSK
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

A1h.7~6 **PWM1CKS:** PWM1 clock source
00: SRC
01: FRC/256
10: FRC
11: FRC x 2 (V_{CC} > 3.0V)

A1h.5 **PWM1EN:** PWM1~3 enable
0: PWM1~3 disable
1: PWM1~3enable

A1h.4 **PWM0EN:** PWM0 enable
0: PWM0 disable
1: PWM0 enable

A1h.3~2 **PWM0CKS:** PWM0 clock source
00: SRC
01: FRC/256
10: FRC
11: FRC x 2 (V_{CC} > 3.0V)

A1h.1 **PWM0NMSK**: PWM0N mask data。If CLRPWM0=1 and PMW0MSKE=1, PWM0N will output this mask data.

A1h.0 **PWM0PMSK**: PWM0P mask data。If CLRPWM0=1 and PMW0MSKE=1, PWM0N will output this mask data.

SFR **A7h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCON2	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
R/W	R/W	R/W	R/W		R/W			
Reset	0	0	0	0	0	0	0	0

A7h.7 **PWM0MOD:** PWM0 mode select
0: normal mode
1: half-bridge mode

A7h.6 **PWM0MSKE:** mask output enable
0: disable
1: enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1

A7h.5~4 **PWM0OM:** PWM0 output mode select
00: Mode0
01: Mode1
10: Mode2
11: Mode3

A7h.3~0 **PWM0DZ:** PWM0 dead zone (Dead zone is prohibited in half-bridge mode)
0000: 0 x T_{PWMCLK}
0001: 1 x T_{PWMCLK}
...
1111: 15 x T_{PWMCLK}

SFR **D1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DH	PWM0DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D1h.7~0 **PWM0DH:** PWM0 duty high byte
write sequence: PWM0DL then PWM0DH
read sequence: PWM0DH then PWM0DL

SFR **D2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0DL	PWM0DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D2h.7~0 **PWM0DL:** PWM0 duty low byte
write sequence: PWM0DL then PWM0DH
read sequence: PWM0DH then PWM0DL

SFR **D3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DH	PWM1DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D3h.7~0 **PWM1DH:** PWM1 duty high byte
write sequence: PWM1DL then PWM1DH
read sequence: PWM1DH then PWM1DL

SFR **D4h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1DL	PWM1DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D4h.7~0 **PWM1DL:** PWM1 duty low byte
write sequence: PWM1DL then PWM1DH
read sequence: PWM1DH then PWM1DL

SFR **D5h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DH	PWM2DH							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

D5h.7~0 **PWM2DH:** PWM2 duty high byte
write sequence: PWM2DL then PWM2DH
read sequence: PWM2DH then PWM2DL

SFR **D6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM2DL	PWM2DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

D6h.7~0 **PWM2DL:** PWM2 duty low byte
write sequence: PWM2DL then PWM2DH
read sequence: PWM2DH then PWM2DL

SFR **D9h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDH	PWM0PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

D9h.7~0 **PWM0PRDH:** PWM0 period high byte
write sequence: PWM0PRDL then PWM0PRDH
read sequence: PWM0PRDH then PWM0PRDL

SFR **DAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRDL	PWM0PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DAh.7~0 **PWM0PRDL:** PWM0 period low byte
write sequence: PWM0PRDL then PWM0PRDH
read sequence: PWM0PRDH then PWM0PRDL

SFR **DBh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDH	PWM1PRDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DBh.7~0 **PWM1PRDH:** PWM1 period high byte
write sequence: PWM1PRDL then PWM1PRDH
read sequence: PWM1PRDH then PWM1PRDL

SFR **DCh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRDL	PWM1PRDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

DCh.7~0 **PWM1PRDL:** PWM1 period low byte
write sequence: PWM1PRDL then PWM1PRDH
read sequence: PWM1PRDH then PWM1PRDL

SFR **DDh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DH	PWM3DH							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DDh.7~0 **PWM3DH:** PWM3 duty high byte
write sequence: PWM3DL then PWM3DH
read sequence: PWM3DH then PWM3DL

SFR **DEh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM3DL	PWM3DL							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

DEh.7~0 **PWM3DL:** PWM3 duty low byte
write sequence: PWM3DL then PWM3DH
read sequence: PWM3DH then PWM3DL

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD10	P1MOD1				P1MOD0			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

91h.7~4 **P1MOD1:** P1.1 pin control
0000~1111: Set 1011 to output PWM0P to P1.1; see Table 7.1

91h.3~0 **P1MOD0:** P1.0 pin control
0000~1111: Set 1011 to output PWM0N to P1.0; see Table 7.1

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD32	P1MOD3				P1MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

92h.7~4 **P1MOD3:** P1.3 pin control
0000~1111: Set 1011 to output PWM2 to P1.3; see Table 7.1

92h.3~0 **P1MOD2:** P1.2 pin control
0000~1111: Set 1011 to output PWM1 to P1.2; see Table 7.1

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD54	P1MOD5				P1MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ah.7~4 **P1MOD5:** P1.5 pin control
0000~1111: see Table 7.1

9Ah.3~0 **P1MOD4:** P1.4 pin control
0000~1111: Set 1011 to output PWM3 to P1.4; see Table 7.1

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD32	P3MOD3				P3MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ch.7~4 **P3MOD3:** P3.3 pin control
0000~1111: Set 1011 to output PWM1 to P3.3; see Table 7.1

9Ch.3~0 **P3MOD2:** P3.2 pin control
0000~1111: Set 1011 to output PWM0N to P3.2; see Table 7.1

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD54	P3MOD5				P3MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Dh.7~4 **P3MOD5:** P3.5 pin control
0000~1111: Ssee Table 7.1

9Dh.3~0 **P3MOD4:** P3.4 pin control
0000~1111: Set 1011 to output PWM2 to P3.4; see Table 7.1

SFR **9Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD76	P3MOD7				P3MOD6			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Eh.7~4 **P3MOD7:** P3.7 pin control
0000~1111: Set 1011 to output PWM3 to P3.7; see Table 7.1

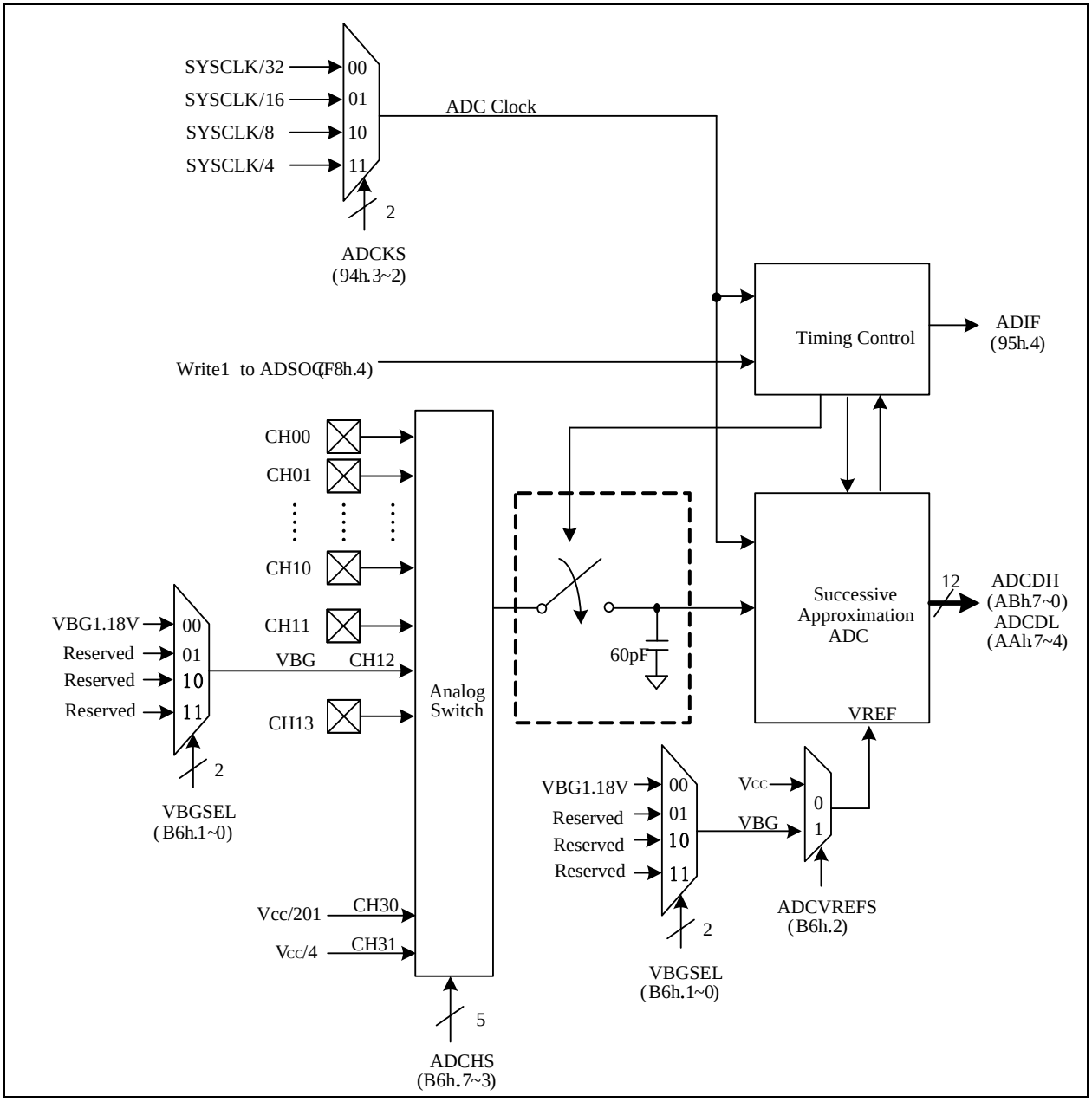
9Eh.3~0 **P3MOD6:** P3.6 pin control
0000~1111: Set 1011 to output PWM0P to P1.6; see Table 7.1

11. ADC

The Chip offers a 12-bit ADC consisting of a 13-channel analog input multiplexer, control register, clock generator, 12-bit successive approximation register, and output data register.

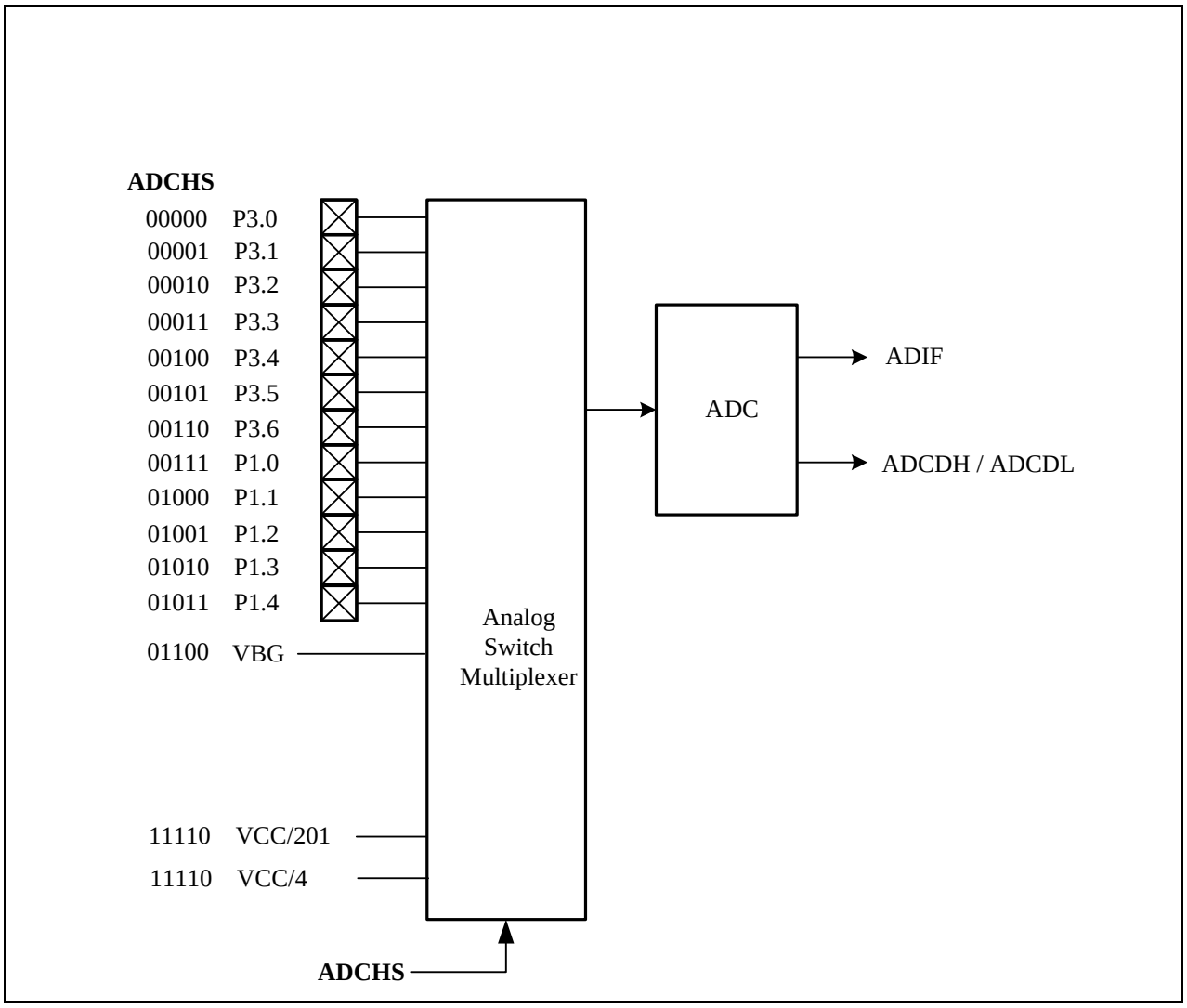
To use the ADC, set the ADCKS bit first to choose a proper ADC clock frequency, which must be less than 1 MHz. Then, launch the ADC conversion by setting the ADSOC bit, and H/W will automatic clear it at the end of the conversion. After the end of the conversion, H/W will set the ADIF bit and generate an interrupt if an ADC interrupt is enabled. The ADIF bit can be cleared by writing 0 to this bit or 1 to the ADSOC bit.

Using the ADCVREFS option, the ADC internal reference voltage source (VREF) can be selected to be VCC or VBG1.18V. When ADCVREFS=1, set VBGSEL=00 to select VBG as 1.18V or 2.0V or 2.5V or 3.0V



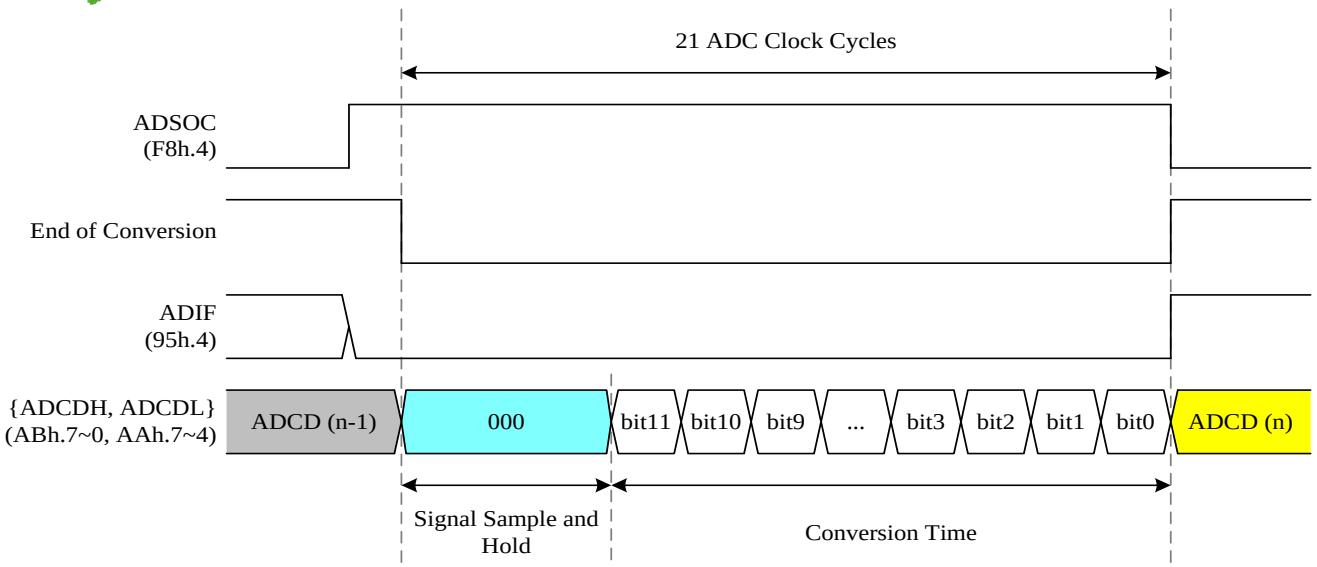
11.1 ADC Channels

The ADC channels are connected to the analog input pins through analog switch multiplexers. The analog switch multiplexer is controlled by the ADCHS register. The chip provides up to 13 IO input pins. In addition, there are 4 internal reference voltages (VBG, VSS, VCC/4, VCC/201). When ADCHS is set to 01100b, the analog input will be connected to VBG. When ADCHS is set to 01001b, the analog input will be connected to the P1.2 input pin. At this time, P1.2 must also be set to ADC channel mode, such as P1MOD32 lower 4 bits are set to 0011.



11.2 ADC Conversion Time

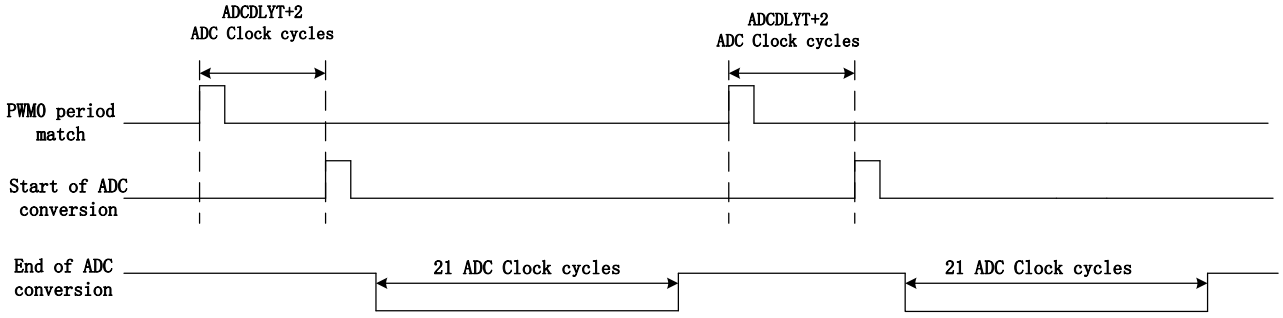
The conversion time is the time required for the ADC to convert the voltage. A total of 21 ADC clock cycles are required to perform the complete conversion. When the conversion time is complete, the ADIF interrupt flag is set by H/W, and the result is loaded into the ADCDH and ADCDL registers of the 12-bit A/D result.



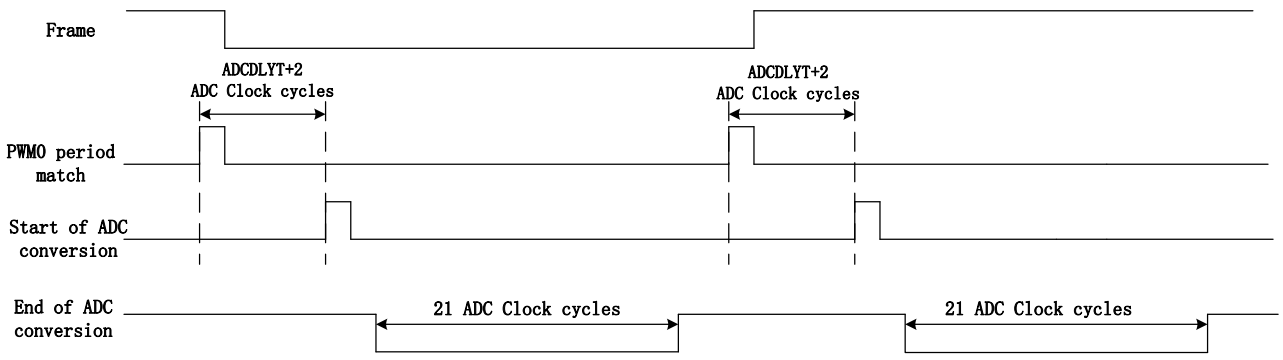
11.3 PWM0 Trigger ADC

The mechanism of PWM triggering ADC can be enabled by setting the non-zero ADCDLY register. When the PWM0 counter matches the period register, if the PWM triggering ADC mechanism is turned on, the hardware will automatically start the ADC conversion after a certain delay time.

11.3.1 PWM0 normal mode trigger ADC

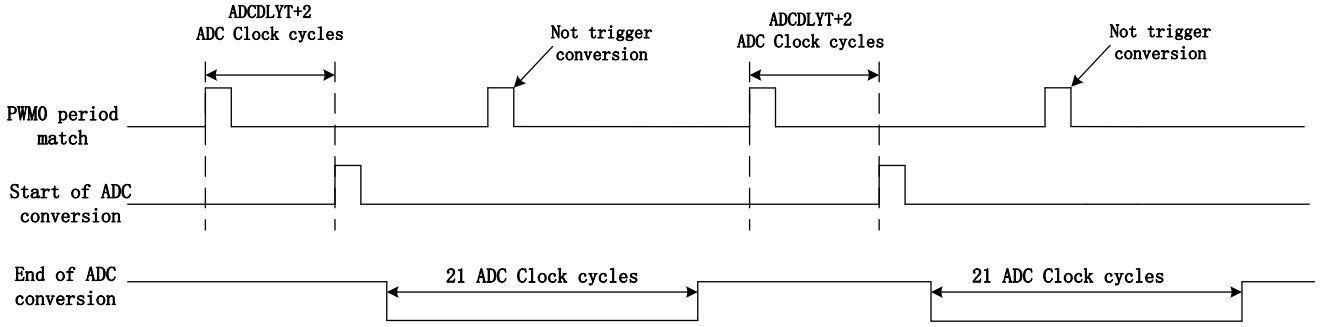


11.3.2 PWM0 half-bridge mode trigger ADC



11.3.3 Unconverted Situation

When the ADC conversion is in progress, the PWM0 period match will not trigger a new ADC conversion.



SFR A9h	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTE1	PWMIE			EEPIE	ADIE	LVDIE	PCIE	TM3IE
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset	0			0	0	0	0	0

A9h.3 **ADIE:** ADC Interrupt enable
0: disable ADC interrupt
1: enable ADC interrupt

SFR **94h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OPTION	–	TM3CKS	WDTPSC		ADCKS		–	–
R/W	–	R/W	R/W		R/W		–	–
Reset	–	0	0	0	–	–	0	0

94h.3~2 **ADCKS:** ADC clock rate select
00: F_{SYSCLK}/32
01: F_{SYSCLK}/16
10: F_{SYSCLK}/8
11: F_{SYSCLK}/4

SFR **95h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTFLG	LVDIF	EEPIF	EEPBUSY	ADIF	–	–	PCIF	TF3
R/W	R/W	R/W	R	R/W	–	–	R/W	R/W
Reset	0	0	0	0	–	–	0	0

95h.4 **ADIF:** ADC interrupt flag
Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

Note: *S/W can write 0 to clear a flag in the INTFLG, but writing 1 has no effect.*

SFR **AAh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDL	ADCDL				–	–	–	–
R/W	R				–	–	–	–
Reset	–	–	–	–	–	–	–	–

AAh.7~4 **ADCDL:** ADC data bit 3~0

SFR **ABh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDH	ADCDH							
R/W	R							
Reset	–	–	–	–	–	–	–	–

ABh.7~0 **ADCDH:** ADC data bit 11~4

SFR **B6h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCHSEL	ADCHS					ADCVREFS	VBGSEL	
R/W	R/W					R/W	R/W	
Reset				1	1	0	0	0

B6h.4~0 **ADCHS:** ADC channel select

00000: CH0（P3.0）
00001: CH1（P3.1）
00010: CH2（P3.2）
00011: CH3（P3.3）
00100: CH4（P3.4）
00101: CH5（P3.5）
00110: CH6（P3.6）
00111: CH7（P1.0）
01000: CH8（P1.1）
01001: CH9（P1.2）
01010: CH10（P1.3）
01011: CH11（P1.4）
01100: CH12 VBG（bang gap voltage）
others: reserved
11110: VCC/201
11111: VCC/4

B6h.2 **ADCVREFS:** ADC reference voltage select

0: VCC
1: VBG

B6h.1~0 **VBGSEL:** VBG voltage select

00: 1.18V
01: Reserved
10: Reserved
11: Reserved

SFR **F8h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AUX1	CLRWDT	CLRTM3	CLRPWM0	ADSOC	CLRPWM1	T0SEL	T1SEL	DPSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	1/0	1	0	0	0

F8h.4 **ADSOC:** Start ADC conversion

W: Set the ADSOC bit to start ADC conversion, and the ADSOC bit will be cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
R: Read ADEOC signal

SFR **ACh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADCDLYT	ADCDLYT							
R/W	R/W							
Reset	0	0	0	0	0	0	0	0

ACh.7~0 **ADCDLYT:** The delay time between PWM period match and ADC start

8'h00: disable PWM0 trigger ADC start
8'h01~8'hFF: enable and delay time((ADCDLT[7:0]+2)/Fadc) to ADC start

SFR **91h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD10	P1MOD1				P1MOD0			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

91h.7~4 **P1MOD1:** P1.1pin control

0000~1111: see table 7.1

91h.3~0 **PINMOD0:** P1.0 pin control

0000~1111: see table 7.1

SFR **92h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD32	P1MOD3				P1MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

92h.7~4 **P1MOD3:** P1.3 pin control

0000~1111: see table 7.1

92h.3~0 **P1MOD2:** P1.2 pin control

0000~1111: see table 7.1

SFR **9Ah**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P1MOD54	P1MOD5				P1MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ah.7~4 **P1MOD5:** P1.5 pin control
0000~1111: see table 7.1

9Ah.3~0 **P1MOD4:** P1.4 pin control
0000~1111: see table 7.1

SFR **9Bh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD10	P3MOD1				P3MOD0			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Bh.7~4 **P3MOD1:** P3.1 pin control
0000~1111: see table 7.1

9Bh.3~0 **P3MOD0:** P3.0 pin control
0000~1111: see table 7.1

SFR **9Ch**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD32	P3MOD3				P3MOD2			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Ch.7~4 **P3MOD3:** P3.3 pin control
0000~1111: see table 7.1

9Ch.3~0 **P3MOD2:** P3.2 pin control
0000~1111: see table 7.1

SFR **9Dh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD54	P3MOD5				P3MOD4			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Dh.7~4 **P3MOD5:** P3.5 pin control
0000~1111: see table 7.1

9Dh.3~0 **P3MOD4:** P3.4 pin control
0000~1111: see table 7.1

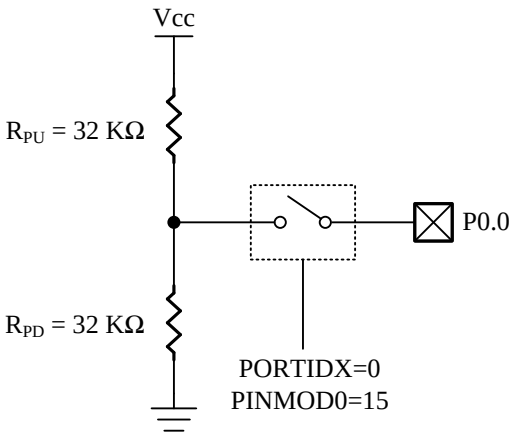
SFR **9Eh**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
P3MOD76	P3MOD7				P3MOD6			
R/W	R/W				R/W			
Reset	0	0	0	1	0	0	0	1

9Eh.7~4 **P3MOD7:** P3.7 pin control
0000~1111: see table 7.1

9Eh.3~0 **P3MOD6:** P3.6 pin control
0000~1111: see table 7.1

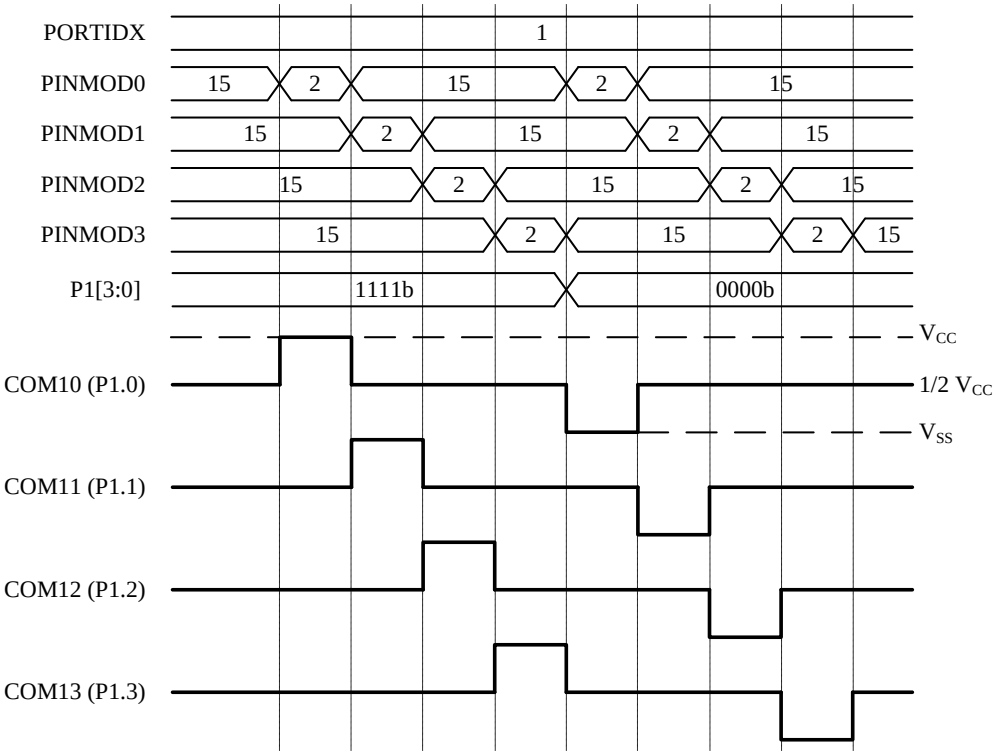
12. S/W Controller LCD Driver

TM52E5223 supports an S/W controlled method to driving LCD. All of the IO pins can be the Common pins. User can flexibly adjust the Common pins and Segment pins. It is capable of driving the LCD panel with 49 dots (Max.) by 7 Commons (COM) and 7 Segments (SEG). The P0.0~P0.5 are used for Common pins COM00~COM07. The P1.0~P1.5 are used for Common pins COM10~COM15. The P3.0~P3.7 are used for Common pins COM30~COM37. Common pins are capable of driving 1/2 bias by setting the corresponding PINMODE=15 (***see section 7***). Refer to the following figures.



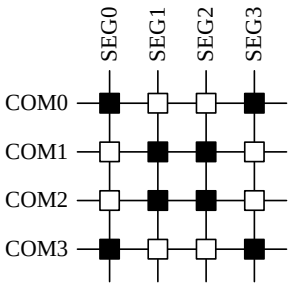
LCD COM00 Circuit

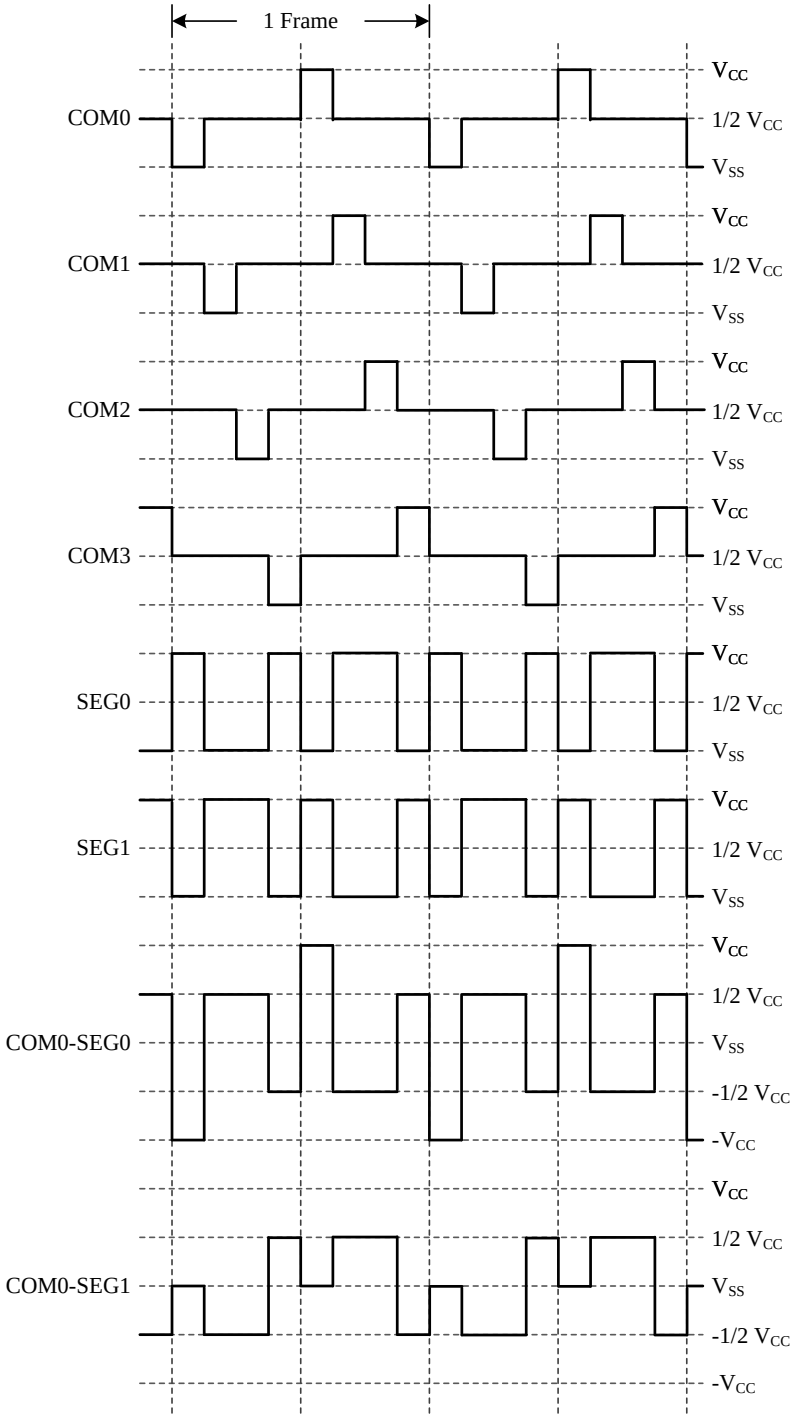
The frequency of any repeating waveform output on the COM pin can be used to represent the LCD frame rate. The figure below shows an LCD frame.



S/W Controlled LCD COM00~03 Scanning

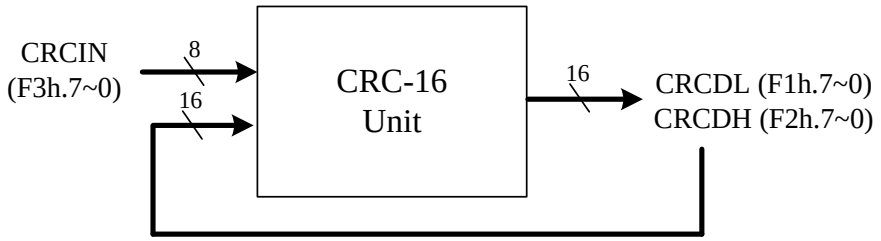
1/4 Duty, 1/2 Bias Output Waveform





13. Cyclic Redundancy Check (CRC)

The chip supports an integrated 16-bit Cyclic Redundancy Check function. The Cyclic Redundancy Check (CRC) calculation unit is an error detection technique test algorithm and uses to verify data transmission or storage data correctness. The CRC calculation takes an 8-bit data stream or a block of data as input and generates a 16-bit output remainder. The data stream is calculated by the same generator polynomial.



CRC Block Diagram

The CRC generator provides the 16-bit CRC result calculation based on the CRC-16-IBM polynomial. In this CRC generator, there are only one polynomial available for the numeric values calculation. It can't support the 16-bit CRC calculations based on any other polynomials. Each write operation to the CRCIN register creates a combination of the previous CRC value stored in the CRCDH and CRCDL registers. It will take one MCU instruction cycle to calculate.

CRC-16-IBM (Modbus) Polynomial representation: $X^{16} + X^{15} + X^2 + 1$

SFR **F1h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDL	CRCDL							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F1h.7~0 **CRCDL:** 16-bit CRC checksum data bit 7~0

SFR **F2h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCDH	CRCDH							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

F2h.7~0 **CRCDL:** 16-bit CRC checksum data bit 15~8

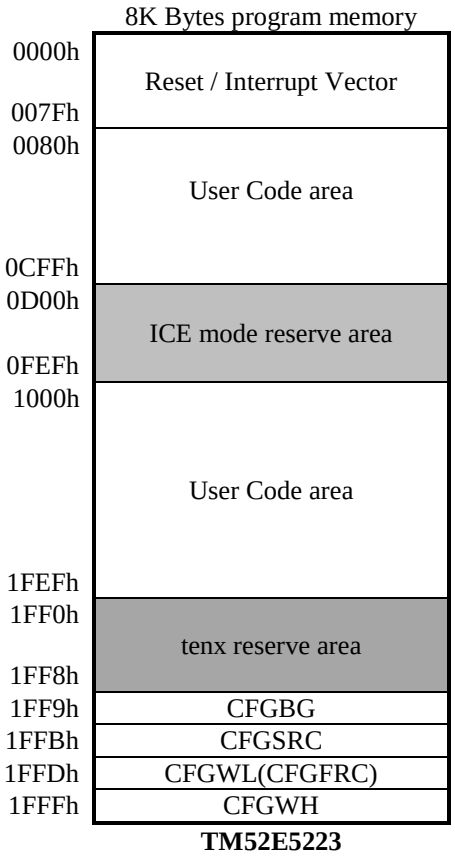
SFR **F3h**	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CRCIN	CRCIN							
W	W							
Reset	–	–	–	–	–	–	–	–

F3h.7~0 **CRCIN:** CRC input data register

14. In Circuit Emulation (ICE) Mode

This device can support the In Circuit Emulation Mode. To use the ICE Mode, user just needs to connect P3.0 and P3.1 pin to the tenx proprietary EV Module. The benefit is that user can emulate the whole system without changing the on board target device. But there are some limits for the ICE mode as below.

1. The device must be un-protect.。
2. The device's P3.0 and P3.1 pins must work in input Mode。
3. The Program Memory's addressing space D00h~FFFh 和 0033h~003Ah are occupied by tenx EV module. So user Program cannot access these spaces
4. The HT-Link communication pin's function cannot be emulated.
5. The V_{DD} level is controlled by HT-Link module。



TM52E5223

SFR & CFGW MAP

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
80h	0000-0000	**P0**	–	–	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
81h	0000-0111	**SP**	SP							
82h	0000-0000	**DPL**	DPL							
83h	0000-0000	**DPH**	DPH							
84h	xxxx-xx00	**INTE2**	–	–	–	–	–	–	PWM1IE	PWM0IE
86h	xxxx-x000	**INTPWM**	–	–	–	–	–	–	PWM1IF	PWM0IF
87h	0xxx-0000	**PCON**	SMOD	–	–	–	GF1	GF0	PD	IDL
88h	0000-0000	**TCON**	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
89h	0000-0000	**TMOD**	GATE1	CT1N	TMOD1		GATE0	CT0N	TMOD0	
8Ah	0000-0000	**TL0**	TL0							
8Bh	0000-0000	**TL1**	TL1							
8Ch	0000-0000	**TH0**	TH0							
8Dh	0000-0000	**TH1**	TH1							
90h	1111-1111	**P1**			P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
91h	0001-0001	**P1MOD10**	P1MOD1				P1MOD0			
92h	0001-0001	**P1MOD32**	P1MOD3				P1MOD2			
93h	0000-0000	**UARTCON**	–					UARTPS		
94h	0000-0000	**OPTION**	–	TM3CKS	WDTPSC		ADCKS		–	–
95h	0000-xx00	**INTFLG**	LVDIF	EEPIF	EEPBUSY	ADIF	–	–	PCIF	TF3
96h										
97h	xxxx-xx00	**SWCMD**	SWRST / WDTO							
98h	0000-0000	**SCON**	SM0	SM1	SM2	REN	TB8	RB8	TI	RI
99h	xxxx-xxxx	**SBUF**	SBUF							
9Ah	0001-0001	**P1MOD54**	P1MOD5				P1MOD4			
9Bh	0001-0001	**P3MOD10**	P3MOD1				P3MOD0			
9Ch	0001-0001	**P3MOD32**	P3MOD3				P3MOD2			
9Dh	0001-0001	**P3MOD54**	P3MOD5				P3MOD4			
9Eh	0001-0001	**P3MOD76**	P3MOD7				P3MOD6			
9Fh	0000-0000	**UARTBRP**	UARTBRP							
A1h	xx10-1010	**PWMCON**	PWM1CKS		PWM1EN	PWM0EN	PWM0CKS		PWM0NMSK	PWM0PMSK
A7h	0000-0000	**PWMCON2**	PWM0MOD	PWM0MSKE	PWM0OM		PWM0DZ			
A8h	0x00-0000	**IE**	EA	–		ES	ET1	EX1	ET0	EX0
A9h	0000-0000	**INTE1**	PWMIE	–	–	EEPIE	ADIE	LVDIE	PCIE	TM3IE
AAh	xxxx-xxxx	**ADCDL**	ADCDL				–			
ABh	xxxx-xxxx	**ADCDH**	ADCDH							
ACh	0000-0000	**ADCDLYT**	ADCDLYT							
B0h	1111-1111	**P3**	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0
B6h	xxx1-1111	**ADCHSEL**	ADCHS					ADCVREFS	VBGSEL	
B8h	xx00-0000	**IP**	–	–	–	PS	PT1	PX1	PT0	PX0
B9h	xx00-0000	**IPH**	–	–	–	PSH	PT1H	PX1H	PT0H	PX0H
BAh	000x-0000	**IP1**	PPWM	–	–	PEEP	PADI	PLVD	PPC	PT3
BBh	000x-0000	**IP1H**	PPWMH	–	–	PEEPH	PADIH	PLVDH	PPCH	PT3H
BFh	000x-0000	**LVDS**	LVDM	LVDO	LVDHYS	LVDPD	LVDSEL			
C9h	0000-0000	**EEPCON**	EEPWE / EEPTO							
D0h	0000-0000	**PSW**	CY	AC	F0	RS1	RS0	OV	F1	P
D1h	0000-0000	**PWM0DH**	PWM0DH							
D2h	0000-0000	**PWM0DL**	PWM0DL							
D3h	0000-0000	**PWM1DH**	PWM1DH							

Adr	RST	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D4h	0000-0000	**PWM1DL**	PWM1DL							
D5h	0000-0000	**PWM2DH**	PWM2DH							
D6h	0000-0000	**PWM2DL**	PWM2DL							
D7h	0000-0000	**FRCFT**	–	–	–	FRCFT				
D8h	00x0-0011	**CLKCON**	–	–	STPSCK	STPPCK	STPFCK	SELFCK	CLKPSC	
D9h	1111-1111	**PWM0PRDH**	PWM0PRDH							
DAh	1111-1111	**PWM0PRDL**	PWM0PRDL							
DBh	1111-1111	**PWM1PRDH**	PWM1PRDH							
DCh	1111-1111	**PWM1PRDL**	PWM1PRDL							
DDh	0000-0000	**PWM3DH**	PWM3DH							
DEh	0000-0000	**PWM3DL**	PWM3DL							
DFh	0000-0101	**RDCTL**	–	–	–	–	–	ATDEN	ATDT	
E0h	0000-0000	**ACC**	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0
E3h	x100-0000	**LVRCON**	–	–	–	LVRPD	LVRSEL			
E5h	0000-0x00	**EFTCON**	EFT2CS	EFT1CS	EFT1S		EFTSLOW	–	EFTWOUT	CKHLDE
EAh	xxxx-xxxx	**CFGSRC**	–	–	–	SRCTRIM				
EFh	xx00-0000	**AUX3**	warmtime	TM3PSC			–	IOVIS	–	–
F0h	0000-0000	**B**	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0
F1h	1111-1111	**CRCDL**	CRCDL							
F2h	1111-1111	**CRCDH**	CRCDH							
F3h	0000-0000	**CRCIN**	CRCIN							
F5h	xxxx-xxxx	**CFGBG**	–	–	–	BGTRIM1				
F6h	xxxx-xxxx	**CFGWL**	–	FRCTRIM						
F7h	0000-0110	**AUX2**	WDTE		PWRSAV	VBGOUT		EEPTE		
F8h	0010-1000	**AUX1**	CLRWDT	CLRTM3	CLRPWM0	ADSOC	CLRPWM1	T0SEL	T1SEL	DPSEL

Flash Address	NAME	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1FF9h	**CFGBG**	–	–	–	BGTRIM1				
1FFBh	**CFGSRC**	–	–	–	SRCTRIM				
1FFDh	**CFGWL**	–	FTCTRIM						
1FFFh	**CFGWH**	PROT	XRSTE	PORSEL	–	–	–	–	–

SFR & CFGW DESSRIPTION

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
81h	**SP**	7~0	SP	R/W	07h	Stack Point
82h	**DPL**	7~0	DPL	R/W	00h	Data Point low byte
83h	**DPH**	7~0	DPH	R/W	00h	Data Point high byte
84h	**INTE2**	1	PWM1IE	R/W	0	PWM1 Interrupt Enable 0: disable PWM1 ~ PWM3 interrupt 1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)
		0	PWM0IE	W	0	PWM0 Interrupt Enable 0: disable PWM0 interrupt 1: enable (note: PWMIE must be 1 at the same time to generate PWM interrupt)
86h	**INTPWM**	1	PWM1IF	W	0	PWM1~PWM3 interrupt Flag. Set by H/W at the end of PWM1 period, S/Wwrite 1h to clear int flag
		0	PWM0IF	R/W	0	PWM0 Interrupt Flag. Set by H/W at the end of PWM0 period, S/Wwrite 2h to clear int flag
87h	**PCON**	7	SMOD	R/W	0	Set 1 to enable UART double baud rate
		3	GF1	R/W	0	General purpose flag bit
		2	GF0	R/W	0	General purpose flag bit
		1	PD	R/W	0	Power down control bit, set 1 to enter Halt/Stop mode
		0	IDL	R/W	0	Idle control bit, set 1 to enter Idle mode
88h	**TCON**	7	TF1	R/W	0	Timer1 overflow flag Set by H/W when Timer/Counter 1 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		6	TR1	R/W	0	Timer1 run control. 1: timer runs; 0: timer stops
		5	TF0	R/W	0	Timer0 overflow flag Set by H/W when Timer/Counter 0 overflows. Cleared by H/W when CPU vectors into the interrupt service routine.
		4	TR0	R/W	0	Timer0 run control. 1:timer runs; 0:timer stops
		3	IE1	R/W	0	External Interrupt 1 (INT1 pin) edge flag Set by H/W when an INT1 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		2	IT1	R/W	0	External Interrupt 1 control bit 0: Low level active (level triggered) for INT1 pin 1: Falling edge active (edge triggered) for INT1 pin
		1	IE0	R/W	0	External Interrupt 0 (INT0 pin) edge flag Set by H/W when an INT0 pin falling edge is detected. Cleared by H/W when CPU vectors into the interrupt service routine.
		0	IT0	R/W	0	External Interrupt 0 control bit 0: Low level active (level triggered) for INT0 pin 1: Falling edge active (edge triggered) for INT0 pin
89h	**TMOD**	7	GATE1	R/W	0	Timer1 gating control bit 0: Timer1 enable when TR1 bit is set 1: Timer1 enable only while the INT1 pin is high and TR1 bit is set
		6	CT1N	R/W	0	Timer1 Counter/Timer select bit 0: Timer mode, Timer1 data increases at 2 System clock cycle rate 1: Counter mode, Timer1 data increases at T1 pin's negative edge
		5~4	TMOD1	R/W	00	Timer1 mode select 00: 8-bit timer/counter (TH1) and 5-bit prescaler (TL1) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL1). Reloaded from TH1 at overflow. 11: Timer1 stops
		3	GATE0	R/W	0	Timer0 gating control bit 0: Timer0 enable when TR0 bit is set 1: Timer0 enable only while the INT0 pin is high and TR0 bit is set

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		2	CT0N	R/W	0	Timer0 Counter/Timer select bit 0: Timer mode, Timer0 data increases at 2 System clock cycle rate 1: Counter mode, Timer0 data increases at T0 pin's negative edge
		1~0	TMOD0	R/W	00	Timer0 mode select 00: 8-bit timer/counter (TH0) and 5-bit prescaler (TL0) 01: 16-bit timer/counter 10: 8-bit auto-reload timer/counter (TL0). Reloaded from TH0 at overflow. 11: TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer/counter using Timer1's TR1 and TF1 bits.
8Ah	**TL0**	7~0	TL0	R/W	00h	Timer0 data low byte
8Bh	**TL1**	7~0	TL1	R/W	00h	Timer1 data low byte
8Ch	**TH0**	7~0	TH0	R/W	00h	Timer0 data high byte
8Dh	**TH1**	7~0	TH1	R/W	00h	Timer1 data high byte
90h	**P1**	7~0	P1	R/W	FFh	Port1 data
91h	**P1MOD10**	7~4	P1MOD1	R/W	0001	P1.1 Pin Control 0000~1111: see table 7.1
		3~0	P1MOD0	R/W	0001	P1.0 Pin Control 0000~1111: see table 7.1
92h	**P1MOD32**	7~4	P1MOD3	R/W	0001	P1.3 Pin Control 0000~1111: see table 7.1
		3~0	P1MOD2	R/W	0001	P1.2 Pin Control 0000~1111: see table 7.1
93h	**UARTCON**	2~0	UARTPS	R/W	000	UART Pin Select 000: RXD/TXD = P3.0/P3.1 001: RXD/TXD = P3.2/P3.3 010: RXD/TXD = P3.1/P3.0 011: RXD/TXD = P3.3/P3.2 100: RXD/TXD = P3.1/P3.1; 1-wire 101: RXD/TXD = P3.3/P3.3; 1-wire 110: RXD/TXD = P3.0/P3.0; 1-wire 111: RXD/TXD = P3.2/P3.2; 1-wire
94h	**OPTION**	6	TM3CKS	R/W	0	Timer3 Clock Source Select. 0: Slow clock/4 (SRC/4 32KHz) 1: FRC/512 (32KHz)
		5~4	WDTPSC	R/W	00	Watchdog Timer pre-scalar time select 00: 480 ms WDT overflow rate 01: 240 ms WDT overflow rate 10: 124 ms WDT overflow rate 11: 60 ms WDT overflow rate
		3~2	ADCKS	R/W	00	ADC clock rate select 00: F_{SYSCLK}/32 01: F_{SYSCLK}/16 10: F_{SYSCLK}/8 11: F_{SYSCLK}/4
95h	**INTFLG**	7	LVDIF	R	0	Low Voltage Detect flag Set by H/W when a low voltage occurs.
		6	EEPIF	R/W	0	EEP write finish interrupt Set by H/W when write EEP finish, S/W can write 0 to clear it
		5	EEPBUSY	R	0	EEP Busy Flag is set high when write EEP
		4	ADIF	R/W	0	ADC interrupt flag Set by H/W at the end of ADC conversion. S/W writes EFh to INTFLG or sets the ADSOC bit to clear this flag.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		1	PCIF	R/W	0	Port1/Port3 Pin change interrupt flag Set by H/W when Port1/Port3 pin state change is detected and its interrupt enable bit is set. It is cleared automatically when the program performs the interrupt service routine. S/W can write 0 to clear all pin interrupt flags (Port1/Port3), it will also clear PIN0IF~PIN7IF and P1IF/P3IF.
		0	TF3	R/W	0	Timer3 Interrupt Flag Set by H/W when Timer3 reaches TM3PSC setting cycles. It is cleared automatically when the program performs the interrupt service routine. S/W can write FEh to INTFLG to clear this bit.
97h	**SWCMD**	7~0	SWRST	W		Write 56h to generate S/W Reset
		1	WDTO	R	0	WatchDog Time-Out flag
98h	**SCON**	7	SM0	R/W	0	UART Serial port mode select bit 0, 1 (SM0, SM1) = 00: Mode0: Not Support 01: Mode1: 8 bit UART, Baud Rate is Fsys/16/UARTBRP 10: Mode2: Not Support 11: Mode3: 9 bit UART, Baud Rate is Fsys/16/UARTBRP
		6	SM1	R/W	0	
		5	SM2	R/W	0	Serial port mode select bit 2 SM2 enables multiprocessor communication over a single serial line and modifies the above as follows. In Modes 2 & 3, if SM2 is set then the received interrupt will not be generated if the received ninth data bit is 0. In Mode 1, the received interrupt will not be generated unless a valid stop bit is received. In Mode 0, SM2 should be 0.
		4	REN	R/W	0	Set 1 to enable UART Reception
		3	TB8	R/W	0	Transmitter bit 8, ninth bit to transmit in Modes 2 and 3
		2	RB8	R/W	0	Receive Bit 8, contains the ninth bit that was received in Mode 2 and 3 or the stop bit is Mode 1 if SM2=0
		1	TI	R/W	0	Transmit Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the beginning of the stop bit in other modes. Must be cleared by S/W
		0	RI	R/W	0	Receive Interrupt flag Set by H/W at the end of the eighth bit in Mode 0, or at the sampling point of the stop bit in other modes. Must be cleared by S/W.
99h	**SBUF**	7~0	SBUF	R/W	–	UART transmit and receive data. Transmit data is written to this location and receive data is read from this location, but the paths are independent.
9Ah	**P1MOD54**	7~4	P1MOD5	R/W	0001	P1.5 Pin Control 0000~1111: see table 7.1
		3~0	P1MOD4	R/W	0001	P1.4 Pin Control 0000~1111: see table 7.1
9Bh	**P3MOD10**	7~4	P3MOD1	R/W	0001	P3.1 Pin Control 0000~1111: see table 7.1
		3~0	P3MOD0	R/W	0001	P3.0 Pin Control 0000~1111: see table 7.1
9Ch	**P3MOD32**	7~4	P3MOD3	R/W	0001	P3.3 Pin Control 0000~1111: see table 7.1
		3~0	P3MOD2	R/W	0001	P3.2 Pin Control 0000~1111: see table 7.1
9Dh	**P3MOD54**	7~4	P3MOD5	R/W	0001	P3.5 Pin Control 0000~1111: see table 7.1
		3~0	P3MOD04	R/W	0001	P3.4 Pin Control 0000~1111: see table 7.1
9Eh	**P3MOD76**	7~4	P3MOD7	R/W	0001	P3.7 Pin Control 0000~1111: see table 7.1
		3~0	P3MOD6	R/W	0001	P3.6 Pin Control 0000~1111: see table 7.1

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
9Fh	**UARTBRP**	7~0	UARTBRP	W	00h	UART Baud rate Control UART BAUD Rate = Fsys/16/UARTBRP
A1h	**PWMCON**	7~6	PWM1CKS	R/W	00	PWM1~5 clock source 00: F_{SYSCLK} 01: FRC/256 10: FRC 11: FRC x 2 (V_{CC} > 3.0V)
		5	PWM1EN	R/W	0	PWM1~5 Enable. 0: PWM1~5 Disable 1: PWM1~5 ensable
		4	PWM0EN	R/W	0	PWM0 Enable. 0: PWM0 Disable 1: PWM0 ensable
		3~2	PWM0CKS	R/W	00	PWM0 clock source 00: F_{SYSCLK} 01: FRC/256 10: FRC 11: FRC x 2 (V_{CC} > 3.0V)
		1	PWM0NMSK	R/W	0	PWM0N Mask Data. while CLRPWM0=1 and PMW0MSKE=1
		0	PWM0PMSK	R/W	0	PWM0P Mask Data. while CLRPWM0=1 and PMW0MSKE=1
A7h	**PWMCON2**	7	PWM0MOD	R/W	0	PWM0 mode select 0: Normal mode 1: Half-bridge mode
		6	PWM0MSKE	R/W	0	PWM0 mask output enable 0: Disable 1: Enable, PWM0P/PWM0N output data by PWM0PMSK/PWM0NMSK while CLRPWM0=1
		5~4	PWM0OM	R/W	00	PWM0 output mode select 00: Mode0 01: Mode1 10: Mode2 11: Mode3
		3~0	PWM0DZ	R/W	0000	PWM0 dead zone (Dead zone is prohibited in half-bridge mode) 0000: Disable 0001: 1 x T_{PWMCLK} ..... 1111: 15 x T_{PWMCLK}
A8h	**IE**	7	EA	R/W	0	Global interrupt enable control. 0: Disable all Interrupts. 1: Each interrupt is enabled or disabled by its own interrupt control bit.
		4	ES	R/W	0	Set 1 to enable Serial Port UART Interrupt
		3	ET1	R/W	0	Set 1 to enable Timer1 Interrupt
		2	EX1	R/W	0	Set 1 to enable external INT1 pin Interrupt & Halt/Stop mode wake up capability
		1	ET0	R/W	0	Set 1 to enable Timer0 Interrupt
		0	EX0	R/W	0	Set 1 to enable external INT0 pin Interrupt & Halt/Stop mode wake up capability
A9h	**INTE1**	7	PWMIE	R/W	0	Set 1 to enable PWM0~PWM1 interrupt
		4	EEPIE	R/W	0	Set 1 to enable EEP write finish interrupt
		3	ADIE	R/W	0	Set 1 to enable ADC Interrupt
		2	LVDIE	R/W	0	Set 1 to enable LVD interrupt
		1	PCIE	R/W	0	Set 1 to enable Port1,Port3 Pin Change Interrupt
		0	TM3IE	R/W	0	Set 1 to enable Timer3 Interrupt
AAh	**ADCDL**	7~4	ADCDL	R	–	ADC data bit 3~0
ABh	**ADCDH**	7~0	ADCDH	R	–	ADC data bit 11~4
ACh	**ADCDLYT**	7~0	ADCDLYT	R/W	0	PWM period match to delay trigger ADC start 8'h00: Disable PWM trigger ADC satrt 8'h01~8'hFF: enable and delay time (ADCDLYT[7:0]/Fadcks) to ADC start

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
B0h	**P3**	7~0	P3	R/W	FFh	Port3 data
B6h	**ADCHS**	7~3	ADCHS	R/W	1Fh	ADC Channel Select 00000: CH0 (P3.0) 00001: CH1 (P3.1) 00010: CH2 (P3.2) 00011: CH3 (P3.3) 00100: CH4 (P3.4) 00101: CH5 (P3.5) 00110: CH6 (P3.6) 00111: CH7 (P1.0) 01000: CH8 (P1.1) 01001: CH9 (P1.2) 01010: CH10 (P1.3) 01011: CH11(P1.4) 01100: CH12 V_{BG} (Internal Bandgap Reference Voltage) 01101: CH13 (P1.5) Others: reserved 11110: CH30(VCC/201) 11111: CH31(VCC/4)
		2	ADCVREFS	R/W	0	ADC reference voltage 0: V_{CC} 1: VBG
		1~0	VBGSEL	R/W	00	VBG voltage select, When ADCVREF is selected as VBG 00: 1.18V; 01: Reserved; 10: Reserved; 11: Reserved
B8h	**IP**	4	PS	R/W	0	Serial Port UART Interrupt Priority Low bit
		3	PT1	R/W	0	Timer1 Interrupt Priority Low bit
		2	PX1	R/W	0	External INT1 Pin Interrupt Priority Low bit
		1	PT0	R/W	0	Timer0 Interrupt Priority Low bit
		0	PX0	R/W	0	External INT0 Pin Interrupt Priority Low bit
B9h	**IPH**	4	PSH	R/W	0	Serial Port UART Interrupt Priority High bit
		3	PT1H	R/W	0	Timer1 Interrupt Priority High bit
		2	PX1H	R/W	0	External INT1 Pin Interrupt Priority High bit
		1	PT0H	R/W	0	Timer0 Interrupt Priority High bit
		0	PX0H	R/W	0	External INT0 Pin Interrupt Priority High bit
BAh	**IP1**	7	PPWM	R/W	0	PWM Interrupt Priority Low bit
		4	PEEP	R/W	0	EEP Interrupt Priority Low bit
		3	PADI	R/W	0	ADC Interrupt Priority Low bit
		2	PLVD	R/W	0	LVD Interrupt Priority Low bit
		1	PPC	R/W	0	Port1/Port3 pin change Interrupt Priority Low bit
		0	PT3	R/W	0	Timer3 Interrupt Priority Low bit
BBh	**IP1H**	7	PPWMH	R/W	0	PWM Interrupt Priority High bit
		4	PEEPH	R/W	0	EEP Interrupt Priority High bit
		3	PADIH	R/W	0	ADC Interrupt Priority High bit
		2	PLVDH	R/W	0	LVD Interrupt Priority High bit
		1	PPCH	R/W	0	Port1/Port3 pin change Interrupt Priority High bit
		0	PT3H	R/W	0	Timer3 Interrupt Priority High bit

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
BFh	**LVDS**	7	LVDM	R/W	0	0: VCC < VLVD (LVDIF = 1 while LVDO = 1) 1: VCC > VLVD (LVDIF = 1 while LVDO = 0)
		6	LVDO	R	0	LVD real-time Output
		5	LVDHYS	R/W	0	LVD Hysteresis Enable 0: LVD Hysteresis disable 1: LVD Hysteresis enable
		4	LVDPD	R/W	0	LVD Power Down. 0: LVD Enable, 1: LVD Disable
		3~0	LVDSEL	R/W	0h	Low Voltage Detect (LVD) select. 0000: set LVD at 1.62V 0001: set LVD at 1.71V 0010: set LVD at 1.83V 0011: set LVD at 1.95V 0100: set LVD at 2.07V 0101: set LVD at 2.19V 0110: set LVD at 2.31V 0111: set LVD at 2.43V 1000: set LVD at 2.56V 1001: set LVD at 2.68V 1010: set LVD at 2.81V 1011: set LVD at 2.93V 1100: set LVD at 3.05V 1101: set LVD at 3.17V 1110: set LVD at 3.30V 1111: set LVD at 3.42V
C9h	**EEPCON**	7~0	EEPCON	W	–	Write E2h to set EEPWE flag; write other value to clear EEPWE flag. It is recommended to clear it immediately after EEPROM write.
		5	EEPWE	R	0	Flag indicates EEPROM memory can be written or not 0: EEPROM Write disable 1: EEPROM Write enable
		3	EEPTO	R	0	Time-Out flag of EEPROM write Set by H/W when EEPROM write Time-out occurs. Cleared this flag by H/W when EEPWE=0.
D0h	**PSW**	7	CY	R/W	0	ALU carry flag
		6	AC	R/W	0	ALU auxiliary carry flag
		5	F0	R/W	0	General purpose user-definable flag
		4	RS1	R/W	0	Register Bank Select bit 1
		3	RS0	R/W	0	Register Bank Select bit 0
		2	OV	R/W	0	ALU overflow flag
		1	F1	R/W	0	General purpose user-definable flag
		0	P	R/W	0	Parity flag
D1h	**PWM0DH**	7~0	PWM0DH	R/W	00h	PWM0 duty high byte
D2h	**PWM0DL**	7~0	PWM0DL	R/W	00h	PWM0 duty low byte
D3h	**PWM1DH**	7~0	PWM1DH	R/W	00h	PWM1 duty high byte
D4h	**PWM1DL**	7~0	PWM1DL	R/W	00h	PWM1 duty low byte
D5h	**PWM2DH**	7~0	PWM2DH	R/W	00h	PWM2 duty high byte
D6h	**PWM2DL**	7~0	PWM2DL	R/W	00h	PWM2 duty low byte
D7h	**FRCFT**	4~0	FRCFT	R/W	00	FRC Fine Tune
D8h	**CLKCON**	5	STPSCK	R/W	1	Set 1 to stop Slow clock in PDOWN mode
		4	STPPCK	R/W	0	Set 1 to stop UART/Timer0/1/2 clock in Idle mode for current reducing.
		3	STPFCK	R/W	0	Set 1 to stop Fast clock for power saving in Slow/Idle mode. This bit can be changed only in Slow mode.
		2	SELFCK	R/W	0	System clock select. This bit can be changed only when STPFCK=0. 0: Slow clock 1: Fast clock
		1~0	CLKPSC	R/W	11	System clock prescaler. Effective after 16 clock cycles (Max.) delay.

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
						00: System clock is Fast/Slow clock divided by 16 01: System clock is Fast/Slow clock divided by 4 10: System clock is Fast/Slow clock divided by 2 11: System clock is Fast/Slow clock divided by 1
D9h	**PWM0PRDH**	7~0	PWM0PRDH	R/W	FFh	PWM0 period high byte
DAh	**PWM0PRDL**	7~0	PWM0PRDL	R/W	FFh	PWM0 period low byte
DBh	**PWM1PRDL**	7~0	PWM1PRDL	R/W	FFh	PWM1/2/3 period low byte
DCh	**PWM1PRDL**	7~0	PWM1PRDL	R/W	FFh	PWM1/2/3 period low byte
DDh	**PWM3DL**	7~0	PWM3DL	R/W	00h	PWM3 duty low byte
DEh	**PWM3DL**	7~0	PWM3DL	R/W	00h	PWM3 duty low byte
DFh	**RDCTL**	2	ATDEN	R/W	1	MTP ATD(Address Transition Detection) read control enablel; 0: MTP Read always=1 1: MTP Read use ATD (for power saving at at slow clock)
		1~0	ATDT	R/W	1h	ATD timing controlwhen ATDEN=1 0: 6.8ns@5V or 10.7ns@3V 1: 12.2ns@5V or 19.4ns@3V 2: 17.6ns@5V or 28ns@3V 3: 23ns@5V or 37ns@3V
E0h	**ACC**	7~0	ACC	R/W	00h	Accumulator
E3h	**LVRCON**	4	LVRPD	R/W	0	LVR Power Down. 0: LVR Enable, 1: LVR Disable
		3~0	LVRSEL	R/W	0	Low Voltage Reset (LVR) select. 0000: set LVR at 1.62V 0001: set LVR at 1.69V 0010: set LVR at 1.82V 0011: set LVR at 1.94V 0100: set LVR at 2.06V 0101: set LVR at 2.17V 0110: set LVR at 2.29V 0111: set LVR at 2.41V 1000: set LVR at 2.54V 1001: set LVR at 2.66V 1010: set LVR at 2.78V 1011: set LVR at 2.90V 1100: set LVR at 3.03V 1101: set LVR at 3.15V 1110: set LVR at 3.27V 1111: set LVR at 3.39V
E5h	**EFTCON**	7	EFT2CS	W	0	EFT2 Detector enable 0: Disable EFT2 1: Enable EFT2
		6	EFT1CS	W	0	EFT1 Detector enable 0: Disable EFT1 1: Enable EFT1
		5~4	EFT1S	W	00	EFT1 Detector sensitivity adjustment
		3	EFTSLOW	W	0	Force SYSCLK to SLOWCLK while EFT detected 0: Disable; 1: Enable
		1	EFTWOUT	W	0	EFTWAIT output to pin 0: P3.6 = normal I/O 1: P3.6 = EFTWAIT
		0	CKHLDE	W	0	clock hold enable 0: Disabl; 1: Enable
EAh	**CFGSRC**	4~0	SRCTRIM	R/W	-	SRC trimming value
EFh	**AUX3**	7	warmtime	R/W	0	Warm-up time for wake-up from Power Down mode 0: 128 Clock 1: 64 Clock

Adr	SFR	Bit#	Bit Name	R/W	Rst	Description
		6~4	TM3PSC	R/W	000	Timer3 Interrupt rate 000: Timer3 Interrupt rate is 65536 Timer3 clock cycle 001: Timer3 Interrupt rate is 32768 Timer3 clock cycle 010: Timer3 Interrupt rate is 16384 Timer3 clock cycle 011: Timer3 Interrupt rate is 8192 Timer3 clock cycle 100: Timer3 Interrupt rate is 4096 Timer3 clock cycle 101: Timer3 Interrupt rate is 2048 Timer3 clock cycle 110: Timer3 Interrupt rate is 1024 Timer3 clock cycle 111: Timer3 Interrupt rate is 512 Timer3 clock cycle
		2	IOVIS	R/W	0	GPIO VIH/VIL selection 0: VIH=0.7VDD, VIL=0.3VDD 1:VIH=0.4VDD, VIL=0.2VDD(Not support in ICE emulation)
F0h	**B**	7~0	B	R/W	00h	B register
F1h	**CRCDL**	7~0	CRCDL	R/W	FFh	16-bit CRC data bit 7~0
F2h	**CRCDH**	7~0	CRCDH	R/W	FFh	16-bit CRC data bit 15~8
F3h	**CRCIN**	7~0	CRCIN	W	–	CRC input data
F5h	**CFGBG**	4~0	BG1TRIM	R/W	–	VBG trimming value
F6h	**CFGWL**	6~0	FRCTRIM	R/W	–	FRC frequency adjustment 00h: lowest frequency 7Fh: highest frequency
F7h	**AUX2**	7~6	WDTE	R/W	00	Watchdog Timer Reset control 0x: WDT disable 10: WDT enable in Fast/Slow mode, disable in Idle/Halt/Stop mode 11: WDT always enable
		5	PWRSAV	R/W	0	Set 1 to reduce the chip's power consumption at Idle/Halt/Stop Mode.
		4	VBGOUT	R/W	0	Bandgap voltage output control 0: P3.2 as normal I/O 1: Bandgap voltage output to P3.2 pin
		2~1	EEPTE	R/W	00	EEP watchdog timer enable 00: Disable 01: wait 7.7 ms trigger watchdog time-out flag 10: wait 31ms trigger watchdog time-out flag 11: wait 62 ms trigger watchdog time-out flag
F8h	**AUX1**	7	CLRWDT	R/W	0	Set 1 to clear WDT, H/W auto clear it at next clock cycle
		6	CLRTM3	R/W	0	Set 1 to clear Timer3, HW auto clear it at next clock cycle.
		5	CLRPWM0	R/W	0	PWM0 clear enable 0: PWM0 is running 1: PWM0 is cleared and held
		4	ADSOC	W	0	ADC Start of Conversion Set 1 to start ADC conversion. Cleared by H/W at the end of conversion. S/W can also write 0 to clear this flag.
			ADSOC	R	0	When ADCDLYT=0 (ref. SFR ACh)
			ADC EOC	R	0	When ADCDLY!=0 (ref. SFR ACh)
		3	CLRPWM1	R/W	0	PWM1/2/3 clear enable 0: PWM1/2/3 is running 1: PWM1/2/3 is cleared and held
		2	T0SEL	R/W	0	Timer0 counter mode (CT0N=1) input select 0: P3.4 pin 1:Slow clock divide by 4 (SLOWCLK/4)
		1	T1SEL	R/W	0	Timer1 counter mode (CT1N=1) input select 0: P3.5 (T1) pin (8051 standard) 1: Slow clock divide by 4 (SLOWCLK/4)
		0	DPSEL	R/W	0	Active DPTR Select

Adr	Flash	Bit#	Bit Name	Description
1FF9h	**CFGBG**	4~0	BG1TRIM	VBG2 adjustment. VBG is trimmed to 1.18V in chip manufacturing.
1FFBh	**CFGSRC**	4~0	SRCTRIM	SRC frequency adjustment. SRC is trimmed to 131KHz in chip manufacturing.
1FFDh	**CFGWL**	6~0	FRCTRIM	FRC frequency adjustment. FRC is trimmed to 16.5888 MHz in chip manufacturing.
1FFFh	**CFGWH**	7	PROT	Flash Code Protect, 1=Protect
		6	XRSTE	External Pin Reset enable, 1=enable.
		5~0	-	Reserved

INSTRUCTION SET

Instructions are 1, 2 or 3 bytes long as listed in the 'byte' column below. Each instruction takes 1~8 System clock cycles to execute as listed in the 'cycle' column below

ARITHMETIC				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ADD A, Rn	Add register to A	1	2	28-2F
ADD A, dir	Add direct byte to A	2	2	25
ADD A, @Ri	Add indirect memory to A	1	2	26-27
ADD A, #data	Add immediate to A	2	2	24
ADDC A, Rn	Add register to A with carry	1	2	38-3F
ADDC A, dir	Add direct byte to A with carry	2	2	35
ADDC A, @Ri	Add indirect memory to A with carry	1	2	36-37
ADDC A, #data	Add immediate to A with carry	2	2	34
SUBB A, Rn	Subtract register from A with borrow	1	2	98-9F
SUBB A, dir	Subtract direct byte from A with borrow	2	2	95
SUBB A, @Ri	Subtract indirect memory from A with borrow	1	2	96-97
SUBB A, #data	Subtract immediate from A with borrow	2	2	94
INC A	Increment A	1	2	04
INC Rn	Increment register	1	2	08-0F
INC dir	Increment direct byte	2	2	05
INC @Ri	Increment indirect memory	1	2	06-07
DEC A	Decrement A	1	2	14
DEC Rn	Decrement register	1	2	18-1F
DEC dir	Decrement direct byte	2	2	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	8 / 16	A4
DIV AB	Divide A by B	1	8/16/32	84
DA A	Decimal Adjust A	1	2	D4

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ANL A, Rn	AND register to A	1	2	58-5F
ANL A, dir	AND direct byte to A	2	2	55
ANL A, @Ri	AND indirect memory to A	1	2	56-57
ANL A, #data	AND immediate to A	2	2	54
ANL dir, A	AND A to direct byte	2	2	52
ANL dir, #data	AND immediate to direct byte	3	4	53
ORL A, Rn	OR register to A	1	2	48-4F
ORL A, dir	OR direct byte to A	2	2	45
ORL A, @Ri	OR indirect memory to A	1	2	46-47
ORL A, #data	OR immediate to A	2	2	44
ORL dir, A	OR A to direct byte	2	2	42
ORL dir, #data	OR immediate to direct byte	3	4	43
XRL A, Rn	Exclusive-OR register to A	1	2	68-6F
XRL A, dir	Exclusive-OR direct byte to A	2	2	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	2	66-67
XRL A, #data	Exclusive-OR immediate to A	2	2	64
XRL dir, A	Exclusive-OR A to direct byte	2	2	62
XRL dir, #data	Exclusive-OR immediate to direct byte	3	4	63
CLR A	Clear A	1	2	E4
CPL A	Complement A	1	2	F4
SWAP A	Swap Nibbles of A	1	2	C4
RL A	Rotate A left	1	2	23
RLC A	Rotate A left through carry	1	2	33

LOGICAL				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
RR A	Rotate A right	1	2	03
RRC A	Rotate A right through carry	1	2	13

DATA TRANSFER				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
MOV A, Rn	Move register to A	1	2	E8-EF
MOV A, dir	Move direct byte to A	2	2	E5
MOV A, @Ri	Move indirect memory to A	1	2	E6-E7
MOV A, #data	Move immediate to A	2	2	74
MOV Rn, A	Move A to register	1	2	F8-FF
MOV Rn, dir	Move direct byte to register	2	4	A8-AF
MOV Rn, #data	Move immediate to register	2	2	78-7F
MOV dir, A	Move A to direct byte	2	2	F5
MOV dir, Rn	Move register to direct byte	2	4	88-8F
MOV dir, dir	Move direct byte to direct byte	3	4	85
MOV dir, @Ri	Move indirect memory to direct byte	2	4	86-87
MOV dir, #data	Move immediate to direct byte	3	4	75
MOV @Ri, A	Move A to indirect memory	1	2	F6-F7
MOV @Ri, dir	Move direct byte to indirect memory	2	4	A6-A7
MOV @Ri, #data	Move immediate to indirect memory	2	2	76-77
MOV DPTR, #data	Move immediate to data pointer	3	4	90
MOVC A, @A+DPTR	Move code byte relative DPTR to A	1	8	93
MOVC A, @A+PC	Move code byte relative PC to A	1	8	83
MOVX A, @Ri	Move external data (A8) to A	1	8	E2-E3
MOVX A, @DPTR	Move external data (A16) to A	1	8	E0
MOVX @Ri, A	Move A to external data (A8)	1	8	F2-F3
MOVX @DPTR, A	Move A to external data (A16)	1	8	F0
PUSH dir	Push direct byte onto stack	2	4	C0
POP dir	Pop direct byte from stack	2	4	D0
XCH A, Rn	Exchange A and register	1	2	C8-CF
XCH A, dir	Exchange A and direct byte	2	2	C5
XCH A, @Ri	Exchange A and indirect memory	1	2	C6-C7
XCHD A, @Ri	Exchange A and indirect memory nibble	1	2	D6-D7

BOOLEAN				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
CLR C	Clear carry	1	2	C3
CLR bit	Clear direct bit	2	2	C2
SETB C	Set carry	1	2	D3
SETB bit	Set direct bit	2	2	D2
CPL C	Complement carry	1	2	B3
CPL bit	Complement direct bit	2	2	B2
ANL C, bit	AND direct bit to carry	2	4	82
ANL C, /bit	AND direct bit inverse to carry	2	4	B0
ORL C, bit	OR direct bit to carry	2	4	72
ORL C, /bit	OR direct bit inverse to carry	2	4	A0
MOV C, bit	Move direct bit to carry	2	2	A2
MOV bit, C	Move carry to direct bit	2	4	92

BRANCHING				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
ACALL addr 11	Absolute jump to subroutine	2	6	11-F1
LCALL addr 16	Long jump to subroutine	3	6	12
RET	Return from subroutine	1	6	22
RETI	Return from interrupt	1	6	32
AJMP addr 11	Absolute jump unconditional	2	6	01-E1
LJMP addr 16	Long jump unconditional	3	6	02
SJMP rel	Short jump (relative address)	2	6	80
JC rel	Jump on carry = 1	2	4 (or 6)	40
JNC rel	Jump on carry = 0	2	4 (or 6)	50
JB bit, rel	Jump on direct bit = 1	3	4 (or 6)	20
JNB bit, rel	Jump on direct bit = 0	3	4 (or 6)	30
JBC bit, rel	Jump on direct bit = 1 and clear	3	4 (or 6)	10
JMP @A+DPTR	Jump indirect relative DPTR	1	6	73
JZ rel	Jump on accumulator = 0	2	4 (or 6)	60
JNZ rel	Jump on accumulator ≠ 0	2	4 (or 6)	70
CJNE A, dir, rel	Compare A, direct, jump not equal relative	3	4 (or 6)	B5
CJNE A, #data, rel	Compare A, immediate, jump not equal relative	3	4 (or 6)	B4
CJNE Rn, #data, rel	Compare register, immediate, jump not equal relative	3	4 (or 6)	B8-BF
CJNE @Ri, #data, rel	Compare indirect, immediate, jump not equal relative	3	4 (or 6)	B6-B7
DJNZ Rn, rel	Decrement register, jump not zero relative	2	4 (or 6)	D8-DF
DJNZ dir, rel	Decrement direct byte, jump not zero relative	3	4 (or 6)	D5

MISCELLANEOUS				
Mnemonic	**Description**	**byte**	**cycle**	**opcode**
NOP	No operation	1	2	00

In the above table, an entry such as E8-EF indicates a continuous block of hex opcodes used for 8 different registers, the register numbers of which are defined by the lowest three bits of the corresponding code. Non-continuous blocks of codes, shown as 11-F1 (for example), are used for absolute jumps and calls with the top 3 bits of the code being used to store the top three bits of the destination address.

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A=25°C)

Parameter	Rating	Unit
Supply voltage	V_{SS} –0.3 ~ V_{SS} +5.5	V
Input voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
Output voltage	V_{SS} –0.3 ~ V_{CC} +0.3	
All pins output current high	–80	
All pins output current low	+150	
Maximum Operating Voltage	5.5	V
Operating temperature	–40 ~ +105	°C
Storage temperature	–65 ~ +150	

2. DC Characteristics (T_A=25°C,V_{CC}=1.8V ~ 5.5V)

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
Operating Voltage	V_{CC}	F_{SYSCLK} = FRC/1=16.5888 MHz		2.4	–	5.5	V
		F_{SYSCLK} <= FRC/2=8.2944 MHz		1.8	–	5.5	
Input High Voltage	V_{IH}	All Input	V_{CC}=5V, IOVIS=0	0.7V_{CC}	–	–	V
			V_{CC}=5V, IOVIS=1	0.4V_{CC}			
			V_{CC}=3V, IOVIS=0	–	–	0.3 V_{CC}	V
			V_{CC}=3V, IOVIS=1			0.2V_{CC}	
Input Low Voltage	V_{IL}	All Input	V_{CC}=5V	–	–	0.2V_{CC}	V
			V_{CC}=3V	–	–	0.2V_{CC}	V
I/O Port Source Current	I_{OH}	All Output (P1.0~P1.5, P3.0~P3.7)	V_{CC}=5V, V_{OH}=0.9V_{CC}	12	13. 5	-	mA
			V_{CC}=5V, V_{OH}=0.6V_{CC}	36	40	-	
			V_{CC}=3V, V_{OH}=0.9V_{CC}	5	5. 5	-	
			V_{CC}=3V, V_{OH}=0.66V_{CC}	14	15. 5	-	
I/O Port Sink Current	I_{OL}	All Output	V_{CC}=5V, V_{OL}=0.1V_{CC}	37	41	-	mA
			V_{CC}=3V, V_{OL}=0.1V_{CC}	9	18. 5	-	
Power Supply Current	I_{DD}	Fast mode V_{CC}=5V, No Load	FRC=16.5888 MHz	-	6	-	mA
			FRC=8.2944 MHz	-	4	-	
		Fast mode V_{CC}=3V, No Load	FRC=16.5888 MHz	-	3. 3	-	
			FRC=8.2944 MHz	-	2. 4	-	
		Slow mode No Load	V_{CC}=5V	-	65	-	µA
			V_{CC}=3V	–	34	–	
		Idle mode PWRSAV=0 No Load	SRC, V_{CC}=5V POR ON	–	16	–	µA
			SRC, V_{CC}=5V LVR ON		70		
			SRC, V_{CC}=3V POR ON	–	6	–	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
			SRC, V_{CC}=3V LVR ON		44		
		Idle mode PWRSAV=1 No Load	SRC, V_{CC}=5V	–	16	–	
			SRC, V_{CC}=3V	–	6	–	
		Stop mode PWRSAV=1 No Load	V_{CC}=5V	–	0.7	–	
			V_{CC}=3V	–	0.5	–	
		Halt mode PWRSAV=1 No Load	V_{CC}=5V (Timer3=0.5秒)	–	12	–	
			V_{CC}=3V (Timer3=0.5秒)	–	4	–	
System Clock Frequency	F_{SYSCLK}	V_{CC} >LVR_{TH}	V_{CC}=2.4V	–	–	16.5888	MHz
LVR Reference Voltage	V_{LVR}	T_A=25°C		–	3.39	–	V
				–	3.27	–	
				–	3.15	–	
				–	3.03	–	
				–	2.90	–	
				–	2.78	–	
				–	2.66	–	
				–	2.54	–	
				–	2.41	–	
				–	2.29	–	
				–	2.17	–	
				–	2.06	–	
				–	1.94	–	
				–	1.82	–	
				–	1.69	–	
				–	1.62	–	

Parameter	Symbol	Conditions		Min	Typ	Max	Unit
LVD Reference Voltage	V_{LVD}	T_A=25°C		–	3.42	–	V
				–	3.3	–	
				–	3.17	–	
				–	3.05	–	
				–	2.93	–	
				–	2.81	–	
				–	2.68	–	
				–	2.56	–	
				–	2.43	–	
				–	2.31	–	
				–	2.19	–	
				–	2.07	–	
				–	1.95	–	
				–	1.83	–	
				–	1.71	–	
				–	1.62	–	
LVR Hysteresis Voltage	V_{HYST}	T_A=25°C		–	±0.1	–	V
Low Voltage Detection time	t_{LVR}	T_A=25°C		100	–	–	μs
Pull-Up Resistor	R_{PU}	V_{IN}=0V	V_{CC}=5V	–	32	–	KΩ
			V_{CC}=3V	–	32	–	
Pull-Down Resistor	R_{PD}	V_{IN}=0V	V_{CC}=5V	–	32	–	
			V_{CC}=3V	–	32	–	

3. Clock Timing (T_A= –40°C ~ +105°C)

Parameter	Condition	Min	Typ	Max	Unit
FRC Frequency	25℃,V_{CC}=5.0V	–1%	16.5888	+1%	MHz
	-40℃ ~ 105℃,V_{CC}=5.0V	–1.5%	16.5888	+1.5%	
	-40℃ ~ 105℃,V_{CC}=3.0 ~ 5.0V	–2.5%	16.5888	+2.5%	

4. Reset Timing Characteristics (T_A= –40°C ~ +105°C)

Parameter	Conditions	Min	Typ	Max	Unit
RESET Input Low width	Input V_{CC}=5V ± 10 %	30	–	–	μs
WDT wake up time	V_{CC}=5V, WDTPSC=11	–	60	–	ms
	V_{CC}=3V, WDTPSC=11	–	78	–	
CPU start up time	V_{CC} = 5 V	–	8.6	–	ms

5. ADC Electrical Characteristics (T_A= 25°C,V_{CC}= 3.0V ~ 5.5V,V_{SS}= 0V)

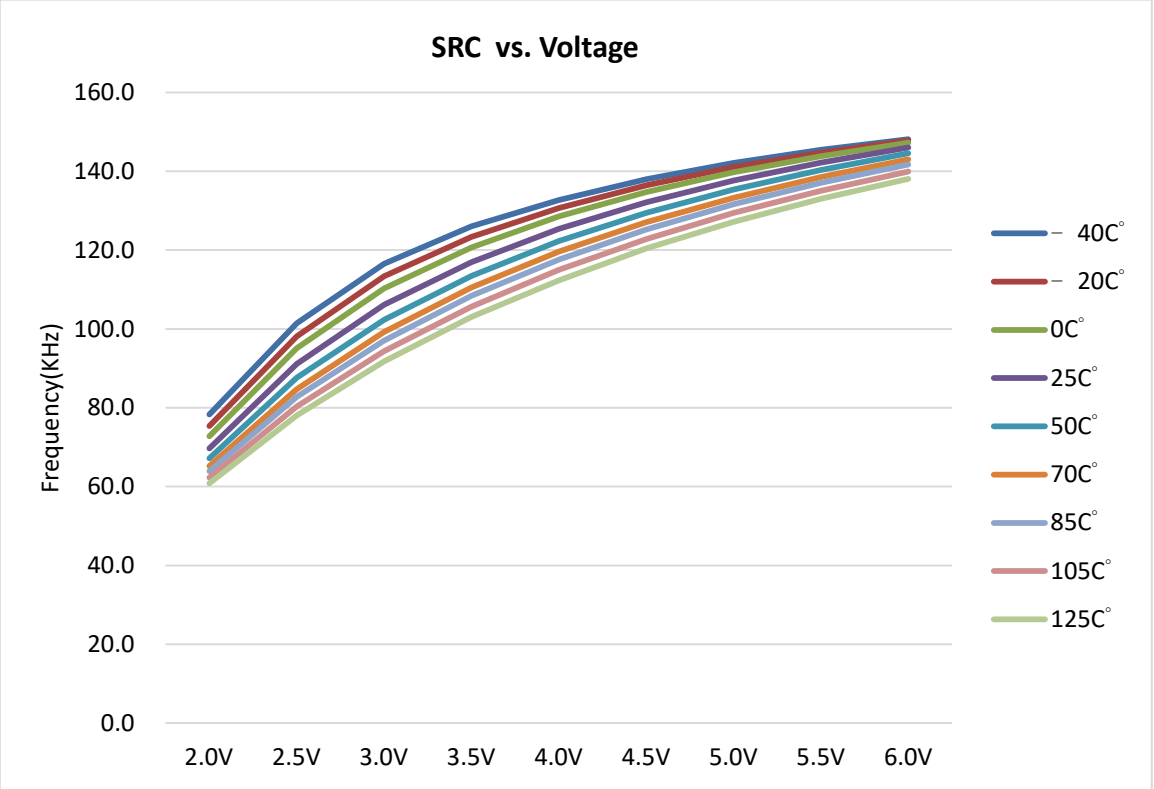
Parameter	Conditions		Min	Typ	Max	Unit
Total Accuracy	V_{CC}=5.12 V, V_{SS}=0V		–	±2.5	±4	LSB
Integral Non-Linearity			–	±3.2	±5	
Max Input Clock (f_{ADC})	Source impedance (Rs < 10K omh)		–	–	2	MHz
	Source impedance (Rs < 20K omh)		–	–	1	
	Source impedance (Rs < 50K omh)		–	–	0.5	
	Source is V_{BG} (ADCHS=01100b)		–	–	2.3	
Conversion Time	F_{ADC} = 1MHz		–	50	–	μs
BandGap Voltage Reference (V_{BG})	VBGSEL=00	V_{CC}=2.5V~5.2V -40°C ~105°C	-1.5%	1.18	1.5%	V
ADC Reference Voltage (V_{ADC})	ADCVREFS=1	V_{CC}=3V~5.2V -40°C ~105°C	-1.5%	1.18	+1.5%	
V_{CC}/4 Reference Voltage ($V_{1/4}$)	–	V_{CC}=5V,25°C	-0.8%	1.26	+0.8%	
		V_{CC}=3.6V,25°C	-0.8%	0.907	+0.8%	
Input Voltage	–		V_{SS}	–	V_{CC}	

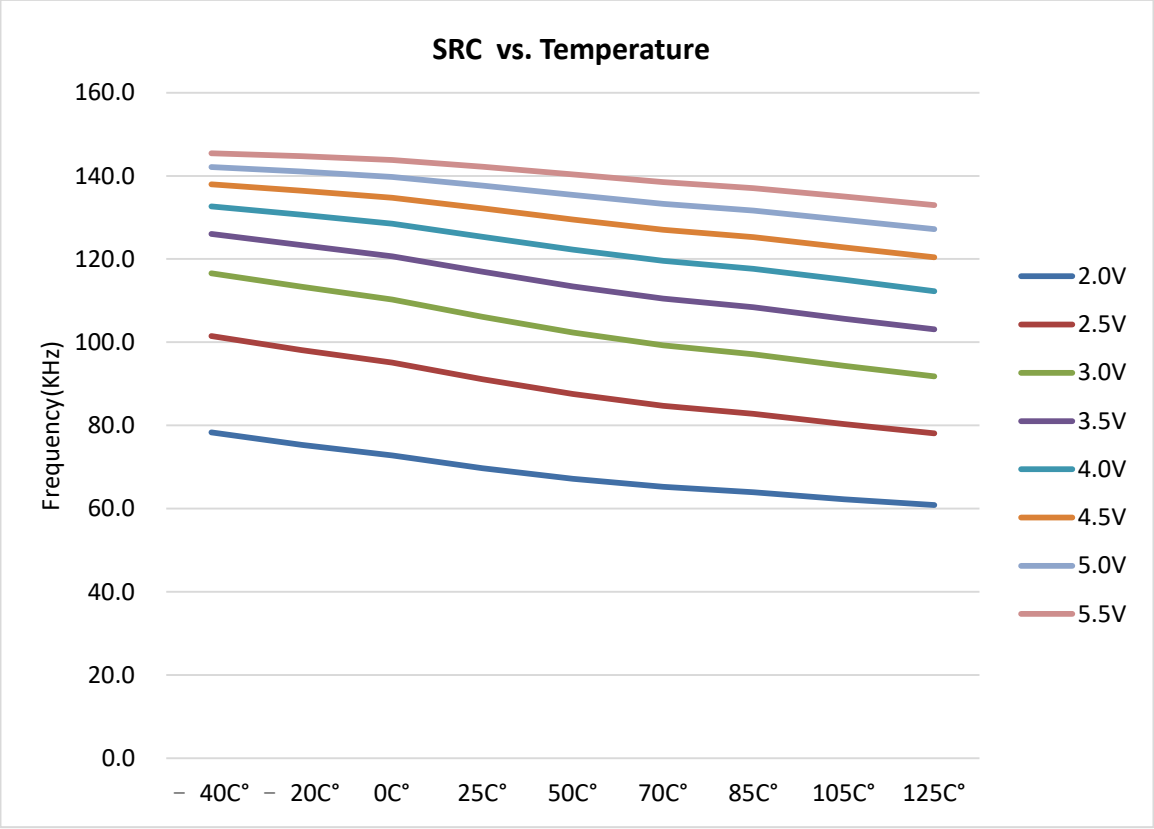
6. EEPROM Characteristics

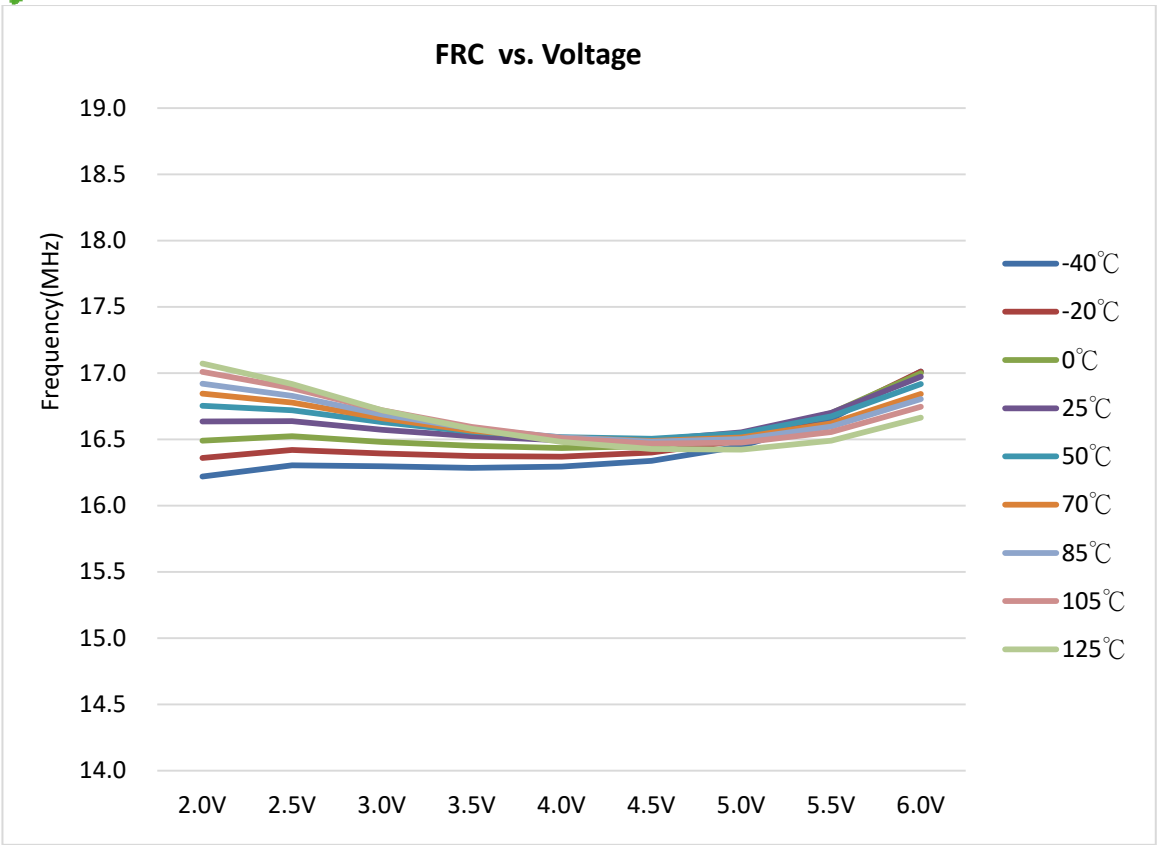
Parameter	Conditions	Min	Typ	Max	Unit
Write Voltage V_{EEWR}	-40°C ~ 105° Fsys=FRC/1, V_{CC} /47uF	3.0		5.5	V
	-40°C ~ 105° Fsys=FRC/2, V_{CC} /47uF	2.5		5.5	
Read Voltage V_{EERD}	-40°C ~ 105° Fsys=FRC/1, V_{CC}/47uF	2.0		5.5	
*Write Endurance N_{EE}	V_{CC}=2.5~5.5V, -40℃ ~105℃	20K	–	–	cycles
	V_{CC} =2.5~5.5V, -20℃ ~ 85℃	30K	–	–	
	V_{CC} =3.0~5.5V, 0℃ ~ 70℃	50K	–		
Write Time T_{EEWR}	V_{CC} =5.0V, 25℃, WDT disable		1.5		mS
	V_{CC} =2.5V, 25℃, WDT disable		4		
	V_{CC} =3.0V, 105℃, WDT disable		15		
Data Retention Y_{RET}		10			Year

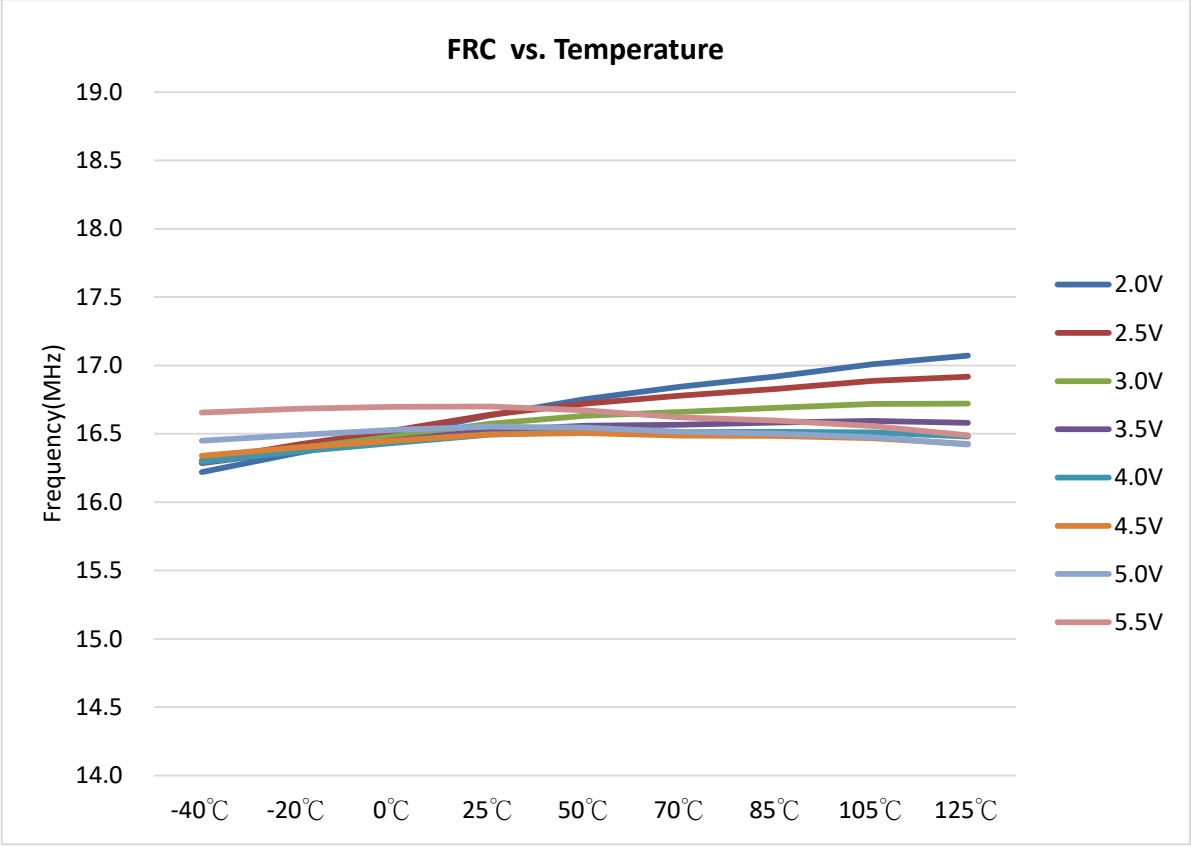
Note: The value of this parameter is based on the characteristics of tested samples

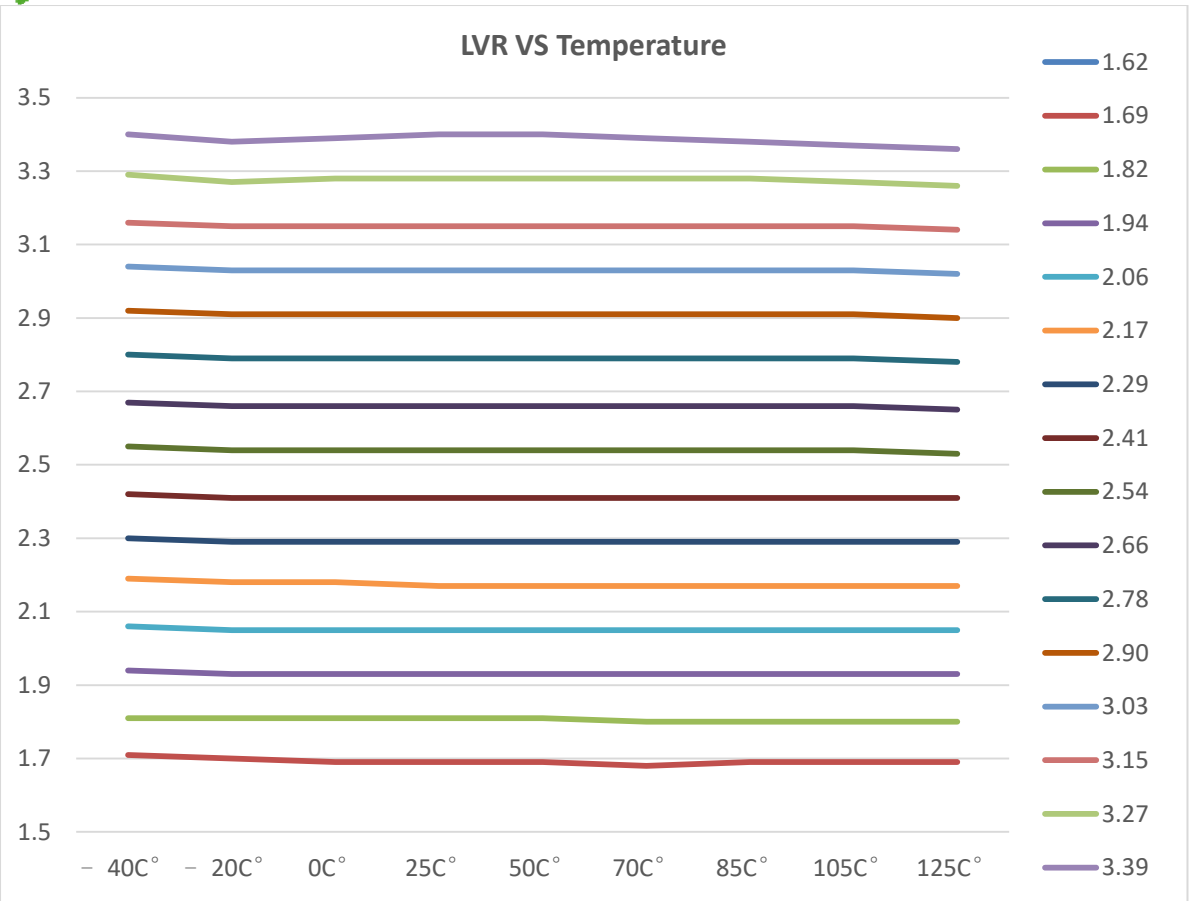
7. Characteristic Graphs

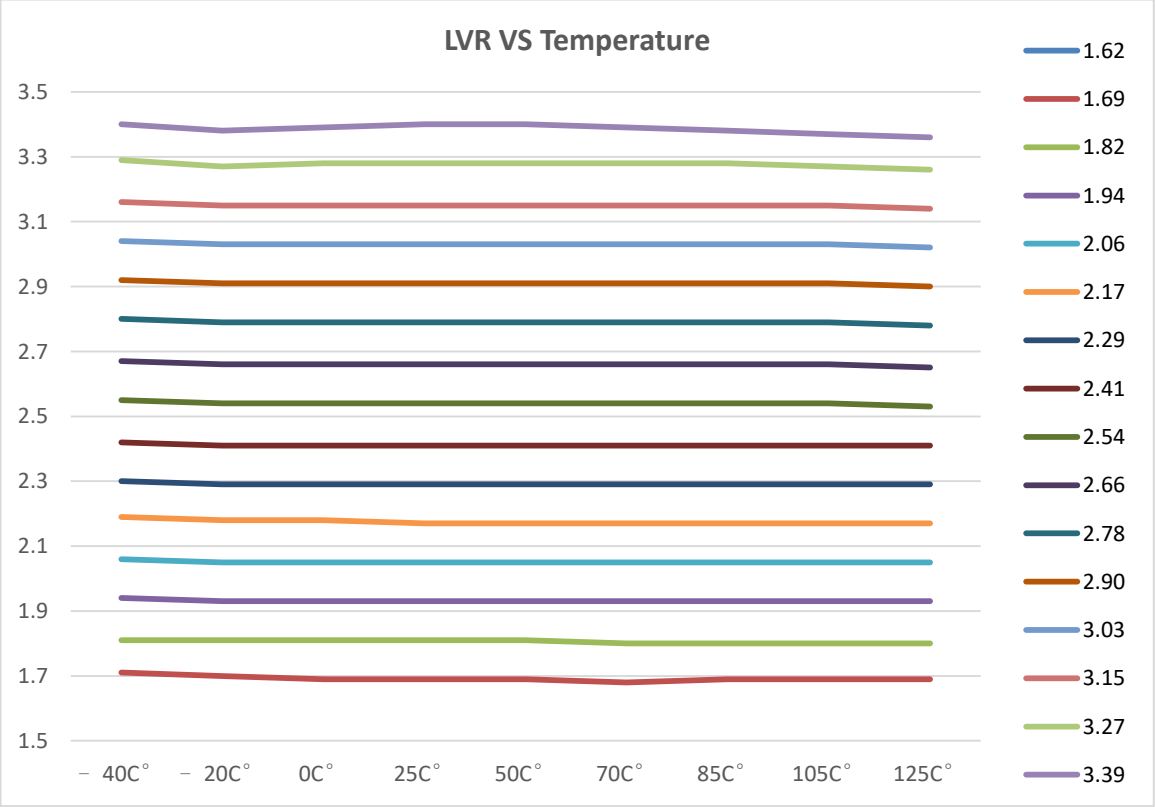


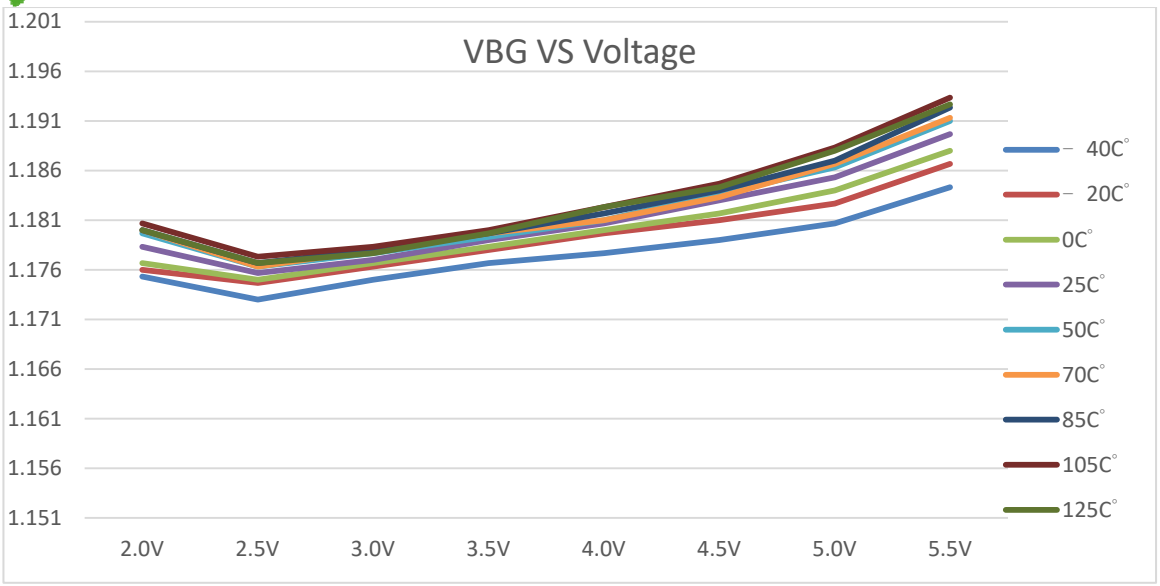



FRC vs. Voltage
Frequency(MHz)
19.0
18.5
18.0
17.5
17.0
16.5
16.0
15.5
15.0
14.5
14.0
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
6.0V
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃
125℃


FRC vs. Temperature
Frequency(MHz)
19.0
18.5
18.0
17.5
17.0
16.5
16.0
15.5
15.0
14.5
14.0
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃
105℃
125℃
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V


LVR VS Temperature
3.5
3.3
3.1
2.9
2.7
2.5
2.3
2.1
1.9
1.7
1.5
-40C°
-20C°
0C°
25C°
50C°
70C°
85C°
105C°
125C°
1.62
1.69
1.82
1.94
2.06
2.17
2.29
2.41
2.54
2.66
2.78
2.90
3.03
3.15
3.27
3.39


LVR VS Temperature
3.5
3.3
3.1
2.9
2.7
2.5
2.3
2.1
1.9
1.7
1.5
-40C°
-20C°
0C°
25C°
50C°
70C°
85C°
105C°
125C°
1.62
1.69
1.82
1.94
2.06
2.17
2.29
2.41
2.54
2.66
2.78
2.90
3.03
3.15
3.27
3.39


VBG VS Voltage
1.201
1.196
1.191
1.186
1.181
1.176
1.171
1.166
1.161
1.156
1.151
2.0V
2.5V
3.0V
3.5V
4.0V
4.5V
5.0V
5.5V
40C°
20C°
0C°
25C°
50C°
70C°
85C°
105C°
125C°

Package and Dice Information

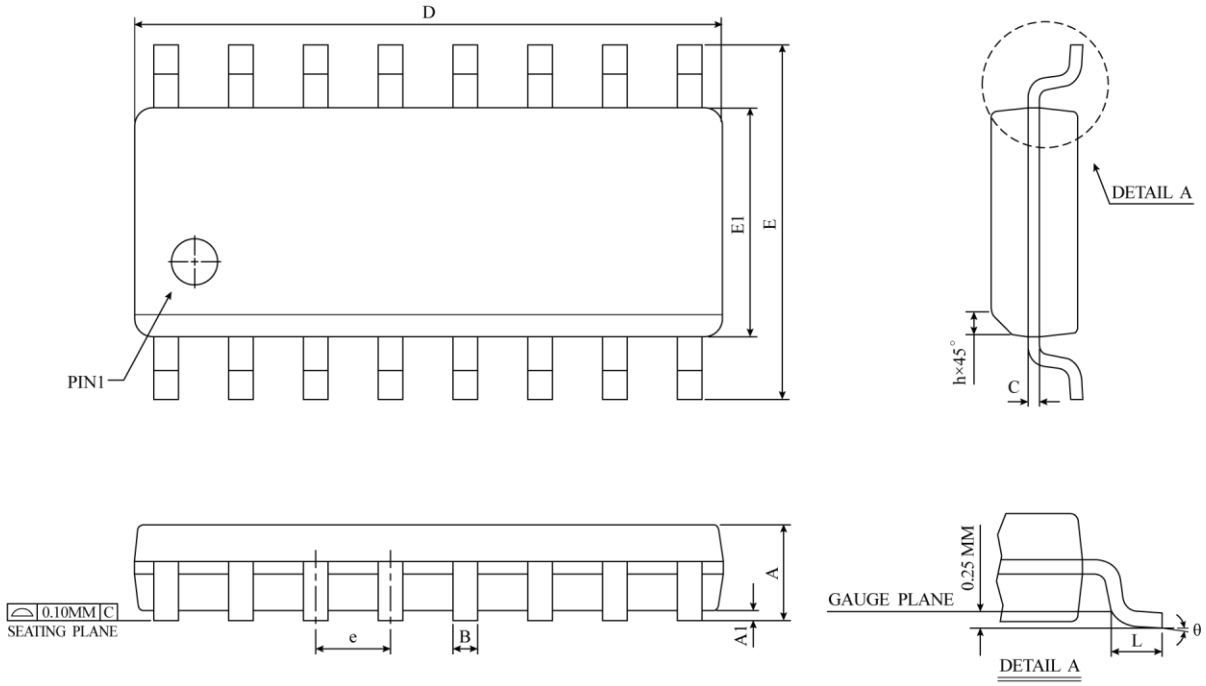
Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

Ordering information

Ordering number	Package
TM52E5223-MTP	Wafer/Dice blank chip
TM52E5223-COD	Wafer/Dice with code
TM52E52232S1	SOP 16-pin (150 mil)
TM52E5223ES	SOP 14-pin (150 mil)
TM52E52231S	SOP 8-pin (150 mil)

Package Information

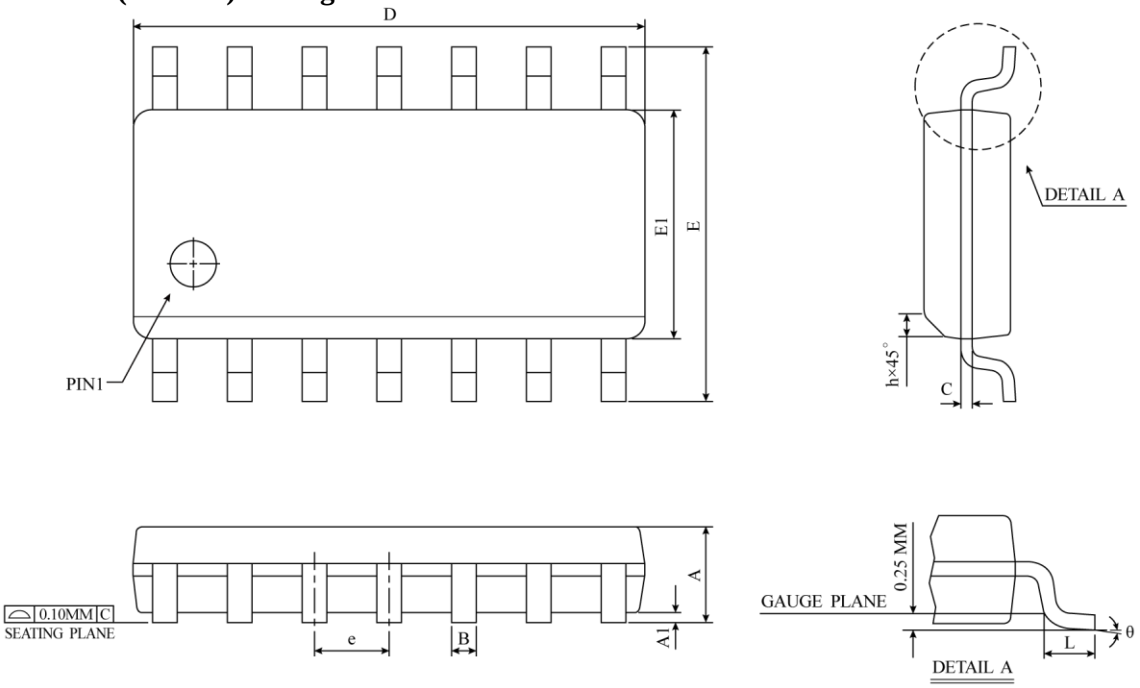
- **SOP-16 (150mil) Package Dimension**



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	9.80	9.90	10.00	0.3859	0.3898	0.3937
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AC)					

⚠ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

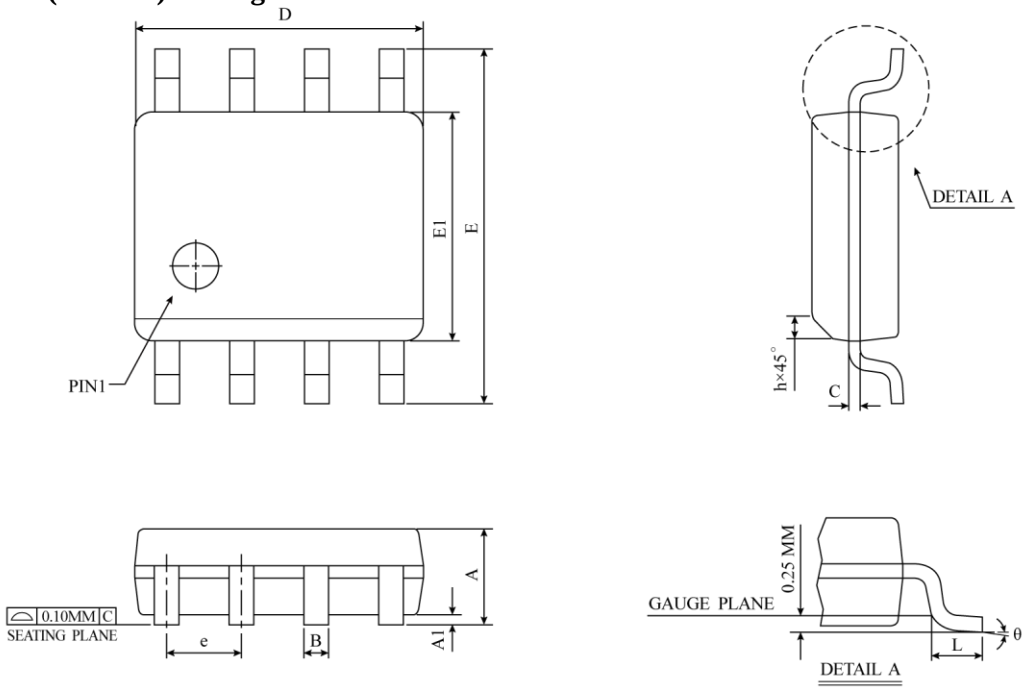
- **SOP-14 (150mil) Package Dimension**



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	8.55	8.65	8.75	0.3367	0.3410	0.3444
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AB)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

- **SOP-8 (150mil) Package Dimension**



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	4.80	4.90	5.00	0.1890	0.1939	0.1988
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AA)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL
NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.