TM57P8620
TM57P8625
TM57P8640
TM57P8645

DATA SHEET

Rev 0.97

AMENDMENT HISTORY

Version	Date	Description
0.90	Aug, 2021	New Release.
0.91	Feb, 2022	1. Added slow crystal oscillator (SXT) characteristics (p.90) 2. Added FIRC characteristic curve (p.92) 3. Correct the unit error in the SIRC characteristic graph (p.93)
0.92	May, 2022	1. Corrected WDT time misplacement (p.8) 2. HIX2 supplementary description, LCDON=1 is required (p.61, p.87) 3. Modified RFC sequence diagram and example (p.67) 4. Added LQFP48 package 5. Modified PA7 pull-up resistor reference value and application conditions (p.91)
0.93	Aug, 2022	1. Update the programming request pins (add PA4) (p.16) 2. Supplementary description of the IAP chapter (p.24) 3. Correct the typo of SEG29/COM3 (p.13)
0.94	Mar, 2023	1. TM0CKS=0 is Fsys (p.53, p.85) 2. Update Application curcuit (p.11)
0.95	Apr, 2023	1. Added upper and lower limits of POR voltage 2. Added upper and lower limits for SIRC frequency @3V
0.96	May, 2023	1. LCD brightness diagram error correction 2. Update die pad list 3. Update VIH,VIL, IOH (p.91) 4. Update SXT start-up voltage (p.92)
0.97	Jul, 2023	1. Adjust the typical value of SIRC clock frequency at 3V

CONTESTS

FAMILY OVERVIEW

P/N	Typ. V_{BAT}	ROM	RAM (bytes)	I/O (Max.)	RFC	Timers	8-bit PWM	Max. LCD S x C	LCD Bias	Time-piece current
TM57M5610	3.0V	1Kx14 MTP	96	12	3-ch	8-bit x1 21-bit x1	x1	11 x 4	1/2	1uA
TM57M5615	1.5V									1.5uA
TM57M5620	3.0V	2Kx14 MTP	176	16	4-ch	8-bit x2 21-bit x1	x2	28 x 4	1/3	3uA
TM57M5625	1.5V							26 x 4	1/2, 1/3	2uA
TM57P8620	3.0V	2Kx14 OTP	176	12	3-ch	8-bit x2 21-bit x1	x1	12 x 4	1/3	3uA
TM57P8625	1.5V							10 x 4	1/2, 1/3	2uA
TM57M5640	3.0V	4Kx14 MTP	336	20	4-ch	8-bit x2 21-bit x1	x2	44 x 4	1/3	3uA
TM57M5645	1.5V							42 x 4	1/2, 1/3	2uA
TM57P8640	3.0V	4Kx14 OTP	336	16	4-ch	8-bit x2 21-bit x1	x2	28 x 4	1/3	3uA
TM57P8645	1.5V							26 x 4	1/2, 1/3	2uA

Note: No matter V_{BAT}=3V or V_{BAT}=1.5V, the typical LCD bias voltage is:
1/2 bias: VL1=1.5V, V_{LCD}=3V
1/3 bias: VL1=1.0V, VL2=2.0V, V_{LCD}=3V

FEATURES

1. **Operating Voltage :**

   P8620: V_{BAT}= POR~3.6V

   P8625: V_{BAT}= LVCR~1.8V

   P8640:V_{BAT}= POR~3.6V

   P8645:V_{BAT}= LVCR~1.8V

***Note**: POR means "power on reset" (power on reset), LVCR means "ROM error reset"*

***Note**: VBAT must exceed POR at power-up. Set POROFF = 0x37 (disable POR) to obtain the lowest VBAT operation, LVCR (ROM error reset, follow the minimum operating voltage) is always enabled. Please refer to "POR v.s. SXT32K Min. Operating Voltage" characteristic curve.*

2. **Timepiece Current (CPU Off, LCD On, 32K crystal oscillating) :**

   P8620: 7uA @V_{DD}=3V, V_{BAT}=3V, without power saving

   P8620: 3uA @V_{DD}=1.5V, V_{BAT}=3V, with power saving

   P8625: 2uA(1/2bias) or 4uA(1/3bias) @V_{DD}=1.5V, V_{BAT}=1.5V

   P8640: 5uA @V_{DD}=3V, V_{BAT}=3V, without power saving

   P8640: 3uA @V_{DD}=1.5V, V_{BAT}=3V, with power saving

   P8645: 2uA(1/2bias) or 4uA(1/3bias) @V_{DD}=1.5V, V_{BAT}=1.5V

3. **Program ROM:**

   P8620: 2K x 14 bit OTP

   P8625: 2K x 14 bit OTP

   P8640: 4K x 14 bit OTP

   P8645: 4K x 14 bit OTP

4. **RAM:**

   P8620: 176 bytes

   P8625: 176 bytes

   P8640: 336 bytes

   P8645: 336 bytes

5. **STACK: 6 Levels**

6. **System Oscillation Sources (Fsys) :**

   - Fast-clock
     - FIRC (Fast Internal RC) : 2.7MHz @V_{DD}=3V; 0.9MHz @V_{DD}=1.5V
   - Slow-clock
     - SIRC (Slow Internal RC) : 36KHz @V_{DD}=3V; 32KHz @V_{DD}=1.5V
     - SXT (Slow Crystal) : 32768 Hz
   - System Oscillation Sources can be divided by 1/2/4/8 as System Clock (Fsys)

- Dual System Clock Switching between Fast-clock and Slow-clock
  - FIRC + SIRC
  - FIRC + SXT

7. Power Saving Operation Mode

- FAST Mode: CPU running at Fast-clock
- SLOW Mode: CPU running at Slow-clock
- IDLE Mode: Fast-clock and CPU stop; Slow-clock, Timer2 and LCD keep running
- STOP Mode: All clocks stop

8. Resistance to Frequency Converter (RFC)

9. Three Independent Timers

- Timer0 (TM0)
  - 8-bit timer with divided by 1~256 pre-scale option, counter/reload/interrupt/stop/capture function
  - Clock sources: Fsys or Slow-clock (SIRC/SXT) /1/4/16/64
- Timer1 (TM1)
  - 8-bit timer with divided by 1~256 pre-scale option, reload/interrupt/stop/capture/clear function
  - Clock source: Fsys
- Timer2 (T2)
  - 21-bit timer with 4 interrupt time period options (60s/1s/0.5s/0.125s)
  - Clock sources: Fsys /128 or Slow-clock (SIRC/SXT)
  - IDLE mode wake-up, if clock source is Slow-clock

10. Interrupts

- Three External Interrupt pins (INT0~INT2)
  - Rising or falling edge triggered interrupt
- Timer0/Timer1/Timer2 Interrupts
- PWM0 Interrupt
- RFC overflow Interrupt
- LBD overflow Interrupt

11. Wake up

- External Interrupt pins (INT0~INT2) can wake up CPU in IDLE/STOP mode.
- PB [7:0] low-level can wake up CPU in IDLE/STOP mode.
- Timer2 Interrupt can wake up CPU in IDLE mode if Timer2 clock source is Slow-clock.
- PWM0 Interrupt can wake up CPU in IDLE mode if PWM0 clock source is Slow-clock.

12. LCD Controller / Driver

- Four LCD brightness adjustable (only use in 1/3 bias)
- 1/3 duty or 1/4 duty option

- P8620：

  MAX: 12 SEG x 4 COM,

  1/3 LCD Biasvoltage, typical value is VL1=1.0V, VL2=2.0V, 和 V_{LCD}=3.0V

- P8625：

  MAX: 10 SEG x 4COM,

  1/3 LCD Bias voltage, typical value is VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

  1/2 LCD Bias voltage, typical value is VL1=1.5V 和 V_{LCD}=3.0V

- P8640：

  MAX: 28 SEG x 4 COM,

  1/3 LCD Biass voltage, typical value is VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

- P8645：

  MAX: 26 SEG x 4 COM,

  1/3 LCD Bias voltage, typical value is VL1=1.0V, VL2=2.0V, and V_{LCD}=3.0V

  1/2 LCD Bias voltage, typical value is VL1=1.5V 和 V_{LCD}=3.0V

13. Watchdog Timer (WDT)

- Clocked by system clock with 2 adjustable reset times, 2^{16}/Fsys or 2^{15}/Fsys
  - 1.8sec/0.9sec @V_{DD}=3V (Fsys = SIRC)
  - 2.0sec/1.0sec @V_{DD}=1.5V (Fsys = SIRC)
- Watchdog timer is disabled in IDLE/STOP mode

14. Two 8-bit PWMs for Buzzer / IR application (PWM0&PWM1)

- Adjustable Period & Clock Pre-scale
- Clock sources: Fast-clock or Slow-clock
- PWM0 output amplitude can be doubled (only for P8625 and P8645)

15. Four types Reset

- Power On Reset/Low Voltage Reset (POR)

  P8620:1.6V@25℃

  P8625:1.1V@25℃

  P8640:1.6V@25℃,

  P8645:1.1V@25℃

- ROM check Reset (LVCR)

  Follow the minimum operating voltage and always enable.

- External Pin Reset (INT0~INT2)
- Watchdog Reset (WDT)

16. Low Battery Detector (LBD) by BandGap Voltage Reference

P8620: Detect V_{BAT} from 2.4V to 3.0V

P8625: Detect V_{BAT} from 1.2V to 1.5V @LCDON=1

P8640: Detect V_{BAT} from 2.4V to 3.0V

P8645: Detect V_{BAT} from 1.2V to 1.5V @LCDON=1

17. Operating Temperature Range :

P8620: -40℃ to + 85℃

P8625: -40℃ to + 85℃

P8640: -40℃ to + 85℃

P8645: -40℃ to + 85℃

18. Package Type :

P8620: Dice-form / SOP28

P8625: Dice-form / SOP28

P8640: Dice-form / SSOP48 / LQFP48

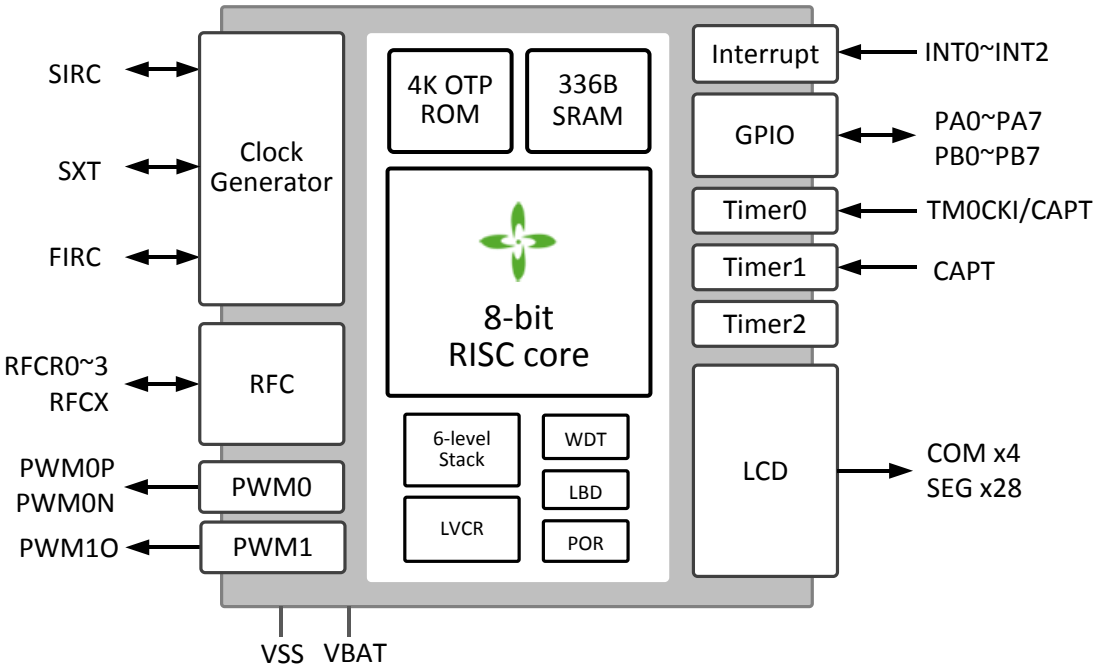
P8645: Dice-form / SSOP48 / LQFP48

19. Supported EV board on ICE

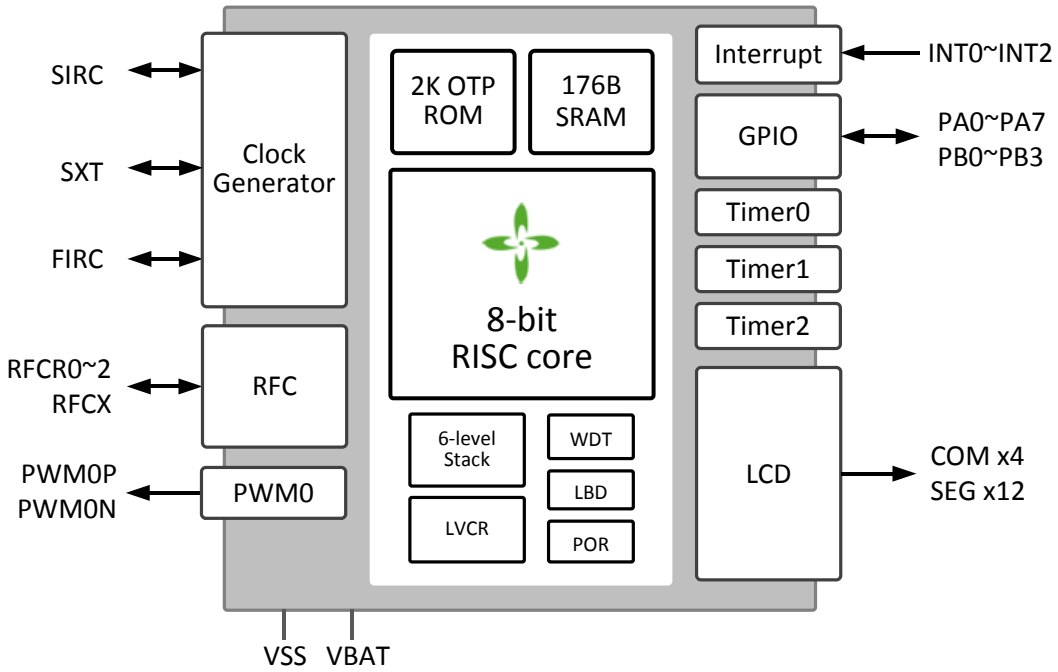
EV board: EV8228

EV8228 does not support the interrupt of low battery detection (LBD), RFC1T architecture, HIX2 function and IAP function.

BLOCK DIAGRAM

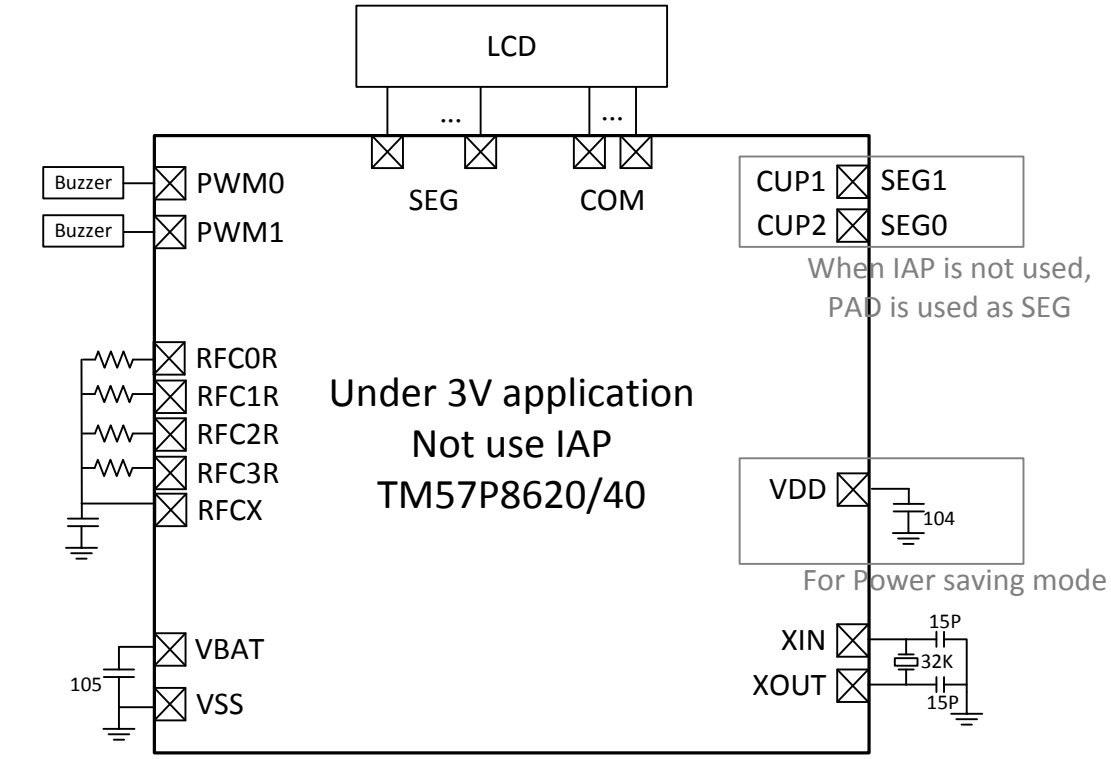


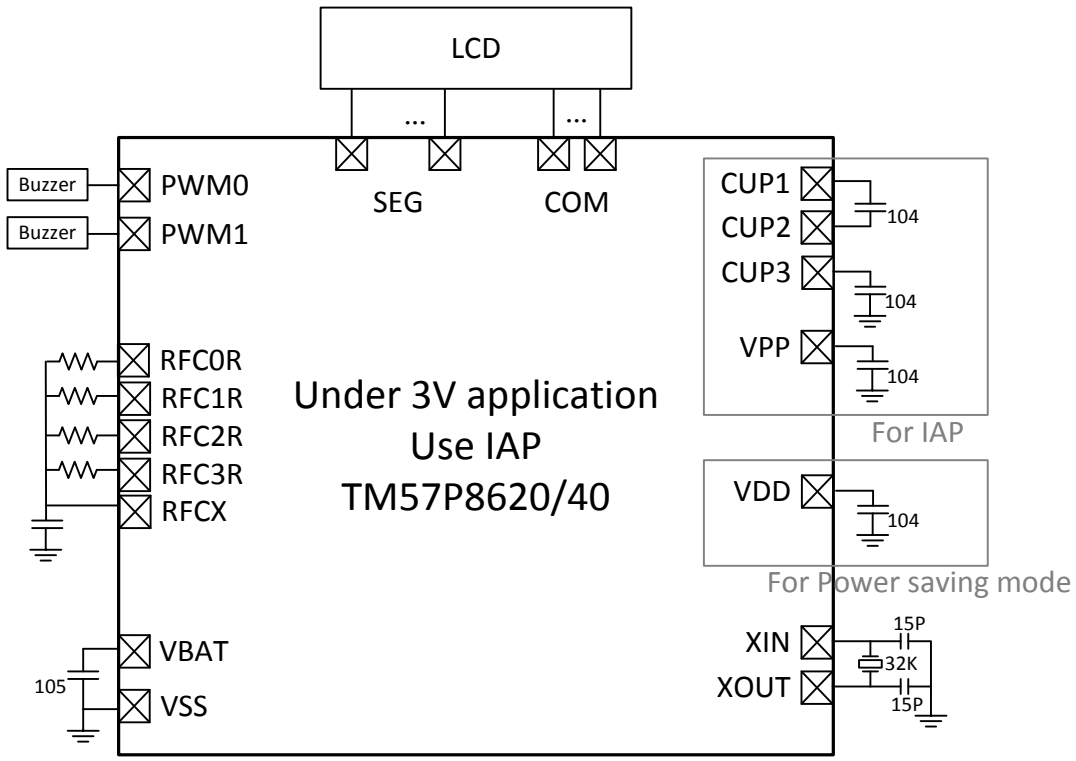
TM57P8640/45

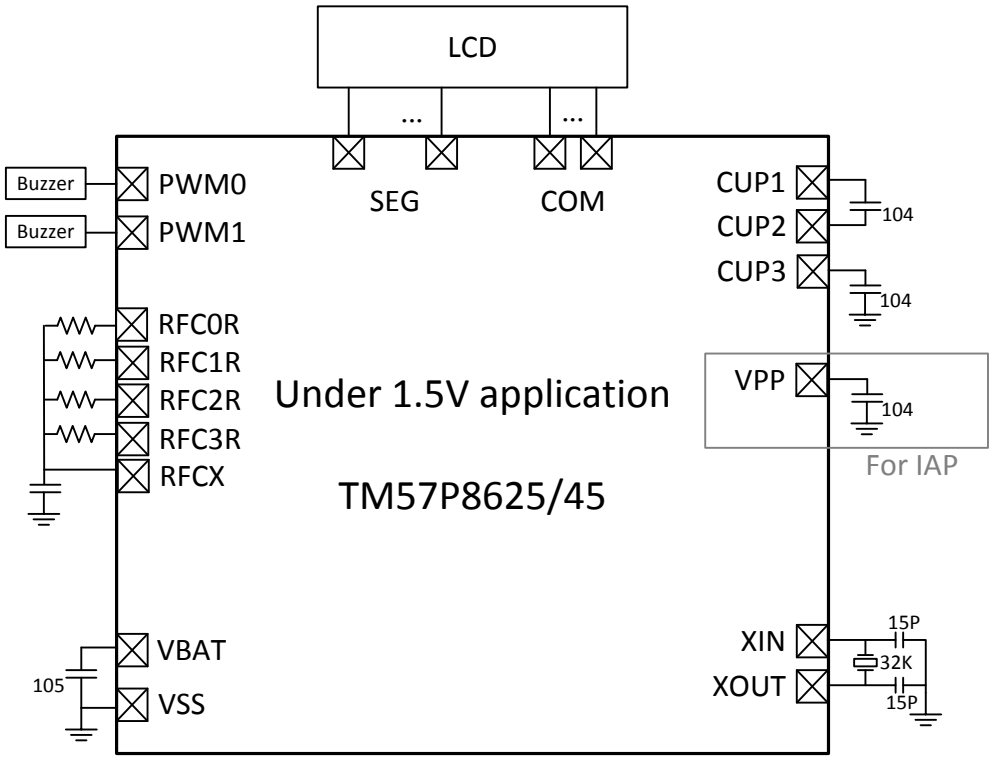


TM57P8620/25

APPLICATION CIRCUIT



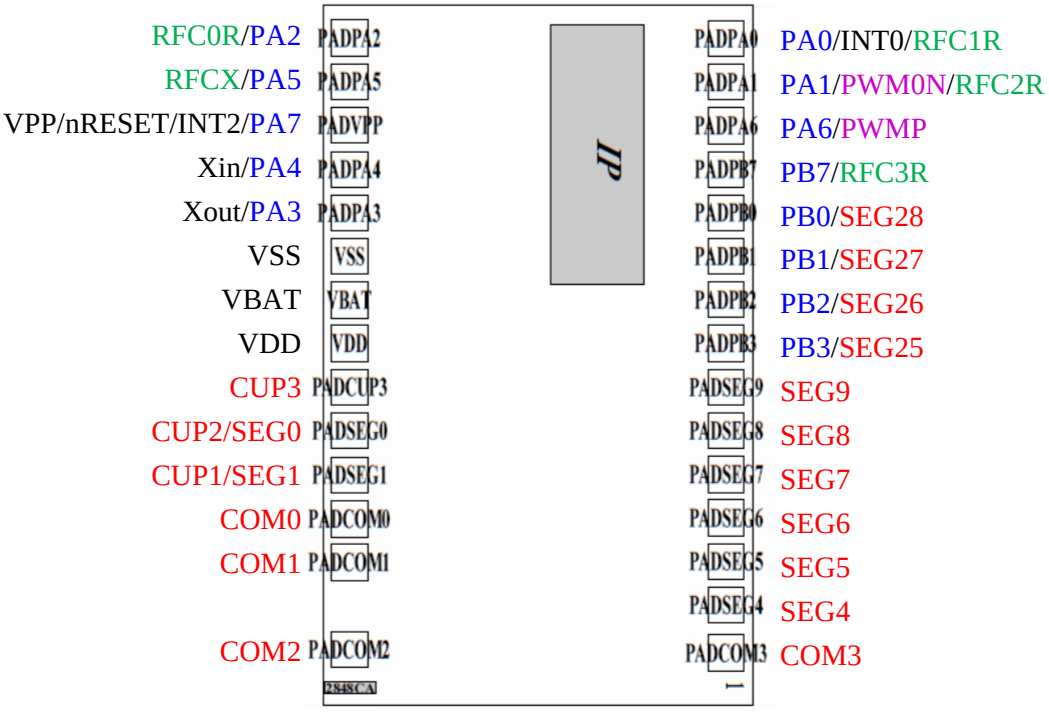




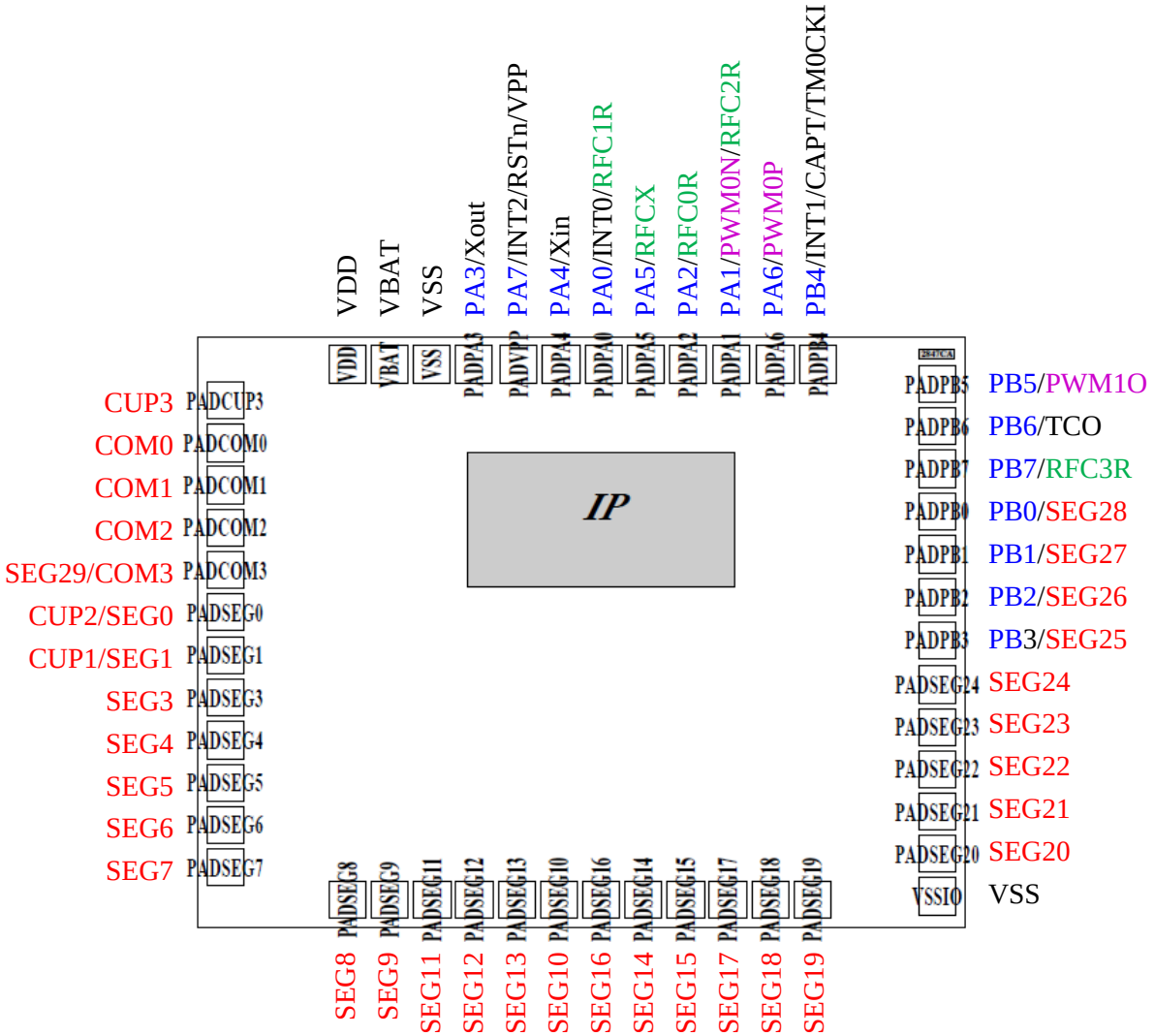
*P8625/45 can boost to 3V by plug-in for IAP.

DIE PAD LIST

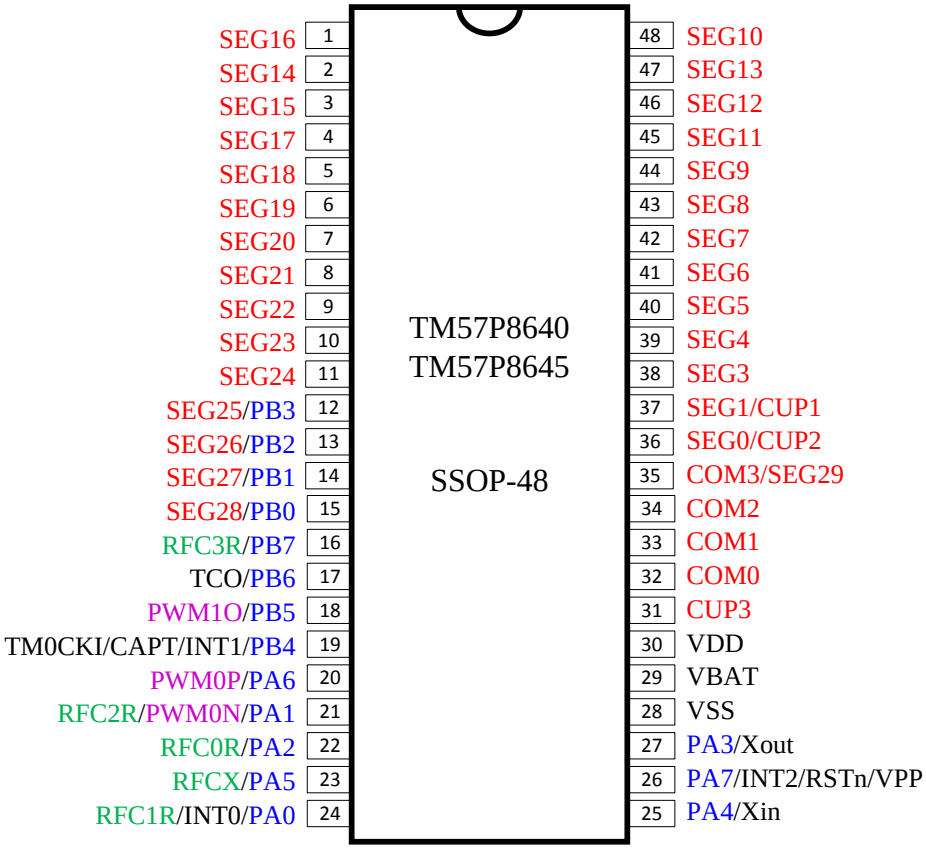
TM57P8620/TM57P8625:

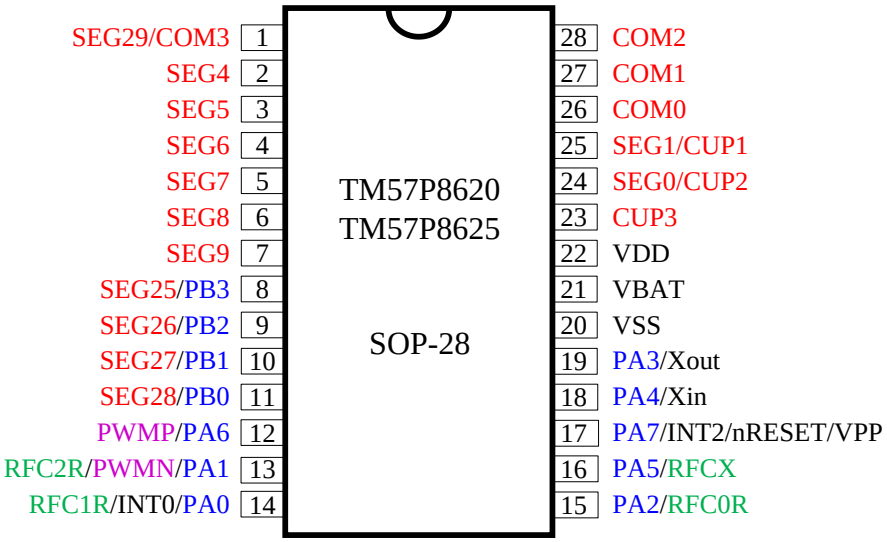


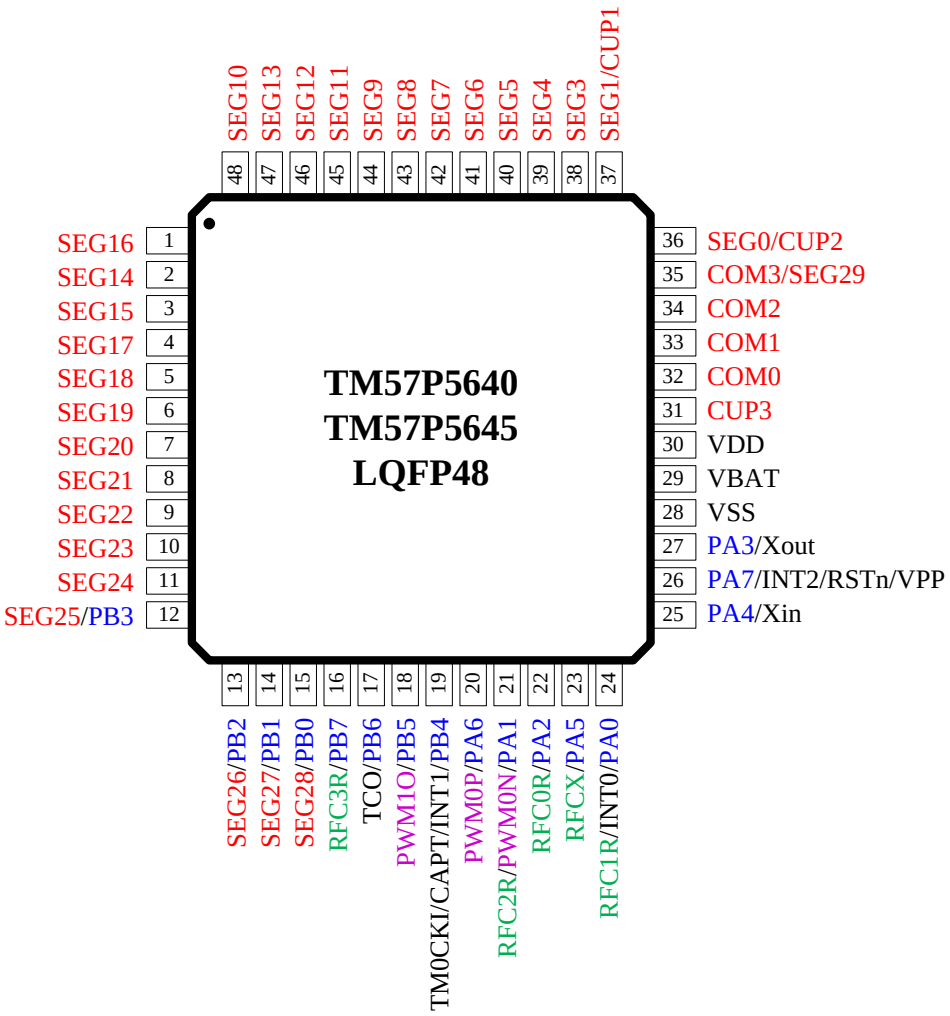
TM57P8640/TM57P8645:



PIN ASSIGNMENT






TM57P5640
TM57P5645
LQFP48
1 SEG16
2 SEG14
3 SEG15
4 SEG17
5 SEG18
6 SEG19
7 SEG20
8 SEG21
9 SEG22
10 SEG23
11 SEG24
12 SEG25/PB3
13 SEG26/PB2
14 SEG27/PB1
15 SEG28/PB0
16 RFC3R/PB7
17 TCO/PB6
18 PWM1O/PB5
19 TM0CKI/CAPT/INT1/PB4
20 PWM0P/PA6
21 RFC2R/PWM0N/PA1
22 RFC0R/PA2
23 RFCX/PA5
24 RFC1R/INT0/PA0
25 PA4/Xin
26 PA7/INT2/RSTn/VPP
27 PA3/Xout
28 VSS
29 VBAT
30 VDD
31 CUP3
32 COM0
33 COM1
34 COM2
35 COM3/SEG29
36 SEG0/CUP2
37 SEG1/CUP1
38 SEG3
39 SEG4
40 SEG5
41 SEG6
42 SEG7
43 SEG8
44 SEG9
45 SEG11
46 SEG12
47 SEG13
48 SEG10

PIN DESCRIPTIONS

Name	In/Out	Pin Description
PA0–PA6	I/O	Bit-programmable I/O port for Schmitt-trigger input, “CMOS push-pull” output or “Open-Drain” output. Pull-up Resistors are assignable by software.
PA7	I/O	Bit-programmable I/O port for Schmitt-trigger input, or “Open-Drain” output. Pull-up resistors are assignable by software.
PB0–PB3	I/O	Bit-programmable I/O port for Schmitt-trigger input, “CMOS push-pull” output or “Open-Drain” output.
PB4–PB7	I/O	Bit-programmable I/O port for Schmitt-trigger input, “CMOS push-pull” output or “Open-Drain” output. Pull-up Resistors are assignable by software.
nRESET	I	External active low reset with internal pull-high
INT0–INT2	I	External interrupt input
TCOUT	O	Instruction cycle clock output. The instruction clock frequency is system clock frequency divided by two (Fsys/2)
TM0CKI	I	Timer0’s input in counter mode
CAPT	I	Timer0/Timer1 Capture input
RFC0R~RFC3R	O	RFC resistor connection pin
RFCX	I	RFC clock input pin
COM0~COM3	O	LCD common output
SEG0~SEG1, SEG3~SEG29	O	LCD segment output
PWM0P, PWM0N	O	8-bit PWM0 output
PWM1O	O	8-bit PWM1 output
CUP1, CUP2, CUP3	–	Used for IAP pump capacitor connection pin or used for 1.5V LCD pump capacitor connection pin
XIN, XOUT	–	Crystal / Resonator oscillator connection for system clock.
VDD	P	Internal voltage pin output
VPP	I	ROM programming high voltage input
VBAT, VSS	P	Power Voltage input pin and ground

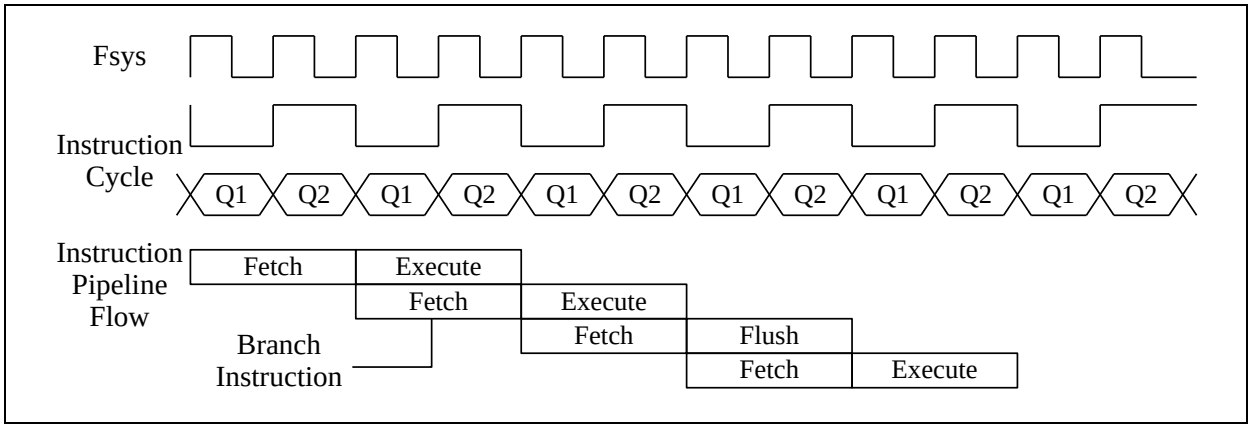
Note: Programming pins are list below. It is better to remove the PCB components connected to these pins during In-Circuit-Programming.
7 wire mode: VBAT/VSS/PA0/PA1/PA3/PA4/PA7 (VPP)
6 wire mode: VBAT/VSS/PA0/PA1/PA4/PA7 (VPP)

FUNCTIONAL DESCRIPTION

1. CPU Core

Clock Scheme and Instruction Cycle

The system clock is internally divided by two to generate Q1 state and Q2 state for each instruction cycle. The Programming Counter (PC) is updated at Q1 and the instruction is fetched from program ROM and latched into the instruction register in Q2. It is then decoded and executed during the following Q1-Q2 cycle. Branch instructions take two cycles since the fetch instruction is 'flushed' from the pipeline, while the new instruction is being fetched and then executed.



ALU and Working (W) Register

The ALU is 8-bit wide and capable of addition, subtraction, shift and logical operations. In two-operand instructions, typically one operand is the W register, which is an 8-bit non-addressable register used for ALU operations. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either W register or a file register. Depending on the instruction executed, the ALU may affect the values of Carry (C), Digit Carry (DC), and Zero (Z) Flags in the STATUS register. The C and DC flags operate as a /Borrow and /Digit Borrow, respectively, in subtraction.

Note: /Borrow represents inverted of Borrow register.

/Digit Borrow represents inverted of Digit Borrow register.

Programming Counter (PC) and Stack

The Programming Counter is 12-bit wide capable of addressing a 2K x 14 (P8620/P8625) or 4K x 14 (P8640/ P8645) ROM. As a program instruction is executed, the PC will contain the address of the next program instruction to be executed. The PC value is normally increased by one except the followings. The Reset Vector (000h) and the Interrupt Vector (001h) are provided for PC initialization and Interrupt. For CALL / GOTO instructions, PC loads 12 bits address from instruction word. For RET / RETI / RETLW instructions, PC retrieves its content from the top level STACK. For the other instructions updating PC [7:0], the PC [11:8] keeps unchanged. Therefore, the data of a lookup table must be located with the same PC [11:8].

The STACK is 12-bit wide and 6-level in depth. The CALL instruction and hardware interrupt will push STACK level in order. While the RET / RETI / RETLW instructions pop the STACK level in order.

For table lookup, the device offers the powerful table read instructions TABRL, TABRH to return the 14-bit ROM data into W register by setting the DPTR = {DPH, DPL} registers in F-Plane.

◇Example: To look up the ROM data located "TABLE"

```
        ORG     000H        ; Reset Vector
        GOTO    START       ; Goto user program address
START:
        MOVLW   00H
        MOVWF   INDEX       ; Set lookup table's address (INDEX)
LOOP:
        MOVFW   INDEX       ; Move INDEX value to W register
        CALL    TABLE       ; To Lookup data (W = 55H when INDEX = 00H)
        …
        INCF    INDEX, 1    ; Increment the INDEX for next address
        …
        GOTO    LOOP        ; Goto LOOP label

        ORG     X00H        ; X = 1, 2, 3, …, E, F
TABLE:
        ADDWF   PCL, 1      ; (Addr = X00H) Add the W with PCL, the result
                            ; back in PCL
        RETLW   55H         ; W = 55H when return
        RETLW   56H         ; W = 56H when return
        RETLW   58H         ; W = 58H when return
```

Note: The chip defines 256 ROM addresses as one page, so that ROM has sixteen pages, 000H~0FFH, 100H~1FFH, 200H~2FFH, …, and F00H~FFFH. On the other words, PC[11:8] can be defined as page. A lookup table must be located at the same page to avoid getting wrong data. Thus, the lookup table has maximum 255 data for above example with starting a lookup table at X00H (X = 1, 2, 3, …, E, F). If a lookup table has fewer data, it needs not setting the starting address at X00H, but only confirms all lookup table data are located at the same page.

◇Example: To look up the ROM data located "TABLE" by TABRL and TABRH instructions

```
        ORG     000H            ; Reset Vector
        GOTO    START           ; Goto user program address
START:
        MOVLW   (TABLE >>8) & 0xff  ; Get high byte address of TABLE label
        MOVWF   DPH             ; DPH (F1E.3~0) = 02H
        MOVLW   (TABLE) & 0xff  ; Get low byte address of TABLE label
        MOVWF   DPL             ; DPL (F1D.7~0) = 80H
LOOP:
        TABRL                   ; W = 86H when DTPR = {DPH, DPL} = 0280H
        TABRH                   ; W = 19H when DTPR = {DPH, DPL} = 0280H
        …
        INCF    DPL, 1          ; Increment the DPL for next address
        …
        GOTO    LOOP            ; Goto LOOP label

        ORG     280H
TABLE:
        DT      0x1986          ; 14-bit ROM data
```

```
DT          0x3719          ; 14-bit ROM data
```

F02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCL	PCL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F02.7~0 **PCL:** Low-byte of Program Counter (PC[7:0])

F0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PCH	–	–	–	–	PCH			
R/W	–	–	–	–	R	R	R	R
Reset	–	–	–	–	0	0	0	0

F0A.3~0 **PCH:** 4 MSBs of Program Counter (PC[11:8])

F1D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPL	DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F1D.7~0 **DPL:** Table read low address, data ROM pointer (DPTR[7:0])

F1E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DPH	–	–	–	–	DPH			
R/W	–	–	–	–	R/W	R/W	R/W	R/W
Reset	–	–	–	–	0	0	0	0

F1E.3~0 **DPH:** 4 MSBs of Table read high address, data ROM pointer (DPTR[11:8])

STATUS Register (F-Plane 03H)

This register contains the arithmetic status of ALU and the reset status. The STATUS register can be the destination for any instruction, as with any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. It is recommended, therefore, that only BCF, BSF and MOVWF instructions are used to alter the STATUS register because these instructions do not affect those bits.

F03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	GB2	GB1	RAMBK	TO	PD	Z	DC	C
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Description	
7	**GB2**: General Purpose Bit 2	
6	**GB1**: General Purpose Bit 1	
5	**RAMBK:** RAM Bank Selection 0: FRAM Bank0 1: FRAM Bank1	
4	**TO**: Time Out Flag 0: after Power On Reset, POR Reset, or CLRWDT/SLEEP instruction 1: WDT time out occurs	
3	**PD**: Power Down Flag 0: after Power On Reset, POR Reset, or CLRWDT instruction 1: after SLEEP instruction	
2	**Z**: Zero Flag 0: the result of a logic operation is not zero 1: the result of a logic operation is zero	
1	**DC**: Decimal Carry Flag or Decimal/Borrow Flag	
	ADD instruction	SUB instruction
	0: no carry 1: a carry from the low nibble bits of the result occurs	0: a borrow from the low nibble bits of the result occurs 1: no borrow
0	**C**: Carry Flag or/Borrow Flag	
	ADD instruction	SUB instruction
	0: no carry 1: a carry occurs from the MSB	0: a borrow occurs from the MSB 1: no borrow

◇Example: Write immediate data into STATUS register

```
MOVLW   00H
MOVWF   STATUS          ; Clear STATUS register
```

◇Example: Bit addressing set and clear STATUS register

```
BSF     STATUS, 0       ; Set C = 1
BCF     STATUS, 0       ; Clear C = 0
```

◇Example: Determine the C flag by BTFSS instruction

```
BTFSS    STATUS, 0      ; Check the C flag
GOTO     LABEL_1        ; If C = 0, goto LABEL_1 label
GOTO     LABEL_2        ; If C = 1, goto LABEL_2 label
```

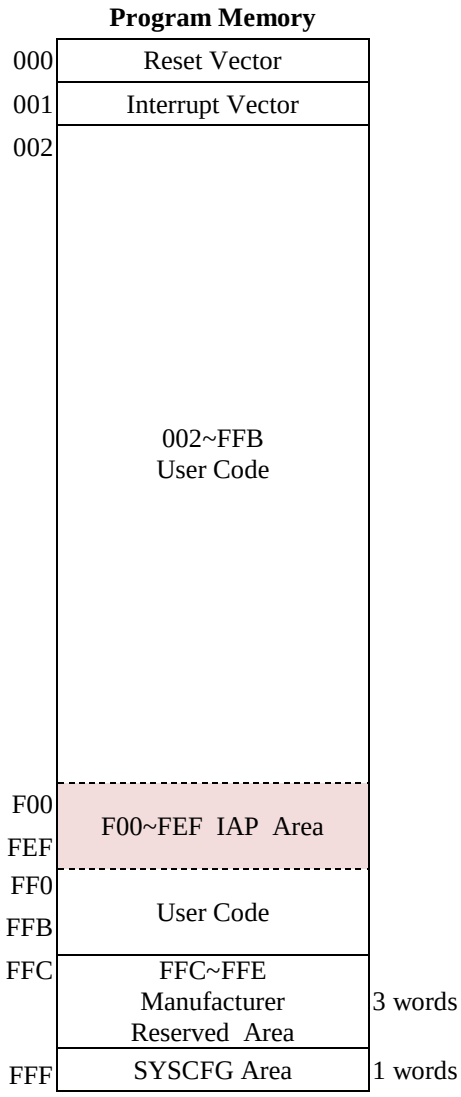
2. Program ROM

P8640/45 support 4K OTP ROM, P8620/25 support 2K OTP ROM, the last 4 words are reserved for production records (chip ID, factory number, checksum) and system settings (SYSCFG).

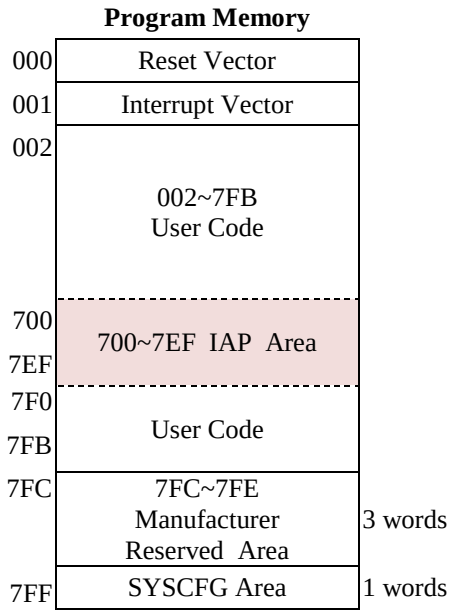
The initial value of OTP (One-time Programmable) ROM is 1, and it can be programmed to 0. When there is a need for reprogramming, UV erase is required before rewriting.

In the User code area, a small area is planned to be used as an IAP area at the same time (240 words). After reset, the system will restart the program counter (PC) at address 000H, and all registers will be restored to default values. When an interrupt occurs, the program counter (PC) will be pushed onto the stack (Stack) and jump to address 001H.

P8640/45: 4K ROM



P8620/25: 2K ROM



3. System Configuration Register (SYSCFG)

The system configuration register (SYSCFG) of this chip is placed at the last address of ROM: P8640/45 is located at FFFh, and P8620/25 is located at 7FFh. The system configuration register (SYSCFG) option is used to determine the initial conditions of the MCU. The user can select the chip working mode through the SYSCFG register.

bit	Description	
13	**nPROT**: Code protection selection	
	1	Disable
	0	Enable. If code is protected, writer can not access the ROM code
12	**nXRSTE**:External Pin (PA7) Reset select	
	1	Disable (PA7 as input I/O pin)
	0	Enable
11	**PORSEL**: Low voltage reset select	
	1	POR 1.1V，disable in IDLE / STOP mode（for P8625/45）
	0	POR 1.6V，disable in IDLE / STOP mode（for P8620/40）
9	**nWDTE**: WDT Reset select	
	1	Disable
	0	Enable in FAST / SLOW mode，disable in IDLE / STOP mode
8~6	Tenx reserved	
5	**nIAPE**: IAP select	
	1	Disable
	0	Enable
4~0	**SRC_TRIM**: 5-bit SIRC trim.	

System Configuration Register (SYSCFG)

4. IAP

This chip is OTP ROM, IAP function can only be written once, not EEPROM.

The environmental limitations of the IAP function of this chip are as follows:

(1) The system clock (Fsys) is the fast clock divided by one (FIRC/1)

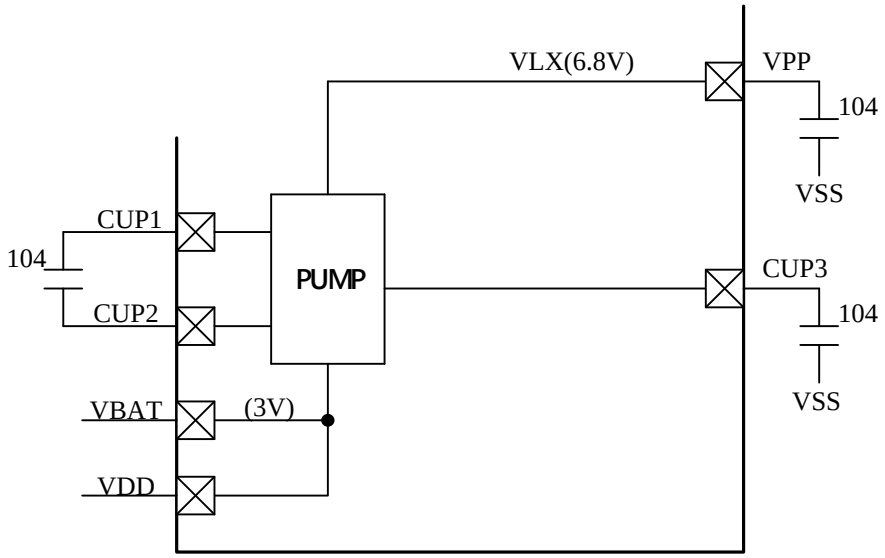
(2) VBAT=3~3.3V (P8625/45 users can boost to 3V by plug-in)

Before using IAP, please turn on IAPEN (SFR R15). It is recommended to turn off IAPEN (SFR R15) when IAP is not used.

P8640/45 planned IAP location is in ROM address F00~FEFh

P8620/25 planned IAP location is at ROM address 700~7EFh

The nIAPE bit in the system configuration register (SYSCFG) determines whether the IAP function is turned on, and the address selection is foolproof. When the address points to the planned IAP location , it will actually write.



IAP application circuit

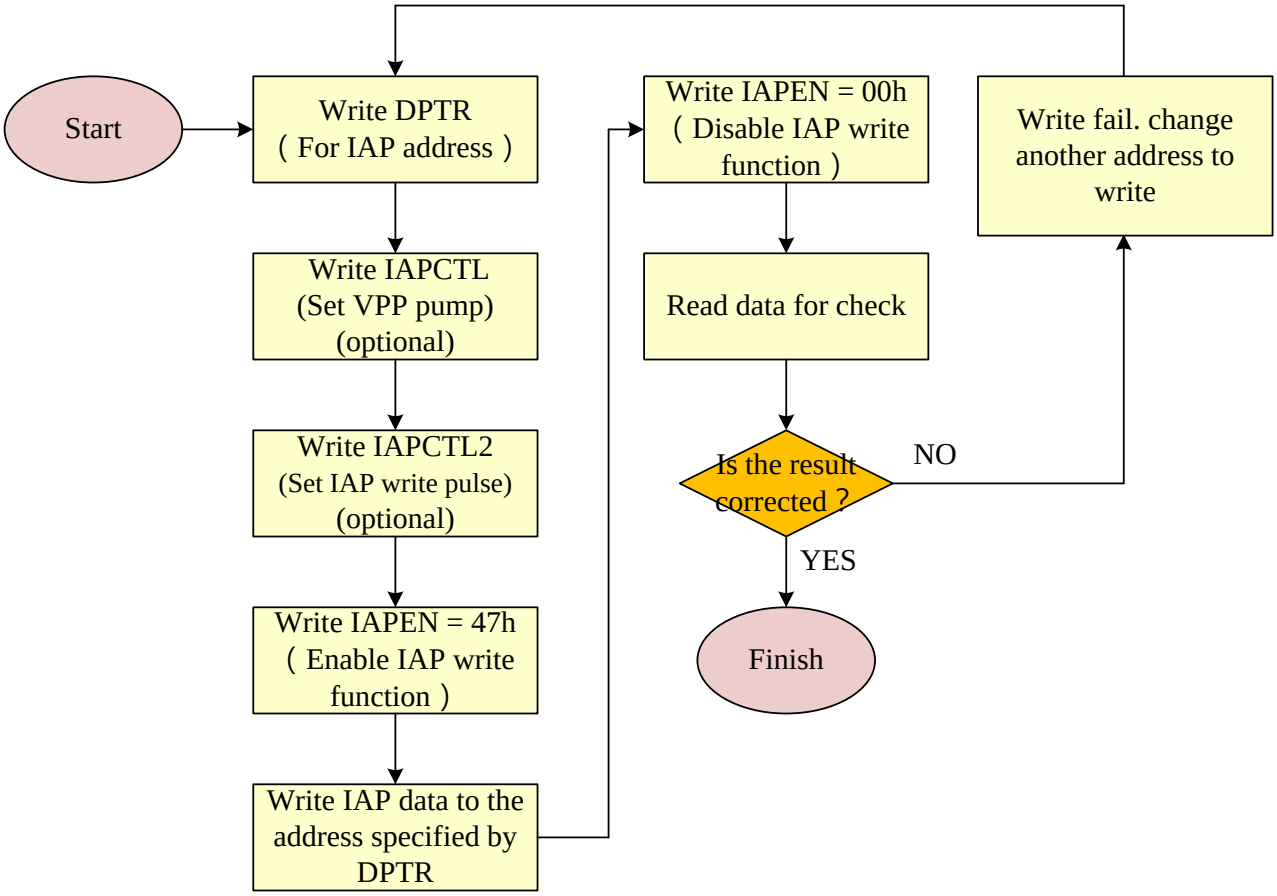
IAP sample program:

```
movlw   60h
movwr   IAPCTL
movlw   03h
movwr   IAPCTL2

movlw   0x0f
movwf   DPH             ;address setting
movlw   0x00
movwf   DPL             ;address setting

movlw   0x47
movwr   IAPEN

movlw   0x5a
movwr   IAPDATA         ;write 0x5a to the ROM at address 0x0f00
tabrh                   ;check
tabrl                   ;check
```


Start
Write DPTR
（For IAP address）
Write IAPCTL
(Set VPP pump)
(optional)
Write IAPCTL2
(Set IAP write pulse)
(optional)
Write IAPEN = 47h
（Enable IAP write
function）
Write IAP data to the
address specified by
DPTR
Write IAPEN = 00h
（Disable IAP write
function）
Read data for check
Is the result
corrected ?
NO
YES
Finish
Write fail. change
another address to
write

R13	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCTL		SV					IAPCKS	
R/W		R/W					R/W	
复位		0	1	1			0	1

R13.6~4 **SV:** Select VPP pump voltage ratio for IAP
(VPP recommended voltage: 6.75V)
0: VPP= 1.83*VBAT 4: VPP= 2.07*VBAT
1: VPP= 1.88*VBAT 5: VPP= 2.15*VBAT
2: VPP= 1.94*VBAT 6: VPP= 2.25*VBAT
3: VPP= 2.00*VBAT 7: VPP= 2.36*VBAT

R13.1~0 **IAPCKS**: Select VPP pump clock source for IAP
(IAPCKS recommended value is 0)
0: VPP pump clock source is FIRC/16
1: VPP pump clock source is FIRC/32
2: VPP pump clock source is FIRC/64
3: VPP pump clock source is FIRC/128

R14	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPCTL2						WR_PULSE		
R/W						R/W		
复位						0	1	1

R14.2~0 **WR_PULSE:** Adjust the pulse width of ROM IAP write signal
(When VCC=3V, the recommended value of WR_PULSE is 3)
(When VCC=3.2V, the recommended value of WR_PULSE is 4)
0: The pulse width of the write signal is the shortest
……
7: The pulse width of the write signal is the longest

R15	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPEN	IAPEN							
R/W	W							R/W
复位	-	-	-	-	-	-	-	0

R15.7~0 **IAPEN:** IAP function switch
Write 47h to enable the IAP function,
Write a value other than 47h to turn off the IAP function

R15.0 **IAPFLG:** IAPEN flag that can be read

R16	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IAPDATA	IAPDATA							
R/W	R/W							
复位	0	0	0	0	0	0	0	0

R16.7~0 **IAPDATA:** Implement IAP by moving the value you want to write to IAPDATA
(IAP address=DPTR)

5. Data Memory (SRAM and SFR)

The data memory of this chip is divided into two blocks, F-Plane and R-Plane.

F-Plane

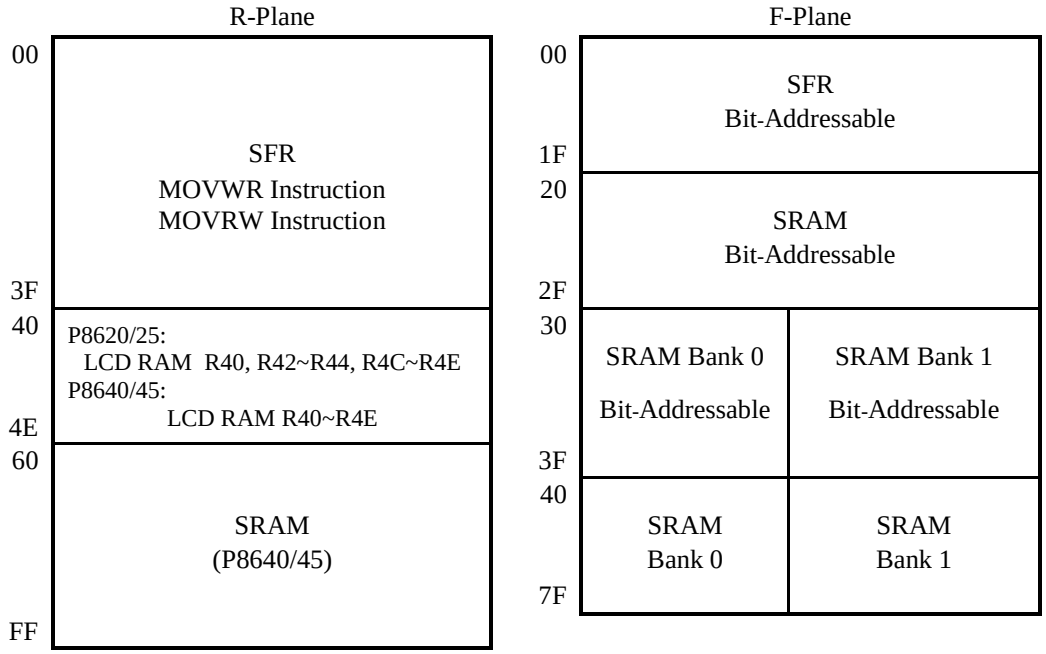
The low position of F-Plane is defined to the special function register (SFR), and the high position is defined to SRAM as general-purpose data memory. In addition to direct addressing, indirect addressing is also supported. The INDF register can be used for indirect addressing. The INDF is a virtual register. It uses the value in the FSR register (FSR is a data pointer) as an address and points to the register at that address.

The first half of F-Plane (00~3F) can support Bit-Addressable.

R-Plane

The low position of R-Plane is defined to the special function register (SFR), and the high position is defined to SRAM as general-purpose data memory. In addition to direct addressing, indirect addressing is also supported. The INDR register can be used for indirect addressing. The INDR is a virtual register. It uses the value in the RSR register (RSR is a data pointer) as an address and points to the address register.

R-Plane does not support bit addressing, and R-Plane only supports MOVWR and MOVRW byte operation instructions.



F-Plane	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
00h	INDF	TM0	PCL	STATUS	FSR	PAD	PBD	
08h	INTIE	INTIF	PCH	CLKCTL	MF0C	PWM0D	LBDCTL	RFCTL
10h	LCDCTL	RFCNTH	RFCNTL	PWM1D	TM1	PWMCLR	LBDIE	LBDIF
18h					RSR	DPL	DPH	

R-Plane	8/0	9/1	A/2	B/3	C/4	D/5	E/6	F/7
00h	INDR	TM0RLD	TM0CTL	PWRDN	WDTCLR	PAMODH	PAMODL	PBMODH
08h	PBMODL		PWM0CTL	PWM0PRD	PWM1CTL	PWM1PRD		
10h	TM1RLD	TM1CTL	PBWKEN	IAPCTL	IAPCTL2	IAPEN	IAPDATA	
18h								POROFF
40h	LCDRAM							
4eh	LCDRAM							

◇Example: Write immediate data into R-Plane register

```
MOVLW   AAH     ; Move immediate AAH into W register
MOVWR   05H     ; Move W value into R-Plane location 05H
```

◇Example: Move R-Plane location 20H data into W register

```
MOVRW   20H     ; To get a content of R-Plane location 20H to W
```

◇Example: Clear R-Plane by indirectly addressing mode

```
        MOVLW   20H     ; W = 20H
        MOVWF   RSR     ; Set R-Plane address to RSR register
LOOP:
        MOVLW   00H
        MOVWR   INDR    ; Clear R-Plane 20H
```

◇Example: Clear F-Plane RAM data by indirectly addressing mode

```
        MOVLW   20H     ; W = 20H (SRAM start address)
        MOVWF   FSR     ; Set start address of user SRAM into FSR register
LOOP:
        MOVLW   00H
        MOVWF   INDF    ; Clear user SRAM data
        INCF    FSR, 1  ; Increment the FSR for next address
        MOVLW   80H     ; W = 80H (SRAM end address)
        XORWF   FSR, 0  ; Check the FSR is end address of user SRAM?
        BTFSS   STATUS, Z ; Check the Z flag
        GOTO    LOOP    ; If Z = 0, goto LOOP label
        …               ; If Z = 1, exit LOOP
```

F00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDF	INDF							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	–	–	–	–

F00.7~0 **INDF:** Not a physical register, addressing INDF actually point to the F-Plane register whose address is contained in the FSR register

F04	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FSR	GB3	FSR						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F04.7 **GB3:** General purpose bit 3

F04.6~0 **FSR:** F-Plane file select register, indirect address mode pointer

F1C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RSR	RSR							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F1C.7~0 **RSR:** R-Plane file select register, indirect address mode pointer

R00	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INDR	INDR							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	–	–	–	–	–	–	–

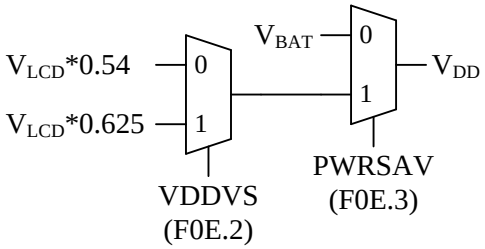
R00.7~0 **INDR:** Not a physical register, addressing INDR actually point to the R-Plane register whose address is contained in the RSR register

6. Power Management

Step-down power saving mode (only for P8620/40)

By setting PWRSAV (F0E.3), P8620/40 can use the step-down power saving mode function to reduce the internal voltage VDD to save power consumption. To use the buck power saving mode, the LCD bias must be set to 1/3.

As shown in the figure below, VBAT is the power supply of the chip, VDD is the internal voltage of the chip, and VLCD is 0.89~1 times of VBAT (VLCD voltage setting is determined by LCDBV. For more information, please refer to the LCD chapter). When PWRSAV is enabled, VDD is the divided voltage of VLCD, and the divided voltage can be selected as 0.54 or 0.625.



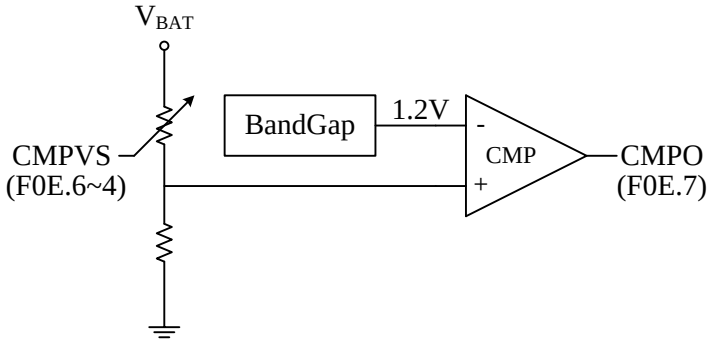
Power-save function

Low battery detection (LBD)

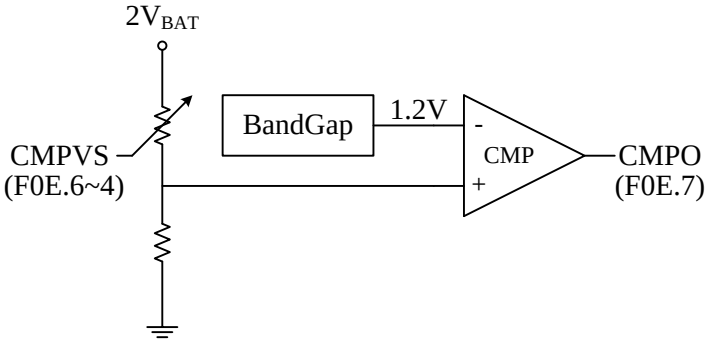
As shown in the figure below, the internal 1.2V bandgap reference provides an accurate voltage reference for the low battery detection (LBD) function. VBAT (P8620/40) or 2VBAT (P8625/45) is divided by a resistor to a certain level, and then The bandgap reference is compared. Bandgap references and comparators consume non-negligible currents, so users should not use them often. Because VBAT voltage levels change slowly, users can check them every hour or once a day to reduce current consumption.

P8625/45 must keep LCDON = 1 when using LBD function.

P8620/40:



P8625/45: (LCDON=1)



F0E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDCTL	CMPO	CMPVS			PWRSAV	VDDVS	PUMPCKS	PORPDF
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	–	0	0	0	0	0	0	–

F0E.7 **CMPO:** Low Battery Detector (LBD) result. CMP=0 means VBAT value is lower than the boundary selected by CMPVS.

Note: P8625/45 must turn on LCD for this function.

F0E.6~4 **CMPVS:** Low Battery Detector(LBD) options. Select V_{BAT}/V_{LCD} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage.

P8620/40:

000: Comparator and Bandgap Disable
001: detect if V_{BAT}>2.4V
010: detect if V_{BAT}>2.5V;
011: detect if V_{BAT}>2.6V;
100: detect if V_{BAT}>2.7V;
101: detect if V_{BAT}>2.8V;
110: detect if V_{BAT}>2.9V;
111: detect if V_{BAT}>3.0V;

P8625/45:

000: Comparator and Bandgap Disable
001: detect if V_{BAT}>1.20V
010:; detect if V_{BAT}>1.25V
011: detect if V_{BAT}>1.30V
100: detect if V_{BAT}>1.35V
101: detect if V_{BAT}>1.40V
110: detect if V_{BAT}>1.45V
111: detect if V_{BAT}>1.50V

F0E.3 **PWRSAV:** Power saving control for P8620/40. ***Note:*** P8625/45 must keep PWRSAV=0
0: Disable, $V_{DD}=V_{BAT}$
1: Enable, $V_{DD}=V_{LCD}$*0.54 or V_{LCD}*0.625

F0E.2 **VDDVS:** V_{DD} voltage selection. It actives while PWRSAV=1.
0: $V_{DD}=V_{LCD}$*0.54
1: $V_{DD}=V_{LCD}$*0.625

F16	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDIE								LBDIE
R/W								R/W
复位								0

F16.0 **LBDIE:** 低电量检测(LBD) 中断使能

0: 禁止

1: 使能

F17	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDIF								LBDIF
R/W								R/W
复位								0

F17.0 **LBDIF:** 低电量检测(LBD)中断旗标

当CMPO=0时由H / W设置LBDIF为1，通过S/W将0xFE写入LBDIF清除以该旗标，但当CMPO持续为0时，LBDIF无法被清除。

7. Reset

This chip has 4 reset methods, controlled by the system configuration register (SYSCFG). After reset, SFR returns to its default value, the program counter (PC) is cleared, and the system starts running from reset vector 000H. The TO and PD flags on the status register (STATUS) indicate the system reset status.

(1) Power-on reset/low voltage reset (POR)

The voltage threshold for this reset is determined by PORSEL in the SYSCFG register. When power on, it must be greater than the POR voltage value, FW can be disabled by setting SFR (POROFF)

-P8620/40: POR 1.6V

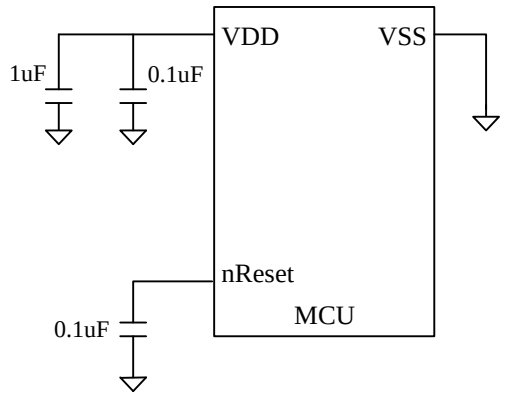
-P8625/45: POR 1.1V

(2) ROM error reset (LVCR)

Always be able to. When the low voltage causes the ROM value to read incorrectly, the chip will be reset, and the LVCR follows the minimum operating voltage.

(3) External pin reset (nRESET, PA7)

The external pin reset (nRESET) can be disabled or enabled through nXRSTE in the SYSCFG register. The external reset pin is active low and should be kept low for at least 2 SIRC clock cycles to ensure that the reset is active. External reset can reset the system during power-on. A good external reset circuit can protect the system from running under inappropriate power conditions.



(4) Watch dog reset (WDT)

The watchdog reset (WDT) can be disabled or enabled through nWDTE in the SYSCFG register. Setting WDTPSC can define the WDT reset generation period. The watchdog's clock is provided by the system clock (Fsys). It runs in FAST/SLOW mode and stops in IDLE/STOP mode. The WDT reset counter can be cleared by other resets or CLRWDT instructions.

-WDT period = 1.8sec/0.9sec @VDD=3V, Fsys = SIRC

-WDT period = 2.0sec/1.0sec @VDD=1.5V, Fsys = SIRC

F03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STATUS	GB2	GB1	RAMBK	TO	PD	Z	DC	C
R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W
Reset	0	0	0	–	–	0	0	0

F03.4 **TO:** WDT Time Out Flag
0: after Power On Reset, POR Reset, or CLRWDT / SLEEP instructions
1: WDT time out occurs

F03.3 **PD:** Power Down Flag
0: after Power On Reset, POR Reset, or CLRWDT instruction
1: after SLEEP instruction

R04	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WDTCLR	WDTCLR							
R/W	W							
Reset	–	–	–	–	–	–	–	–

R04.7~0 **WDTCLR:** Write this register to clear WDT (=CLRWDT instruction)

R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.0 **WDTPSC**: WDT Prescaler, 0: fsys/65536 1:fsys/32768

R1F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POROFF	POROFF							
R/W	W							R/W
Reset	–	–	–	–	–	–	–	0

R1F.7~0 **POROFF (W):** Write this register with 0x37 to force POR disable
R1F.0 **POROFF (R):** Flag indicates POR is forced to disable or not
1: POR is forced to disable

8. Clock Circuitry and Operation Mode

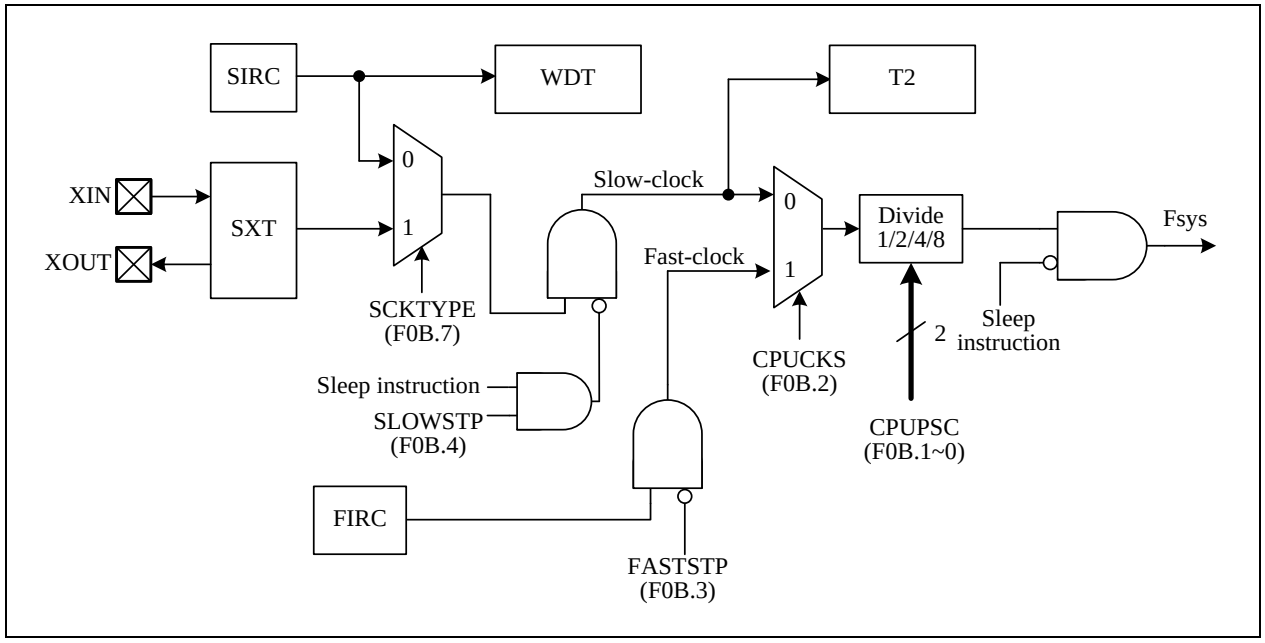
There are three kinds of system clock source.

(1) **SIRC** (Slow Internal RC, 36KHz @V_{DD}=3V, 32KHz @V_{DD}=1.5V)

(2) **SXT** (Slow Crystal, 32768Hz), recommended matching capacitors: two 15P capacitors

(3) **FIRC** (Fast Internal RC, 2.7MHz @V_{DD}=3V, 0.9MHz @V_{DD}=1.5V)

The device is designed with dual-clock system. During runtime, user can directly switch the System clock between Fast-clock (FIRC) and Slow-clock (SIRC or SXT). It also can directly select a clock divider of 1, 2, 4, or 8. The CLKCTL (F0B) SFR controls the System clock operating. H/W automatically blocks the S/W abnormally setting for this register. S/W can only change the Slow-clock type in Fast mode. Never to write both FASTSTP=1 & CPUCKS=1. It is recommended to write this SFR bit by bit.



Clock Scheme Block Diagram

There are four operation modes for this device.

SLOW Mode:

After power-on or reset, device enters SLOW mode. In this mode, the Fast-clock should be stopped (by FASTSTP=1, for power saving) and Slow-clock is enabled. The default Slow-clock is SIRC.

FAST Mode:

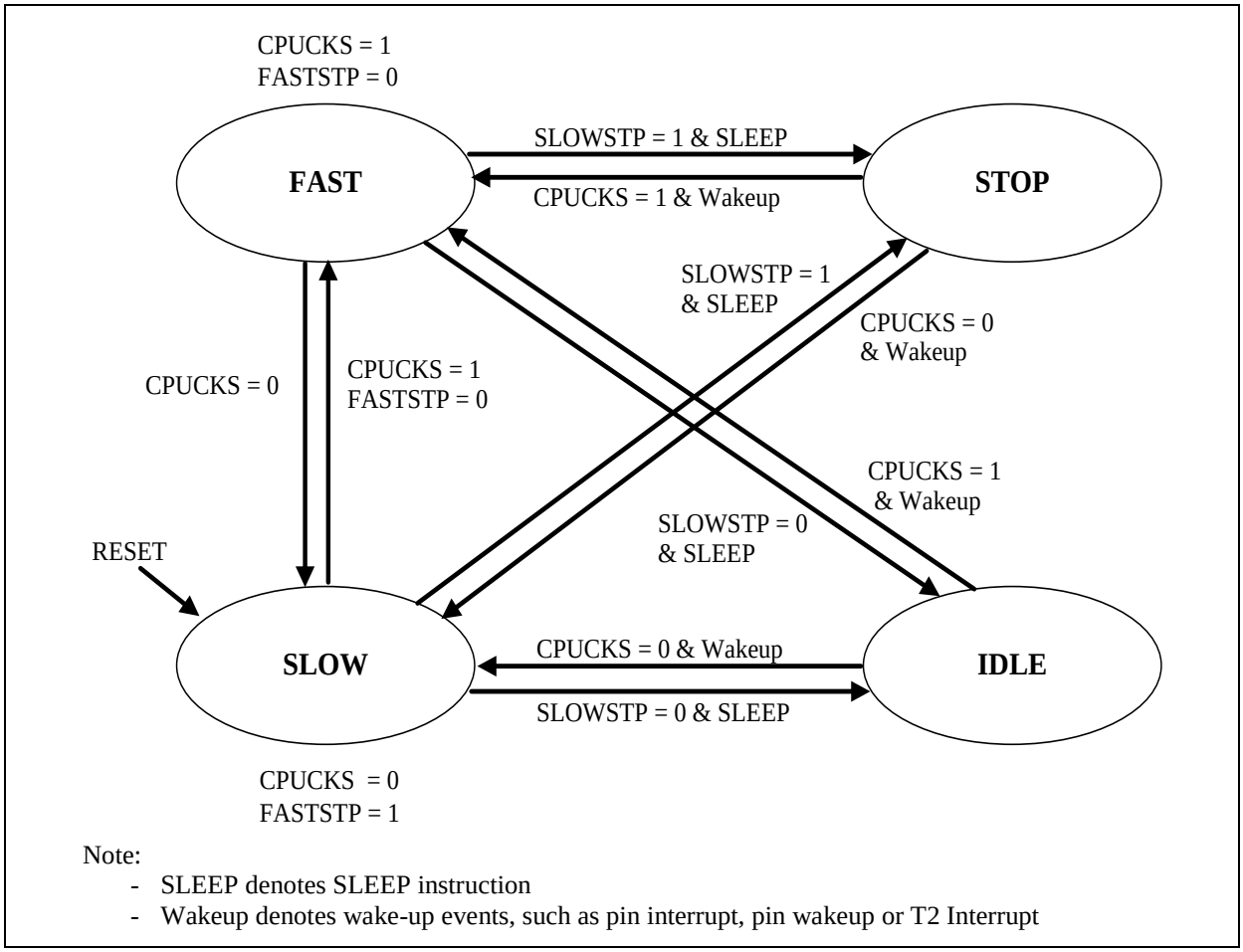
In this mode, the program is executed using Fast-clock as CPU clock.

IDLE Mode:

If Slow-clock is enabled (SLOWSTP=0) and T2CKS=0 before executing the SLEEP instruction, the CPU enters the IDLE mode. In this mode, the Slow-clock source keeps T2 block running. CPU stop fetching code and all blocks are stop except T2 related circuits. Idle mode is terminated by Reset or enabled Interrupts wake up.

STOP Mode:

If Slow-clock is disabled (SLOWSTP=1) and LCD driver is closed (LCDON=0) before executing the SLEEP instruction, every block is turned off and the device enters the STOP mode after executing the SLEEP instruction. Stop Mode can be terminated by Reset or pin wake up.



Note:
- SLEEP denotes SLEEP instruction
- Wakeup denotes wake-up events, such as pin interrupt, pin wakeup or T2 Interrupt

CPU Operation Block Diagram

◇Example: Switch operating mode from SLOW mode to FAST mode

```
BCF     FASTSTP     ; Enable Fast-clock
BSF     CPUCKS      ; Switch system clock source to Fast-clock
```

◇Example: Switch operating mode from FAST mode to SLOW mode

```
BCF     SLOWSTP     ; Enable Slow-clock
BCF     CPUCKS      ; Switch system clock source to Slow-clock
BSF     FASTSTP     ; Stop Fast-clock
```

◇Example: Switch operating mode to IDLE mode

```
BCF     SLOWSTP     ; Enable Slow-clock
SLEEP               ; Enter IDLE mode
```

◇Example: Switch operating mode to STOP mode

```
BSF     SLOWSTP     ; Stop Slow-clock
SLEEP               ; Enter STOP mode
```

F0B	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKCTL	SCKTYPE	SXTGAIN		SLOWSTP	FASTSTP	CPUCKS	CPUPSC	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	1	1	0	1	0	1	1

F0B.7 **SCKTYPE:** Slow-clock type, this bit can be changed only in Fast mode (CPUCKS =1).
0: SIRC
1: SXT, also set PA3 and PA4 as crystal oscillator pins.
Note: In SXT mode, user should set the PA3 and PA4 pins as Input with Pull-up (Mode 0).

F0B.6~5 **SXTGAIN:** 32768 SXT oscillator gain, 3=Highest gain, 0=Lowest gain. Higher gain can shorten the Crystal oscillation warm-up time. Lower gain can reduce oscillation current.

F0B.4 **SLOWSTP:** Slow-clock Stop control
0: Slow-clock run
1: Slow-clock stop

F0B.3 **FASTSTP:** Fast-clock Stop control, This bit can be changed only when CPUCKS=0
0: Fast-clock run
1: Fast-clock stop

F0B.2 **CPUCKS:** System clock (Fsys) selection, This bit can be changed only when FASTSTP=0
0: Slow-clock
1: Fast-clock

F0B.1~0 **CPUPSC:** System clock source prescaler.
00: divided by 8
01: divided by 4
10: divided by 2
11: divided by 1

R03	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWRDN	PWRDN							
R/W	W							
Reset	–	–	–	–	–	–	–	–

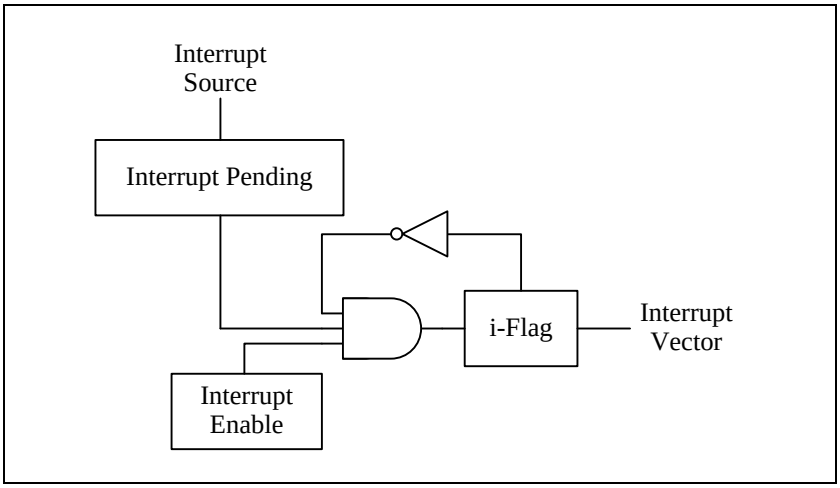
R03.7~0 **PWRDN:** Write this register (=SLEEP instruction) to enter IDLE or STOP Mode

9. Interrupt

This device has 1 level, 1 vector and 9 interrupt sources. Each interrupt source has its own enable control bit. An interrupt event will set its individual pending flag, no matter its enable control bit is 0 or 1.

If the corresponding interrupt enable bit has been set (INTIE), it would trigger CPU to service the interrupt. CPU accepts interrupt in the end of current executed instruction cycle. In the mean while, a "CALL 001" instruction is inserted to CPU, and i-flag is set to prevent recursive interrupt nesting.

The i-flag is cleared in the instruction after the "RETI" instruction. That is, at least one instruction in main program is executed before service the pending interrupt. The interrupt event is level triggered. F/W must clear the interrupt event register while serving the interrupt routine.



F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.7 **PWM0IE:** PWM0 interrupt enable
0: disable
1: enable

F08.6 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

F08.5 **RFCIE:** RFC interrupt enable
0: disable
1: enable

F08.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

F08.3 **T2IE:** T2 interrupt enable
0: disable
1: enable

F08.2 **INT2IE:** INT2 (PA7) interrupt enable
0: disable
1: enable

F08.1 **INT1IE:** INT1 (PB4) interrupt enable

0: disable
1: enable

F08.0 **INT0IE:** INT0 (PA0) interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.7 **PWM0IF:** PWM0 interrupt event pending flag
Set by H/W while PWM0 period completes, clear by S/W writing 0x7F to INTIF

F09.6 **TM1IF:** Timer1 interrupt event pending flag
Set by H/W while Timer1 overflows, clear by S/W writing 0xBF to INTIF

F09.5 **RFCIF:** RFC counter overflow interrupt event pending flag
Set by H/W while RFC counter overflow, clear by S/W writing 0xDF to INTIF

F09.4 **TM0IF:** Timer0 interrupt event pending flag
Set by H/W while Timer0 overflows, clear by S/W writing 0xEF to INTIF

F09.3 **T2IF:** T2 interrupt event pending flag
Set by H/W while T2 overflows, clear by S/W writing 0xF7 to INTIF

F09.2 **INT2IF:** INT2 (PA7) pin interrupt pending flag
Set by H/W at INT2 pin's falling/rising edge, clear by S/W writing 0xFB to INTIF

F09.1 **INT1IF:** INT1 (PB4) pin interrupt pending flag
Set by H/W at INT1 pin's falling/rising edge, clear by S/W writing 0xFD to INTIF

F09.0 **INT0IF:** INT0 (PA0) pin interrupt pending flag
Set by H/W at INT0 pin's falling/rising edge, clear by S/W writing 0xFE to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.2 **INT2EDG:** INT2 pin (PA7) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

F0C.1 **INT1EDG:** INT1 pin (PB4) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

F0C.0 **INT0EDG:** INT0 pin (PA0) interrupt trigger edge select
0: falling edge to trigger
1: rising edge to trigger

F16	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDIE								LBDIE
R/W								R/W
Reset								0

F16.0 **LBDIE:** Low battery detection (LBD) interrupt enable
0: prohibited
1: enable

F17	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDIF								LBDIF
R/W								R/W
Reset								0

F17.0 **LBDIF:** Low battery detection (LBD) interrupt flag
When CMPO=0, H/W sets LBDIF to 1, and writes 0xFE to LBDIF through S/W to clear this flag, but when CMPO continues to 0, LBDIF cannot be cleared.

10. I/O Port

I/O pins can be used as Schmitt-trigger input, CMOS push-pull output, or Open-drain output. The pull-up resistor is assignable to PA0~7, PB4~PB7 by S/W setting. To use the pin in Schmitt-trigger input mode, S/W needs to set the I/O pin to Mode0 or Mode1 and the corresponding port data PxD=1. Reading the pin data (PxD) has different meaning. In "Read-Modify-Write" instruction, CPU actually reads the output data register. In the others instructions, CPU reads the pin state. The so-called "Read-Modify-Write" instruction includes BSF, BCF and all instructions using F-Plane as destination.

In addition, for users of P8625/45, when HIX2=1 (SFR R18.0=1) is set, the CMOS output high voltage of PWM0 (PA1 and PA6) will be doubled VCC. It should be noted that when PA1 turns on the HIX2 function, it will affect the characteristics of RFC2R on PA1.

The operations of 4 pin modes are listed as below.

PA0~PA6, PB4~PB7 supports all 4 pin modes,

PB0~PB3 supports Mode 1~3 (Mode 0 is not supported)

PA7 only supports Mode 0~1.

* P8620 / 25 does not contain PB4 ~ PB7

Pin Mode	PxD SFR data	Pin State	Pull-up Resistor	Digital Input	Pin function
Mode 0	0	Drive Low	N	N	Open Drain output low without pull-high
	1	Pull-High	Y	Y	Input with pull-high
Mode 1	0	Drive Low	N	N	Open Drain output low without pull-high
	1	Hi-Z	N	Y	Input without pull-high
Mode 2	0	Drive Low	N	N	CMOS push-pull output
	1	Drive High	N	N	
Mode 3	1	–	N	N	Alternative function, such as LCD, PWM and RFC

I/O Pin Function Table (except PA7)

CFGWH.12	Pin Mode PA7MOD	PAD[7] SFR data	Pin State	Pull-up Resistor	Pin function
0	0	0	Drive Low	N	open-drain output low without pull-high
0	0	1	Pull-High	Y	Input with pull-high
0	1	0	Drive Low	N	open-drain output low without pull-high
0	1	1	Hi-Z	N	Input without pull-high
1	0	1	Pull-High	Y	Reset input with pull-high

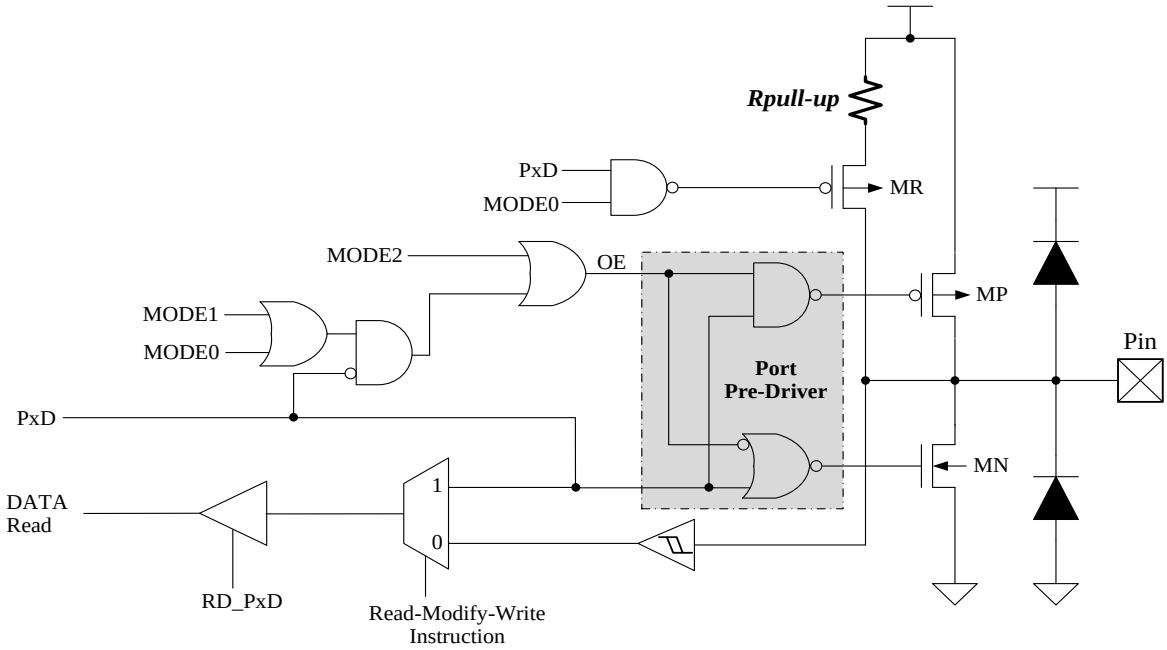
PA7 Pin Function Table

Beside general purposed I/O port function, each pin may have one or more alternative functions.

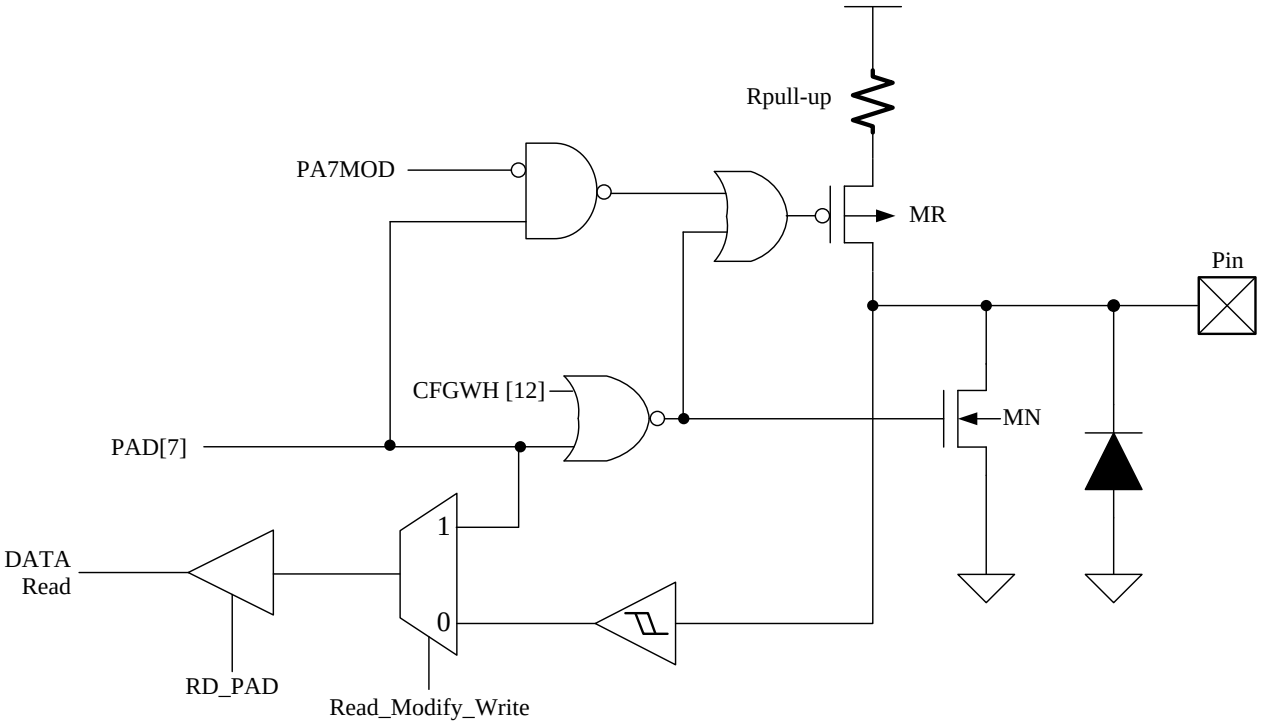
Pin Name	Interrupt	Wake-up	LCD	RFC	Others	Mode3
PA0	INT0			RFC1R		RFC1R
PA1				RFC2R	PWM0N	RFC2R
PA2				RFC0R		RFC0R
PA3					XOUT	
PA4					XIN	
PA5				RFCX		RFCX
PA6					PWM0P	PWM0P
PA7	INT2				nRESET	
PB0		Y	SEG28			SEG28
PB1		Y	SEG27			SEG27
PB2		Y	SEG26			SEG26
PB3		Y	SEG25			SEG25
PB4	INT1	Y			TM0CKI/CAPT	
PB5		Y			PWM1O	PWM1O
PB6		Y			TCOUT	TCOUT
PB7		Y		RFC3R		RFC3R

I/O Pin multi-function Table

Note: In SXT mode, user should set the PA3 and PA4 pins as Input with Pull-up (Mode 0).

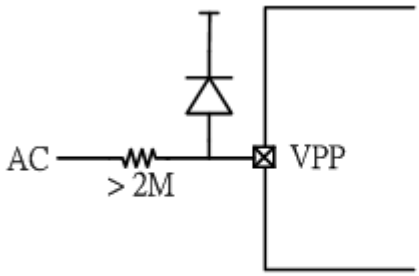


I/O Port Structure (except PA7)



PA7 Structure

Note: PA7(VPP) has no high voltage protection diode, need an external diode and resistor to achieve AC zero corssing detection. The reference circuit is shown below.



Zero crossing detector circuit for VPP pin

F05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAD	PAD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

F05.7~0 **PAD:** PA7~PA0 data

R05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODH	–	PA7MOD	PA6MOD		PA5MOD		PA4MOD	
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	1	0	1	0	1

R05.6 **PA7MOD:** PA7 pin mode
0: Mode0, open-drain I/O with internal pull-up
1: Mode1, open-drain I/O without internal pull-up

R05.5~4 **PA6MOD:** PA6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM0P CMOS push pull output

R05.3~2 **PA5MOD:** PA5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFCX input

R05.1~0 **PA4MOD:** PA4 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R06	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODL	PA3MOD		PA2MOD		PA1MOD		PA0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R06.7~6 **PA3MOD:** PA3 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R06.5~4 **PA2MOD:** PA2 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC0R output

R06.3~2 **PA1MOD:** PA1 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC2R output

R06.1~0 **PA0MOD:** PA0 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up

10: Mode2, port data CMOS push-pull output
11: Mode3, RFC1R output

F06	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBD	PBD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

F06.7~0 **PBD:** PB7~PB0 data

R07	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODH	PB7MOD		PB6MOD		PB5MOD		PB4MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R07.7~6 **PB7MOD:** PB7 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, RFC3R output

R07.5~4 **PB6MOD:** PB6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, TCOUT output

R07.3~2 **PB5MOD:** PB5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM1O output

R07.1~0 **PB4MOD:** PB4 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output

R08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODL	PB3MOD		PB2MOD		PB1MOD		PB0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R08.7~6 **PB3MOD:** PB3 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG25 output

R08.5~4 **PB2MOD:** PB2 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG26 output

R08.3~2 **PB1MOD:** PB1 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG27 output

R08.1~0 **PB0MOD:** PB0 pin mode

0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG28 output

R12	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBWKEN	PBWKEN							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R12.7~0 **PBWKEN:** PB7~PB0 low level wakeup
0: disable
1: enable

R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.1 **PWM0NOE:** PWM0N output to PA1 pin
0: disable
1: enable

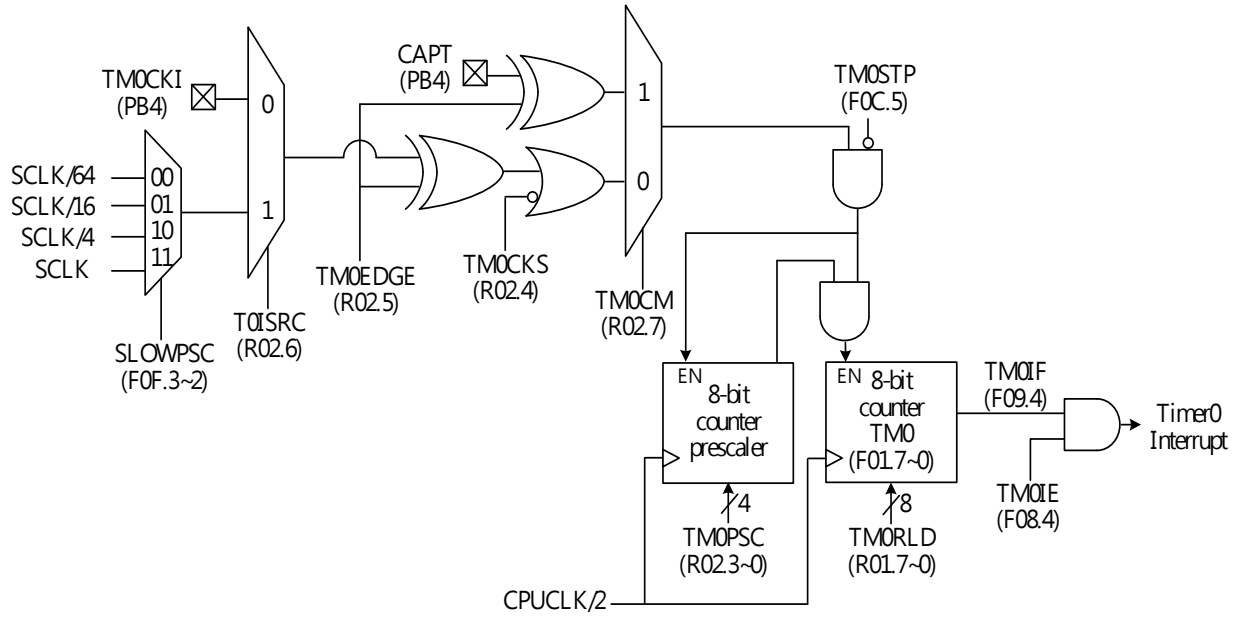
R18	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HIX2								HIX2
R/W								R/W
复位								0

R18.0 **HIX2:** (For P8625 and P8645 only)
Used for PWM0 pin. When HIX2 = 1, the CMOS output high voltage of PWM0 (PA1 and PA6) will be boosted to 2*VCC.

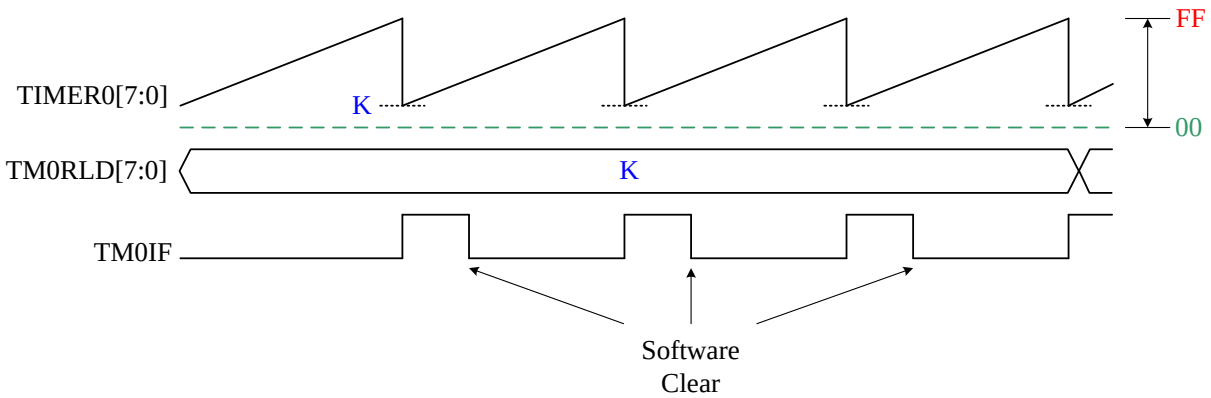
11. Timers

Timer0

Timer0 is an 8-bit wide register located in F-Plane 01h (TM0). The Timer0 register value will increase according to the prescaler clock source, which comes from the instruction cycle (Fsys/2). The increase rate of Timer0 is determined by Timer0's prescaler ratio (TM0PSC). When the Timer0 count overflows, TM0IF is 1 and the Timer0 register value returns to the TM0RLD value. If the Timer0 interrupt enable TM0IE) is 1, then the chip interrupt (interrupt) program will be executed and the PC jumps to 001H. If TM0STP is 1, Timer0 stops counting.



Timer0 Block Diagram



Timer0 Timing Diagram

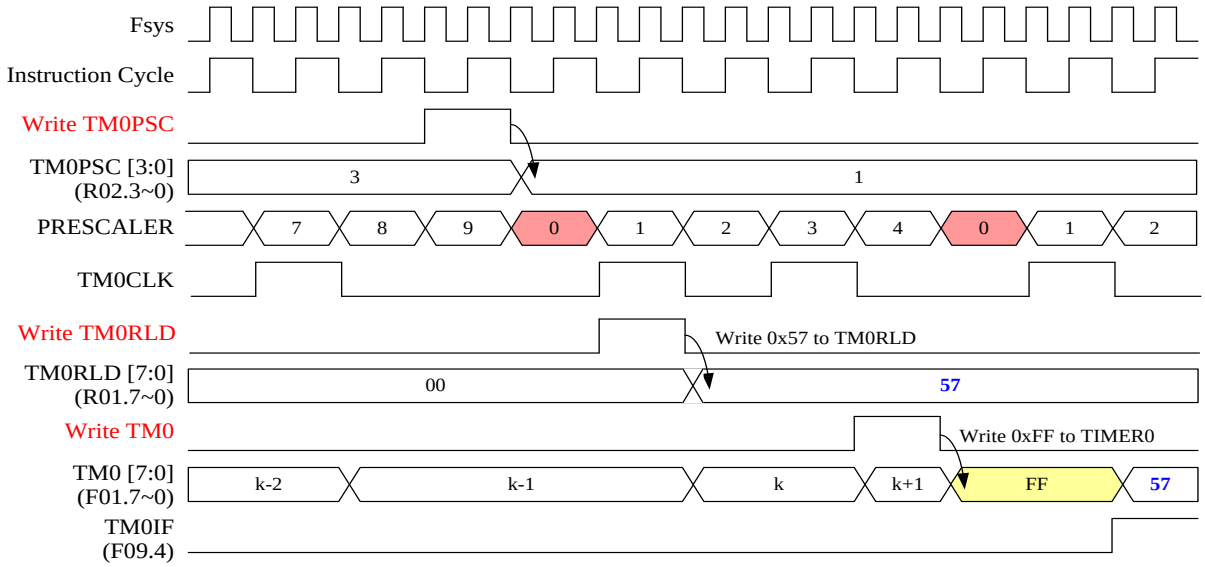
	Capture mode CAPT (PB4)	Timer mode	Counter mode TM0CKI (PB4)	Counter mode SCLK/1/4/16/64
TM0CM	1	0	0	0
TM0CKS	x	0	1	1
T0ISRC	x	x	0	1

Timer0 mode control signal table

Timer mode:

If TM0CM = 0 and TM0CKS = 0, Timer0 is in the timing mode and the clock source is the instruction cycle (Fsys/2).

When Timer0 prescaler (TM0PSC) is written, the internal 8-bit prescaler will be cleared so that the counting cycle is correct when the first Timer0 counts. TM0CLK is an internal signal that increases Timer0 by 1 at the end of TM0CLK. TM0WR is also an internal signal, indicating that Timer0 is a direct write instruction; meanwhile, the internal 8-bit prescaler will be cleared. When Timer0 counts from FFh to TM0RLD, Timer0 overflows. If TM0IE is set to 1, TM0IF will be set to 1 and an interrupt will be generated.



Timer0 works in Timer mode (TM0CKS=0)

The equation of TM0 interrupt time value is as following:

TM0 interrupt frequency = (Fsys/2) / TM0PSC / (256-TM0)

◇ Example: Setup TM0 work in Timer mode

```
; Setup TM0 clock source and divider
        MOVLW   0000 0101B      ; R02.4 = 0, Setup TM0 clock=  Fsys/2
        MOVWR   R02             ; R02.3~0=5 (TM0PSC)
                                ; TM0 clock prescaler = Fsys/64
; Set TM0 timer.
```

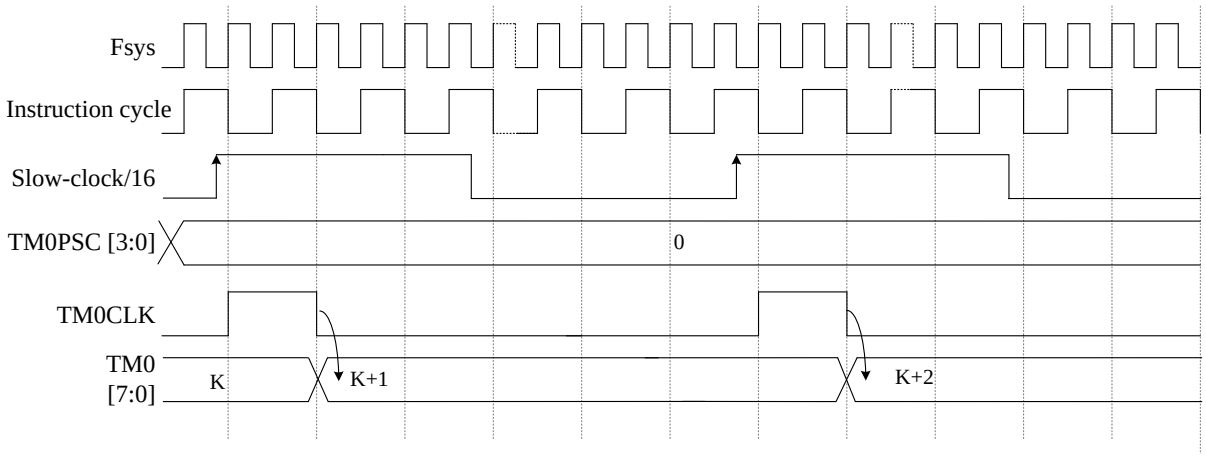
```
        BSF     TM0STP      ; Disable TM0 counting (Default "0").
        MOVLW   156
        MOVWF   TM0         ; Write 156 into TM0 register of F-Plane. (F01)
        MOVLW   124
        MOVWR   TM0RLD      ; Write 124 into TM0RLD register of R-Plane. (R01)

; Enable TM0 timer and interrupt function.
        MOVLW   111**0**1111B   ; Clear TM0 request interrupt flag by byte operation
        MOVWF   INTIF       ; F-Plane 09H
        MOVLW   000**1**0000B   ; Enable TM0 interrupt function
        MOVWR   INTIE       ; F-Plane 08H
        BCF     TM0STP      ; Enable TM0 counting (Default “0”).
```

Counter mode:

If TM0CM = 0, TM0CKS = 1 and T0ISRC = 0, Timer0 is in counting mode.

The chip has two sources of counting modes. If T0ISRC = 0, the count mode source of Timer0 is TM0CKI (PB4). If T0ISRC = 1, the count mode source of Timer0 is "Slow clock divided by 1/4/16/64". These sources are synchronized through the instruction cycle (Fsys/2). This means that the instruction cycle (Fsys/2) must be faster than the counting mode source to work properly.



TM0CKS=1, Timer0 clock source is Slow-clock/16

Capture mode:

If TM0CM = 1, Timer0 is in capture mode.
Users can measure the signal on the CAPT pin through Timer0 capture mode and Timer1 capture mode. The usage of the capture mode can be more introduced in the Timer1 chapter.

F01	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0	TM0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F01.7~0 **TM0:** Timer0 data

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.4 **TM0IE:** Timer0 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.4 **TM0IF:** Timer0 interrupt event pending flag
Set by H/W while Timer0 overflows, clear by S/W writing 0xEF to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.5 **TM0STP:** Timer0 counter stop
0: Timer0 is counting
1: Timer0 stop counting

F0F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCTL	RFCLR	T1STPRFC	T0STPRFC	RFCSTP	SLOWPSC		RFCHS	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	1	0	0

F0F.3~2 **SLOWPSC:** slow clock divider for Timer0
00: divided by 64
01: divided by 16
10: divided by 4
11: divided by 1

R01	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0RLD	TM0RLD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R01.7~0 **TM0RLD:** Timer0 Overflow Reload Data

R02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0CTL	TM0CM	T0ISRC	TM0EDGE	TM0CKS	TM0PSC			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

R02.7 **TM0CM:** Timer0 Capture mode enable
0: Timer mode or Counter mode
1: Capture mode

R02.6 **T0ISRC:** Timer0 Counter mode source
0: TM0CKI pin (PB4)
1: Slow-clock div 1/4/16/64 sets by SLOWPSC(F0F.3~2)

R02.5 **TM0EDGE**:
If TM0EDGE=1, TM0CKI/CAPT input data will be reversed.

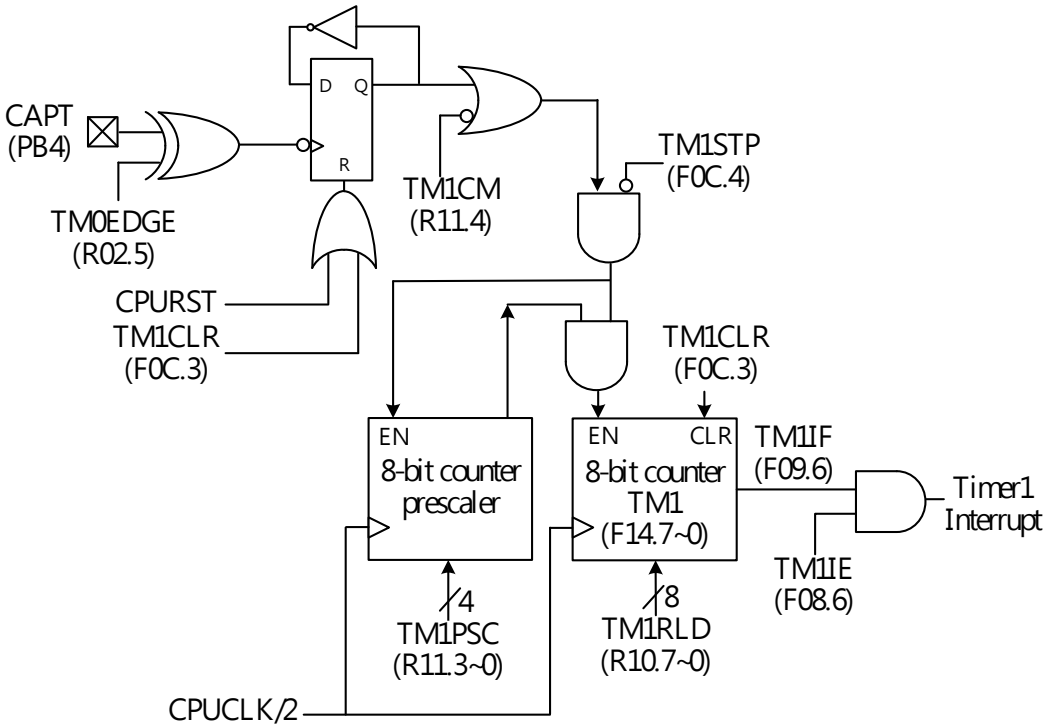
Timer0 prescaler counting edge for Counter mode
0: Rising edge
1: Falling edge
Timer0 capture level for Capture mode
0: High level capture
1: Low level capture
Timer1 capture edge for Capture mode
0: Falling edge capture
1: Rising edge capture

R02.4 **TM0CKS:** Timer0 mode select
0 : Timer mode (Fsys)
1 : Counter mode (SCLK divided 1/4/16/64 or T0CKI(PB4))

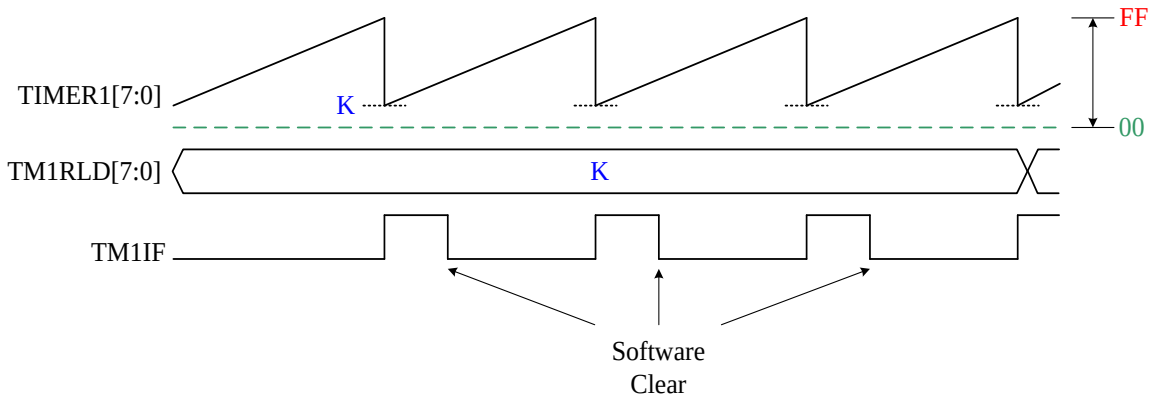
R02.3~0 **TM0PSC:** Timer0 clock source prescaler. Clock source is divided by
0000: Fsys/2 0101: Fsys/64
0001: Fsys/4 0110: Fsys/128
0010: Fsys/8 0111: Fsys/256
0011: Fsys/16 1xxx: Fsys/512
0100: Fsys/32

Timer1

Timer1 is an 8-bit wide register located in F-Plane 14h (TM1). It can be read or written in the same way as any other F-Plane register. There are two modes. One is the timing mode, and the other is the capture mode. It is almost the same as Timer0, except Timer1 has no counting mode, and the capture event of Timer1's capture mode is different from Timer0. Timer1 automatically toggles according to the prescaled clock source, which comes from the instruction cycle (Fsys/2), and the rate is determined by TM1PSC. When the count of Timer1 overflows, TM1IF is 1 and the value of Timer1 register returns to the value of TM1RLD. If Timer1 interrupt enable TM1IE is 1 at this time, the chip interrupt program will be executed and the PC jumps to 001H. If TM1STP is 1, Timer1 stops counting.



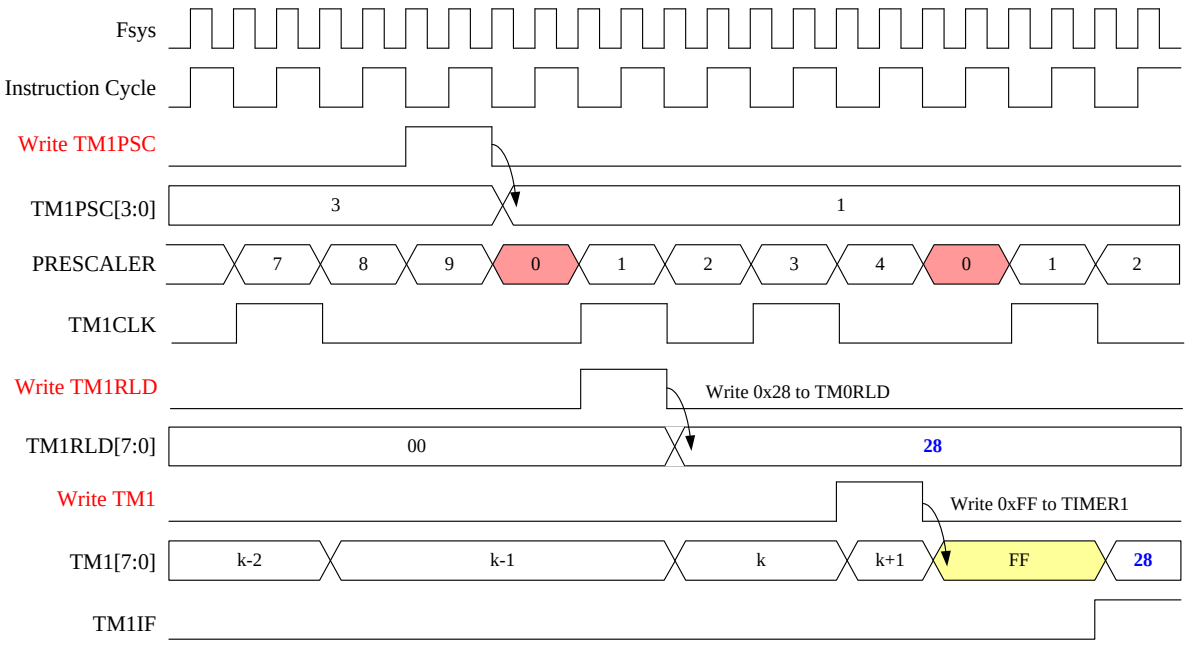
Timer1 Block Diagram



Timer1 Reload Diagram

Timer mode:

If TM1CM=0, Timer1 is in timer mode.



Timer1 Timing Diagram

Capture mode:

If TM1CM = 1, Timer1 is in capture mode.

See the figure below, the capture event of Timer1's capture mode is different from Timer0. The user can measure the signal on the CAPT pin through Timer0 capture mode and Timer1 capture mode.

TM0EDGE = 0:

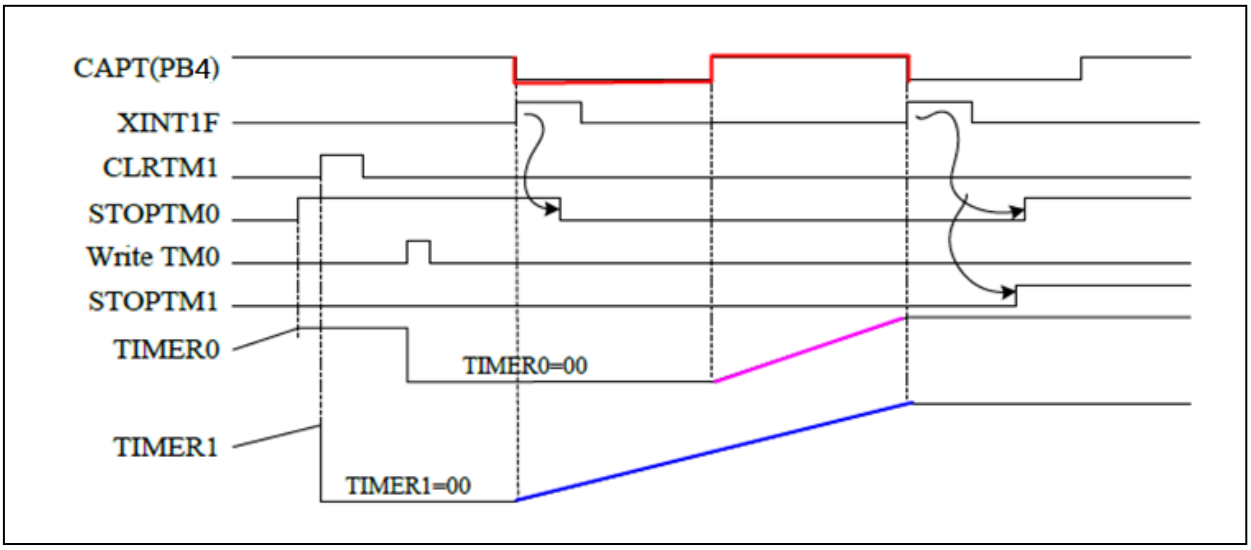
When CAPT is high, Timer0 runs, and when CAPT is low, Timer0 pauses.

When CAPT is a falling edge, if the Timer1 counter is paused, it switches to running; if the Timer1 counter is running, it switches to pause.

TM0EDGE = 1:

When CAPT is low, Timer0 runs, and when CAPT is high, Timer0 pauses.

When CAPT is a rising edge, if the Timer1 counter is paused, it switches to running; if the Timer1 counter is running, it switches to pause.



Timer0 and Timer1 used to measure the signal on CAPT pin

F14	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1	TM1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F14.7~0 **TM1:** Timer1 data

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.6 **TM1IE:** Timer1 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.6 **TM1IF:** Timer1 interrupt event pending flag
Set by H/W while Timer1 overflows, clear by S/W writing 0xBF to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.4 **TM1STP:** Timer1 counter stop
0: Timer1 is counting

1: Timer1 stop counting

F0C.3 **TM1CLR:** Timer1 clear and hold when this bit is "1" in timer mode/capture mode

R02	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM0CTL	TM0CM	T0ISRC	TM0EDGE	TM0CKS	TM0PSC			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	0	0	0

R02.5 **TM0EDGE**:
If TM0EDGE=1, TM0CKI/CAPT input data will be reversed.

Timer0 prescaler counting edge for Counter mode
0: Rising edge
1: Falling edge
Timer0 capture level for Capture mode
0: High level capture
1: Low level capture
Timer1 capture edge for Capture mode
0: Falling edge capture
1: Rising edge capture

R10	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1RLD	TM1RLD							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

R10.7~0 **TM1RLD:** Timer1 Overflow Reload Data

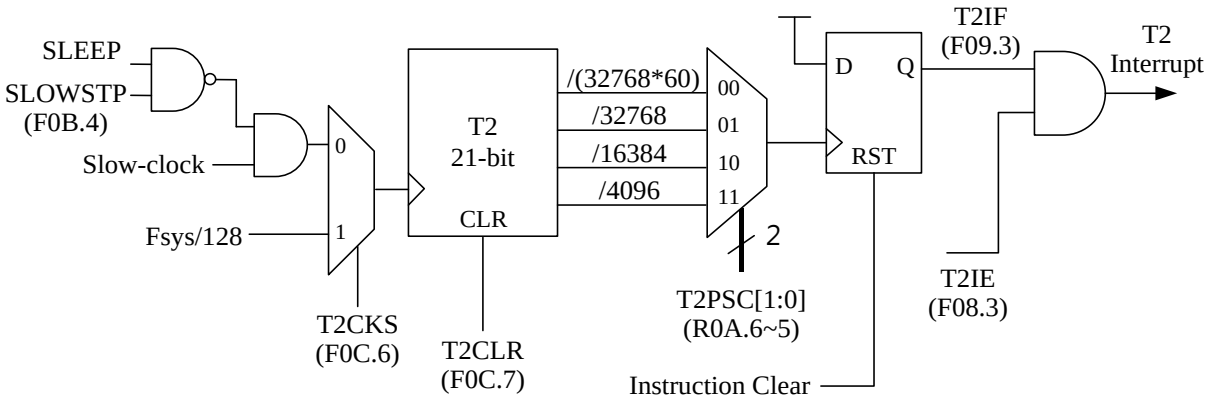
R11	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM1CTL	-	-	-	TM1CM	TM1PSC			
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset	-	-	-	0	0	0	0	0

R11.4 **TM1CM:** Timer1 Capture mode
0: Timer mode
1: Capture mode

R11.3~0 **TM1PSC:** Timer1 clock source prescaler. Clock source is divided by
0000: 1
0001: 2
0010: 4
0011: 8
0100: 16
0101: 32
0110: 64
0111: 128
1xxx: 256

Timer2

Timer (T2) is a 21-bit timer, the clock source is from Fsys/128 or slow clock, selected by T2CKS (F0C.6). The 21-bit content of T2 cannot be read by instructions. The T2 clock prescaler depends on the T2PSC (R08.6~5), which can be divided by one of 32768*60, 32768, 16384 or 4096. An interrupt flag (T2IF) will be generated when the Timer overflows. If TM2IE is 1 , It will enter the interrupt program of the chip. The function is shown below.



T2 Block Diagram

◇ Example: CPU is running at FAST mode, Fsys=Fast-clock=FIRC, Slow-clock source is SXT

```
; Setup T2 clock source and divider
        BCF     T2CKS           ; T2CKS=0, T2 clock source is Slow-clock
        MOVLW   001100000B
        MOVWR   R0A             ; T2PSC=01b, divided by 32768
        BSF     T2CLR           ; T2CLR=1, clear T2 counter

; Enable T2 interrupt function
        MOVLW   11110111B
        MOVWF   INTIF           ; Clear T2 request interrupt flag
        BSF     T2IE            ; Enable T2 interrupt function
```

T2 clock source is Slow-clock = 32 KHz, T2 divided by 32768

T2 interrupt period =1 second

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.3 **T2IE:** T2 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.3 **T2IF:** T2 interrupt event pending flag
Set by H/W while T2 overflows, clear by S/W writing 0xF7 to INTIF

F0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MF0C	T2CLR	T2CKS	TM0STP	TM1STP	TM1CLR	INT2EDG	INT1EDG	INT0EDG
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F0C.7 **T2CLR**: T2 counter clear
0: T2 is counting
1: T2 is cleared, this bit is auto cleared by H/W

F0C.6 **T2CKS:** T2 clock source selection
0: Slow-clock
1: Fsys/128

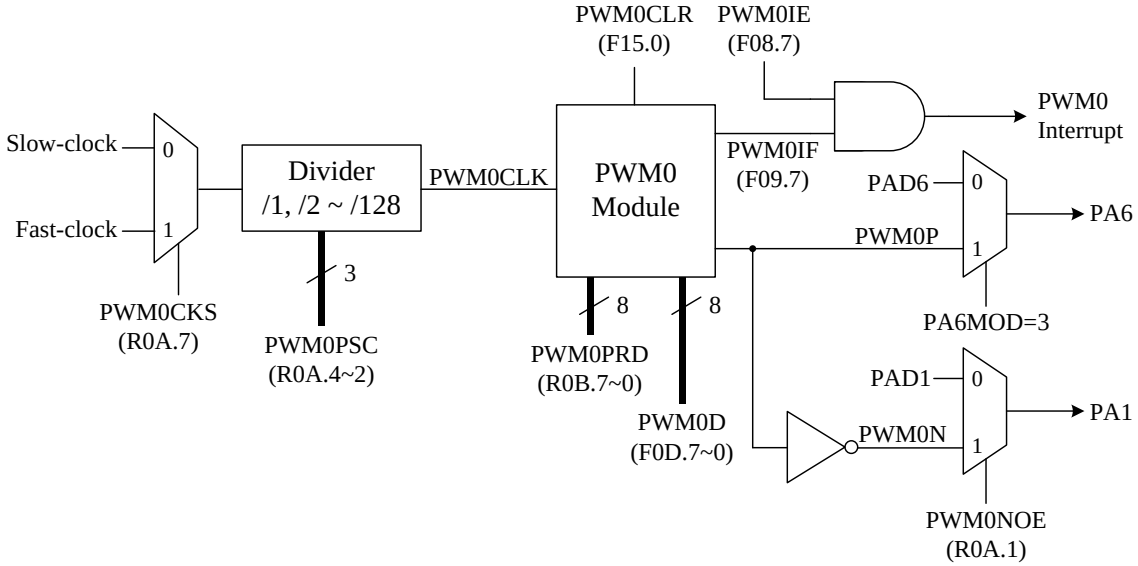
R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.6~5 **T2PSC:** T2 prescaler. T2 interrupt is T2 clock is divided by
00: (32768*60)
01: 32768
10: 16384
11: 4096

12. PWM

PWM0

The PWM0 can select Fast-clock or Slow-clock as its clock source, with divided by 1~128 prescaler. The PWM0 period is adjustable by PWM0PRD and its 256 step duty cycle is controlled by PWM0D. The PWM0P and PWM0N are positive and negative CMOS output pairs to pins.



PWM0 Block Diagram

◇Example: Slow-clock = SXT 32768Hz

```
; Setup PWM0P a 512Hz, 50% duty cycle output
        MOVLW   0001110 0B      ; PWM0CKS=0, PWM0PSC=111
        MOVWR   PWM0CTL         ; PWM0CLK=Slow-clock/1=32768Hz

        MOVLW   63
        MOVWR   PWM0PRD         ; Set PWM0 period = 63 + 1 = 64

        MOVLW   32
        MOVWF   PWM0D           ; Set PWM0 duty = 32

        MOVLW   0011 0000B      ; PA6MOD=3
        MOVWR   PAMODH          ; PWM0P output to PA6 pin
```

PWM0 clock frequency = Slow-clock / PWM0PSC = 32768Hz / 1 = 32768Hz

PWM0 output frequency = PWM0CLK / (PWM0PRD + 1) = 32768Hz / (63 + 1) = 512 Hz

PWM0 duty cycle = PWM0D / (PWM0PRD + 1) = 32 / (63 + 1) = 50%

In addition, for P8625/45 users, when setting HIX2=1 (SFR R18.0=1), the CMOS output high voltage of PWM0 (PA1 and PA6) will be doubled VCC. That is, under the working voltage of 1.5V, PWM0P and PWM0N can provide a waveform output with an amplitude of 3V.

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.7 **PWM0IE:** PWM0 interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.7 **PWM0IF:** PWM0 interrupt event pending flag
Set by H/W while PWM0 period completes, clear by S/W writing 0x7F to INTIF

F15	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCLR							PWM1CLR	PWM0CLR
R/W							R/W	R/W
Reset							0	0

F15.0 **PWM0CLR:** PWM0 clear and hold
0: PWM0 running 1: PWM0 clear and hold

R0A	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0CTL	PWM0CKS	T2PSC		PWM0PSC			PWM0NOE	WDTPSC
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

R0A.7 **PWM0CKS:** PWM0 clock source select
0: Slow-clock
1: Fast-clock

R0A.4~2 **PWM0PSC**: PWM0 clock prescaler
000: PWM0 clock is Slow/Fast clock divided by 128
001: PWM0 clock is Slow/Fast clock divided by 64
010: PWM0 clock is Slow/Fast clock divided by 32
011: PWM0 clock is Slow/Fast clock divided by 16
100: PWM0 clock is Slow/Fast clock divided by 8
101: PWM0 clock is Slow/Fast clock divided by 4
110: PWM0 clock is Slow/Fast clock divided by 2
111: PWM0 clock is Slow/Fast clock divided by 1

R0A.1 **PWM0NOE:** PWM0N output to PA1 pin
0: disable
1: enable

F0D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0D	PWM0D							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

F0D.7~0 **PWM0D**: PWM0 duty, 0=0 PWM0CLK, 80h=128 PWM0CLK, FFh=255 PWM0CLK

R09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM0PRD	PWM0PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

R09.7~0 **PWM0PRD**: PWM0 period, FFh=256 PWM0CLK, 7Fh=128 PWM0CLK

R05	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PAMODH	–	PA7MOD	PA6MOD		PA5MOD		PA4MOD	
R/W	–	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	–	0	0	1	0	1	0	1

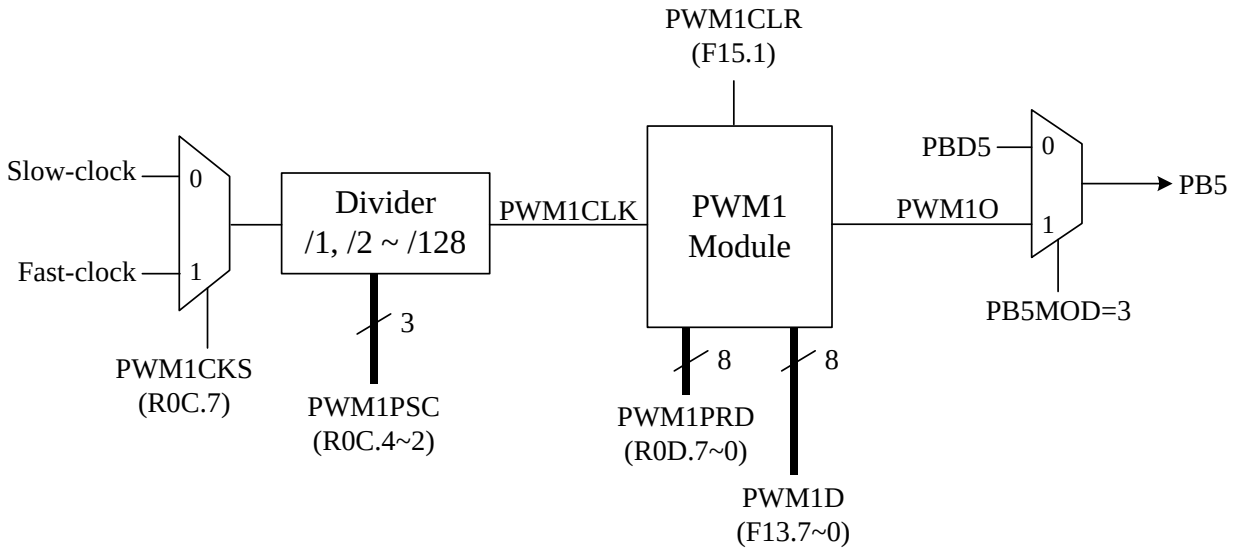
R05.5~4 **PA6MOD:** PA6 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM0P CMOS push pull output

R18	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
HIX2								HIX2
R/W								R/W
复位								0

R18.0 **HIX2:** (For P8625 and P8645 only) (need LCDON(F10.7) = 1)
Used for PWM0 pin. When HIX2 = 1, the CMOS output high voltage of PWM0 (PA1 and PA6) will be boosted to 2*VCC.

PWM1

The PWM1 can select Fast-clock or Slow-clock as its clock source, with divided by 1~128 prescaler. The PWM1 period is adjustable by PWM1PRD and its 256 step duty cycle is controlled by PWM1D. The PWM1O is positive CMOS output to pin.



PWM1 Block Diagram

R0C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1CTL	PWM1CKS	–	–	PWM1PSC			–	–
R/W	R/W	–	–	R/W	R/W	R/W	–	–
Reset	1	–	–	0	0	0	–	–

R0C.7 **PWM1CKS:** PWM1 clock source select
0: Slow-clock
1: Fast-clock

R0C.4~2 **PWM1PSC**: PWM1 clock prescaler
000: PWM1 clock is Slow/Fast clock divided by 128
001: PWM1 clock is Slow/Fast clock divided by 64
010: PWM1 clock is Slow/Fast clock divided by 32
011: PWM1 clock is Slow/Fast clock divided by 16
100: PWM1 clock is Slow/Fast clock divided by 8
101: PWM1 clock is Slow/Fast clock divided by 4
110: PWM1 clock is Slow/Fast clock divided by 2
111: PWM1 clock is Slow/Fast clock divided by 1

F13	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1D	PWM1D							
R/W	R/W							
Reset	1	0	0	0	0	0	0	0

F13.7~0 **PWM1D**: PWM1 duty, 0=0 PWM1CLK, 80h=128 PWM1CLK, FFh=255 PWM1CLK

F15	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWMCLR							PWM1CLR	PWM0CLR
R/W							R/W	R/W
Reset							0	0

F15.1 **PWM1CLR:** PWM1 clear and hold
0: PWM1 running 1: PWM1 clear and hold

R0D	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM1PRD	PWM1PRD							
R/W	R/W							
Reset	1	1	1	1	1	1	1	1

R0D.7~0 **PWM1PRD**: PWM1 period, FFh=256 PWM1CLK, 7Fh=128 PWM1CLK

R07	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODH	PB7MOD		PB6MOD		PB5MOD		PB4MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

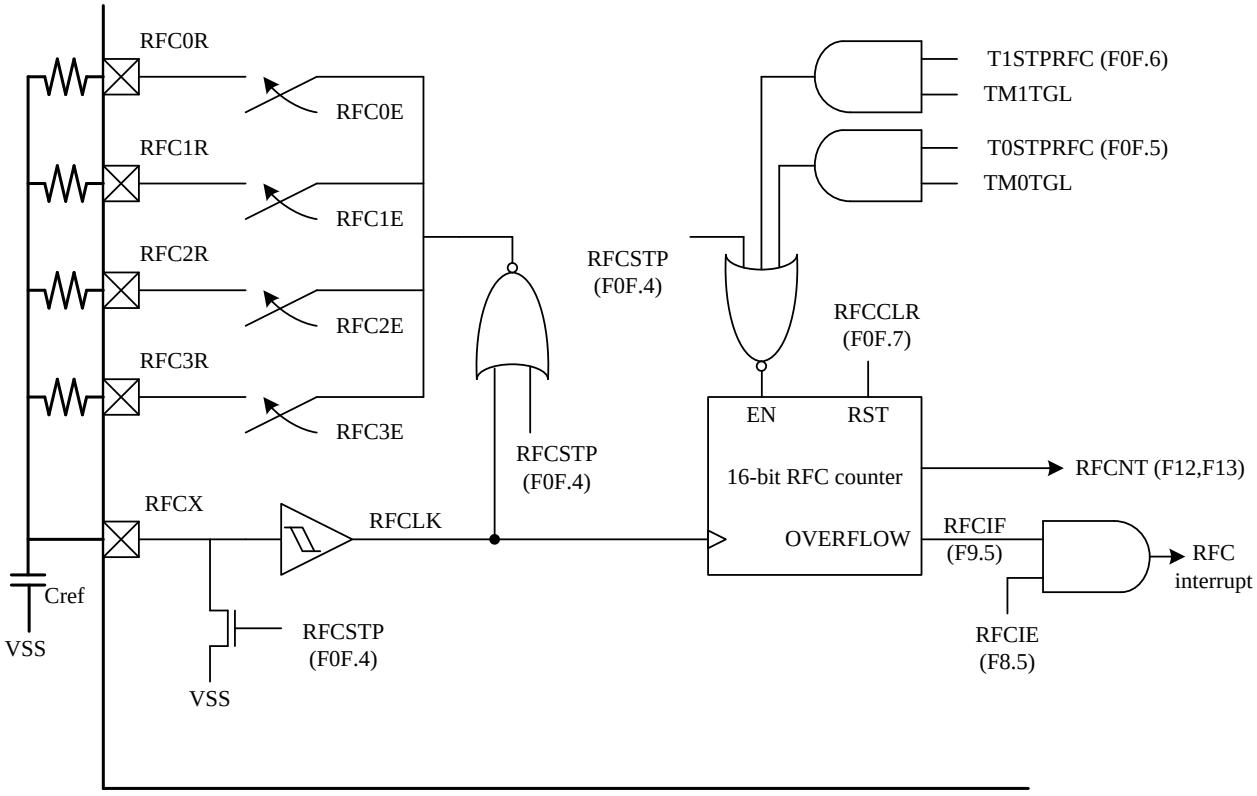
R07.3~2 **PB5MOD:** PB5 pin mode
00: Mode0, open-drain I/O with internal pull-up
01: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, PWM1O CMOS push pull output

13. Resistance to Frequency Converter (RFC)

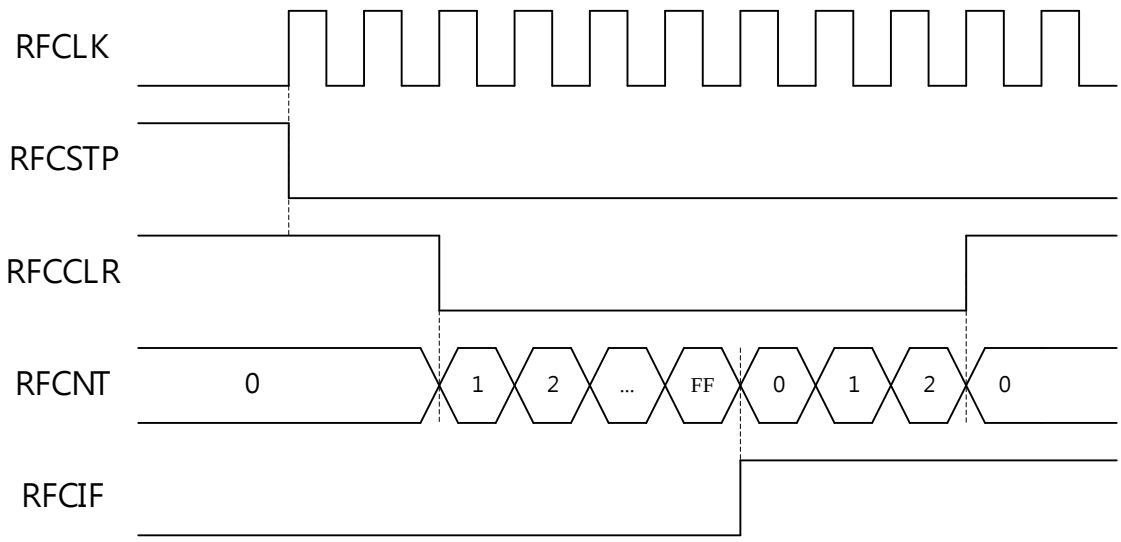
The RFC module contains RC oscillator and RFC counter. The RFC-clock comes from the oscillation circuitry built by RFCX pin and RFC0R, RFC1R, RFC2R or RFC3R pins. There are two RFC architectures, controlled by RFC1T (SFR R17.0).

Architecture 1: RFC counter clock source is RFCLK (RFC1T=0) (same as TM57M5620/25/40/45)

Calculate the number of RFC RC oscillations (RFCLK) in the time between two timer interrupts.



RFC Block Diagram (RFC1T=0)

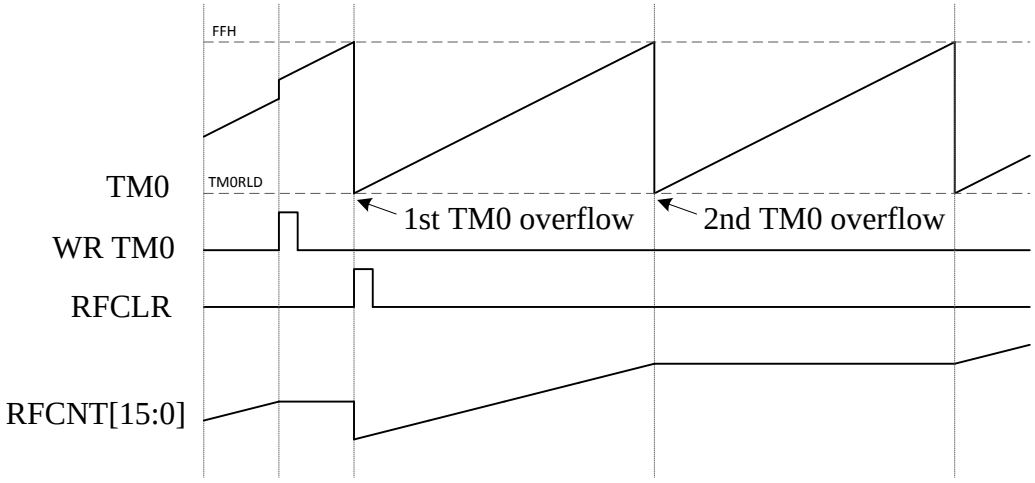


RFC timing diagram (RFC1T=0)

The 16-bit RFC counter can stop by Timer0 or Timer1's overflow control. This function helps the RFC counter to count the RFC clock with more accuracy by H/W automatically start and stop.

Proceed as follows:

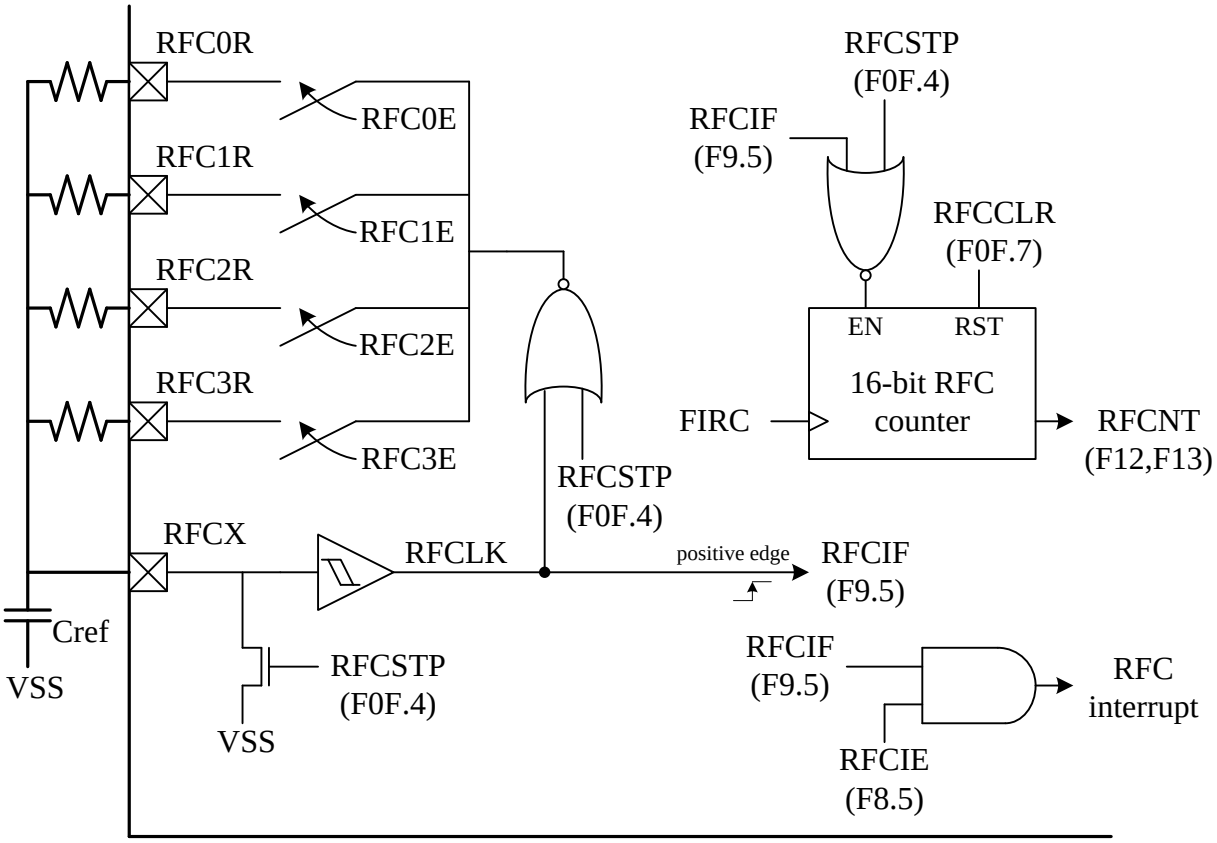
1. Turn on the RFC function (RFCSTP=0), turn on the RFC reset flag (RFCLR=1), and turn on the function of using Timer0 to calculate RFCNT (T0STPRFC=1).
2. Write Timer0 data (F01.7~0).
3. Clear the RFC reset flag (RFCLR=0).
4. After 1st Timer0 overflows, the RFC counter starts counting.
5. After 2st Timer0 overflows, read RFCNT (F12, F13) to get the required RFC count value.



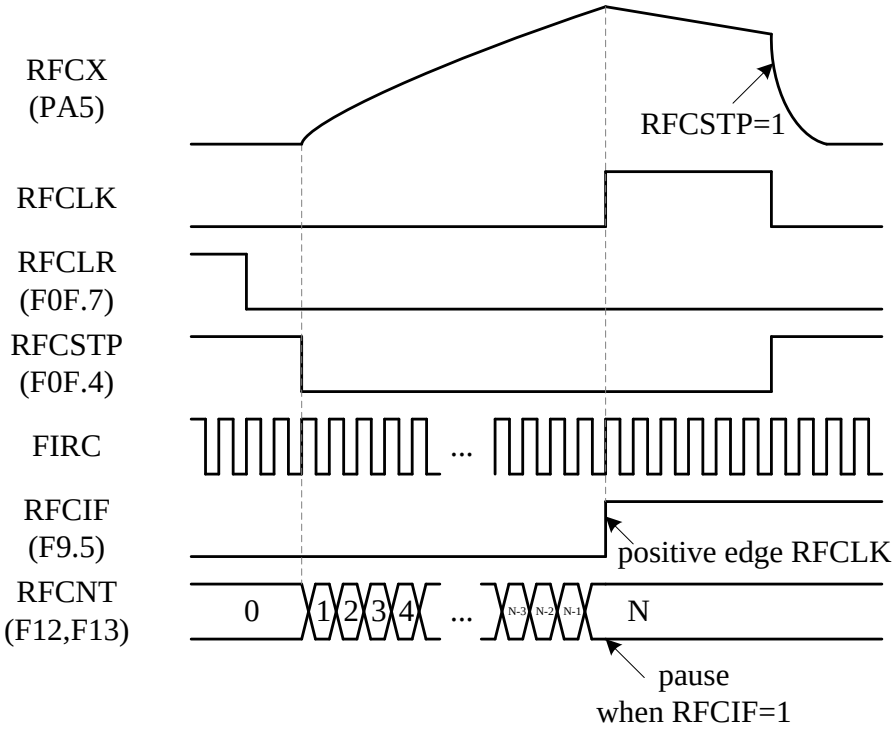
TM0 control RFC

Architecture 2: The RFC counter clock source is FIRC (RFC1T=1)

Calculate the number of counts of the internal fast clock (FIRC) under one RFC RC oscillation period.



RFC Block Diagram (RFC1T=1)



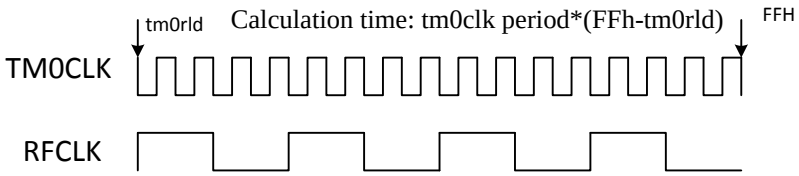
RFC timing diagram (RFC1T=0)

Proceed as follows:

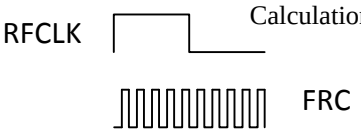
1. Set RFCLR = 0 and RFCSTP = 0.
2. 1st After the RFC interrupt occurs, the RFC counter is automatically suspended, set RFCSTP=1, reset the RFC counter (set RFCLR=1 first and then set RFCLR=0), set RFCSTP=0, after clearing the RFC interrupt flag, the RFC counter starts to count .
3. After the 2rd RFC interrupt occurs, the RFC counter is automatically suspended, and the RFCNT (F12, F13) is read to retrieve the RFC counter value.

*During the period of RFCIF=1, the RFCNT value is suspended and not counted.

RFC1T=0： The RFCNT value obtained in this example is 4



RFC1T=1： The RFCNT value obtained in this example is 10



RFCNT calculation instructions

F0F	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCTL	RFCLR	T1STPRFC	T0STPRFC	RFCSTP	SLOWPSC		RFCHS	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	1	1	1	0	0

F0F.7 **RFCLR:** RFC counter reset.
Reset the RFC counter value.

F0F.6 **T1STPRFC:** Timer1 overflow toggle signal (TM1TGL) to stop RFC counter
(This option is only available under RFC1T=0)
0: disable
1: enable

F0F.5 **T0STPRFC:** Timer0 overflow toggle signal (TM0TGL) to stop RFC counter
(This option is only available under RFC1T=0)
0: disable
1: enable

F0F.4 **RFCSTP:** S/W stop RFC counter and oscillator
0: RFC counter and oscillator run
1: RFC counter and oscillator stop

F0F.1~0 **RFCHS:** select RFC oscillator channel
00: RFC0R (PA2)
01: RFC1R (PA0)
10: RFC2R (PA1)
11: RFC3R (PB7)

F11	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCNTH	RFCNTH							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

F11.7~0 **RFCNTH:** RFC counter high byte, RFCNT[15:8]

F12	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFCNTL	RFCNTL							
R/W	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

F12.7~0 **RFCNTL:** RFC counter low byte, RFCNT[7:0]

F08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIE	PWM0IE	TM1IE	RFCIE	TM0IE	T2IE	INT2IE	INT1IE	INT0IE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F08.5 **RFCIE:** RFC interrupt enable
0: disable
1: enable

F09	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
INTIF	PWM0IF	TM1IF	RFCIF	TM0IF	T2IF	INT2IF	INT1IF	INT0IF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

F09.5 **RFCIF:** RFC interrupt flag

Under RFC1T=0:
This flag is a counter overflow warning. When the RFC counter (RFCNT) overflows, H/W will set RFCIF to 1. Write 0xDF to INTIF via S/W to clear this flag.

Under RFC1T=1:
This flag is the RFC cycle flag. Whenever the positive edge of RFCLK is triggered, H/W will set RFCIF to 1. Write 0xDF to INTIF via S/W to clear this flag. When this flag is 1, RFCNT will suspend counting.

R17	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFC1T								RFC1T
R/W								R/W
复位								0

R17.0 **RFC1T:** When RFC1T=1, RFC uses a architecture with a calculation time of 1 RFCLK.

14. LCD Driver

When LCDON = 1, the LCD driver is enabled. Under the condition of 1/3 LCD Bias, the typical value of LCD Bias voltage is 1/3 VLCD, 2/3 VLCD and VLCD; under the condition of 1/2 LCD Bias, the typical value of LCD Bias voltage is 1/2VLCD and VLCD.

Only one LCD Bias (1/3 Bias) is available for P8620/40.

P8625/45 has two LCD Bias (1/3 Bias, 1/2 Bias) to choose from. When LCDON = 1 for P8625/45, the LCD voltage pump will continue to work to maintain VLCD equal to 2VBAT. The user can select slow clock/4 or slow clock/8 as the clock source of the LCD pump through PUMPCKS.

The maximum value that the LCD driver can drive is shown in the following table. The user can set the function of the multiplexed pin to COM3 or SEG29 through LCDUTY as required. The maximum value that the LCD driver can drive

P/N	LCD (SEG x COM) Max.
TM57P8620	12 x 4 or 13 x 3
TM57P8625	10x 4 or 11 x 3
TM57P8640	28 x 4 or 29 x 3
TM57P8645	26 x 4 or 27 x 3

The maximum value that the LCD driver can drive

LCD frame rate adjustment

Users can use LCDFRM to select different LCD frame rates. The actual LCD frame rate is related to the slow clock source frequency and has nothing to do with the system clock prescaler (CPUPSC). The following table is the LCD frame rate table when SCKTYPE=1 (using SXT) and 32768Hz crystal oscillator is plugged in:

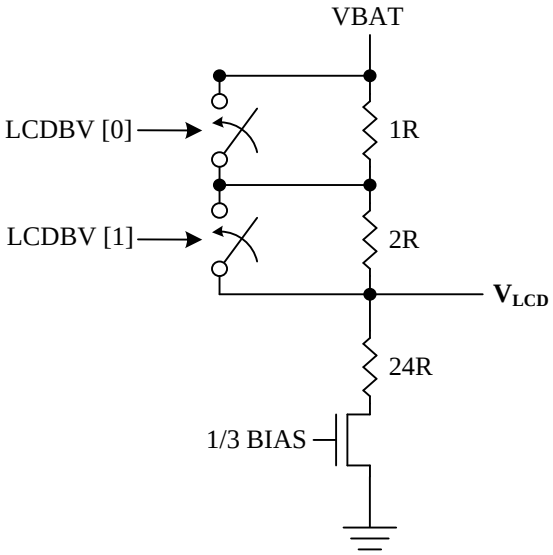
LCDUTY	LCDFRM	LCD frame rate @SXT32768Hz
1/4 DUTY	0	47Hz
1/4 DUTY	1	57Hz
1/4 DUTY	2	73Hz
1/4 DUTY	3	85Hz
1/3 DUTY	0	49Hz
1/3 DUTY	1	57Hz
1/3 DUTY	2	68Hz
1/3 DUTY	3	85Hz

LCD frame rate @SXT32768Hz

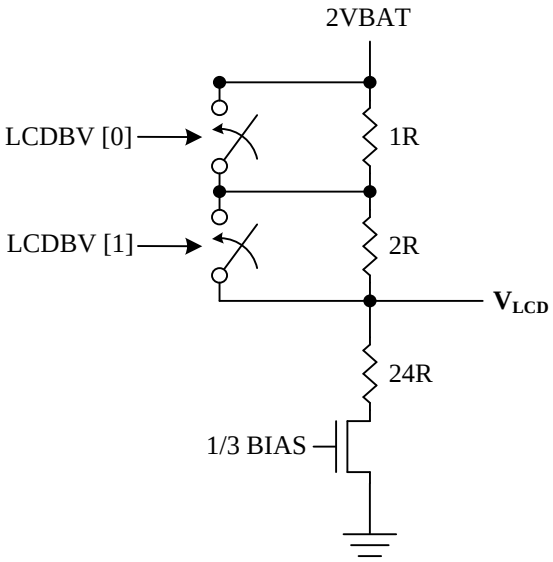
LCD brightness adjustment

Under 1/3Bias, users can increase or decrease the value of VLCD through LCDBV to adjust the brightness of LVD. The schematic diagram is as follows:

P8620/40:



P8625/45: (LCDON=1)



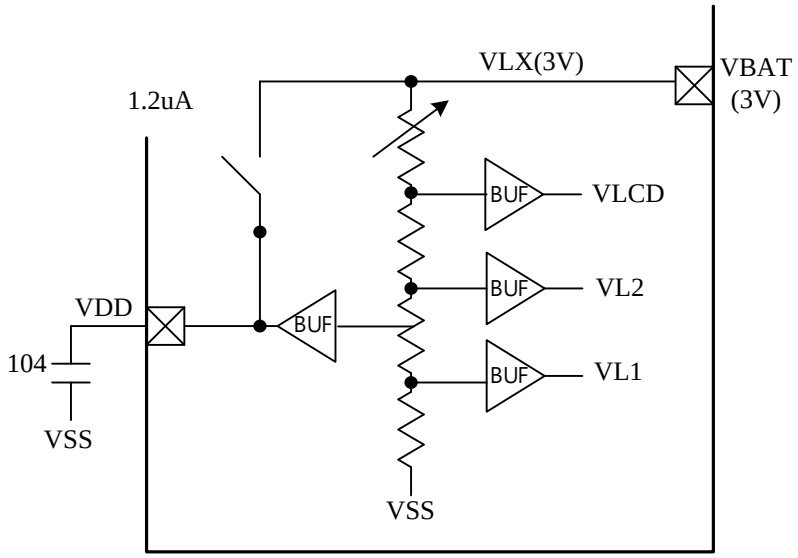
LCDBV[1:0]	LCDBIAS	P8620/40	P8625/45 (LCDON=1)
00	1/3 BIAS	V_{LCD}=0.89*VBAT	V_{LCD}=0.89*2VBAT
01	1/3 BIAS	V_{LCD}=0.92*VBAT	V_{LCD}=0.92*2VBAT
10	1/3 BIAS	V_{LCD}=0.96*VBAT	V_{LCD}=0.96*2VBAT
11	1/3 BIAS	V_{LCD}=VBAT	V_{LCD}=2VBAT
Don't care	1/2 BIAS	N/A	V_{LCD}=2VBAT

V_{LCD} 与 LCD brightness adjustment

LCD related pin usage

P8620/40：

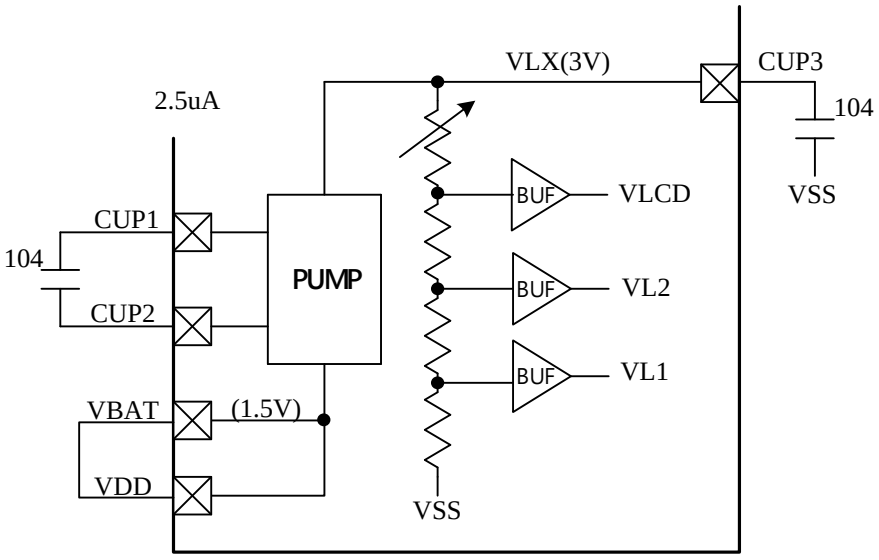
Pin VDD is connected to a capacitor to ground to stabilize the voltage of the chip. Pin CUP1 and pin CUP2 are used as SEG.



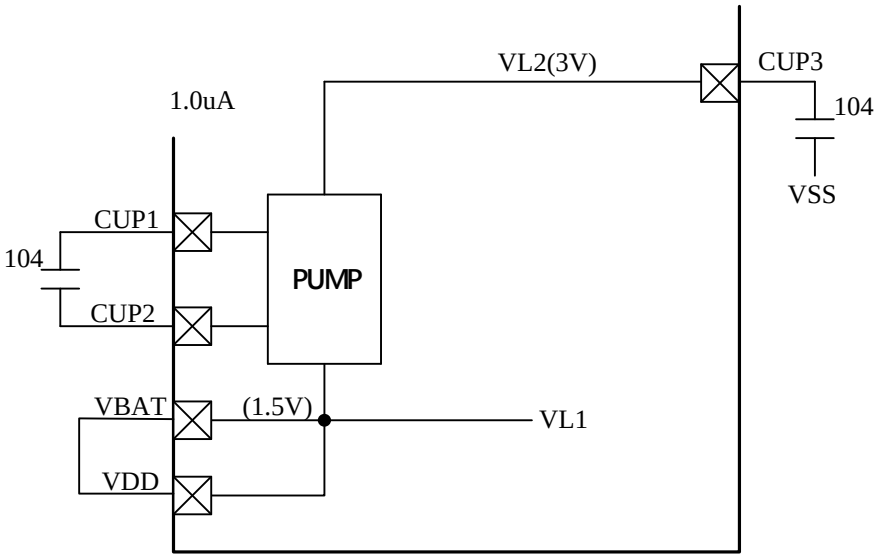
P8620/40, 1/3 Bias

P8625/45：

Pin CUP3 is connected to a capacitor to ground to stabilize the LCD voltage. Pin CUP1 and pin CUP2 are connected together through a capacitor to pump the LCD voltage.



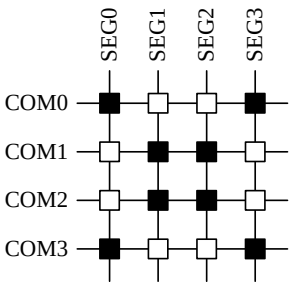
P8625/45, 1/3 Bias

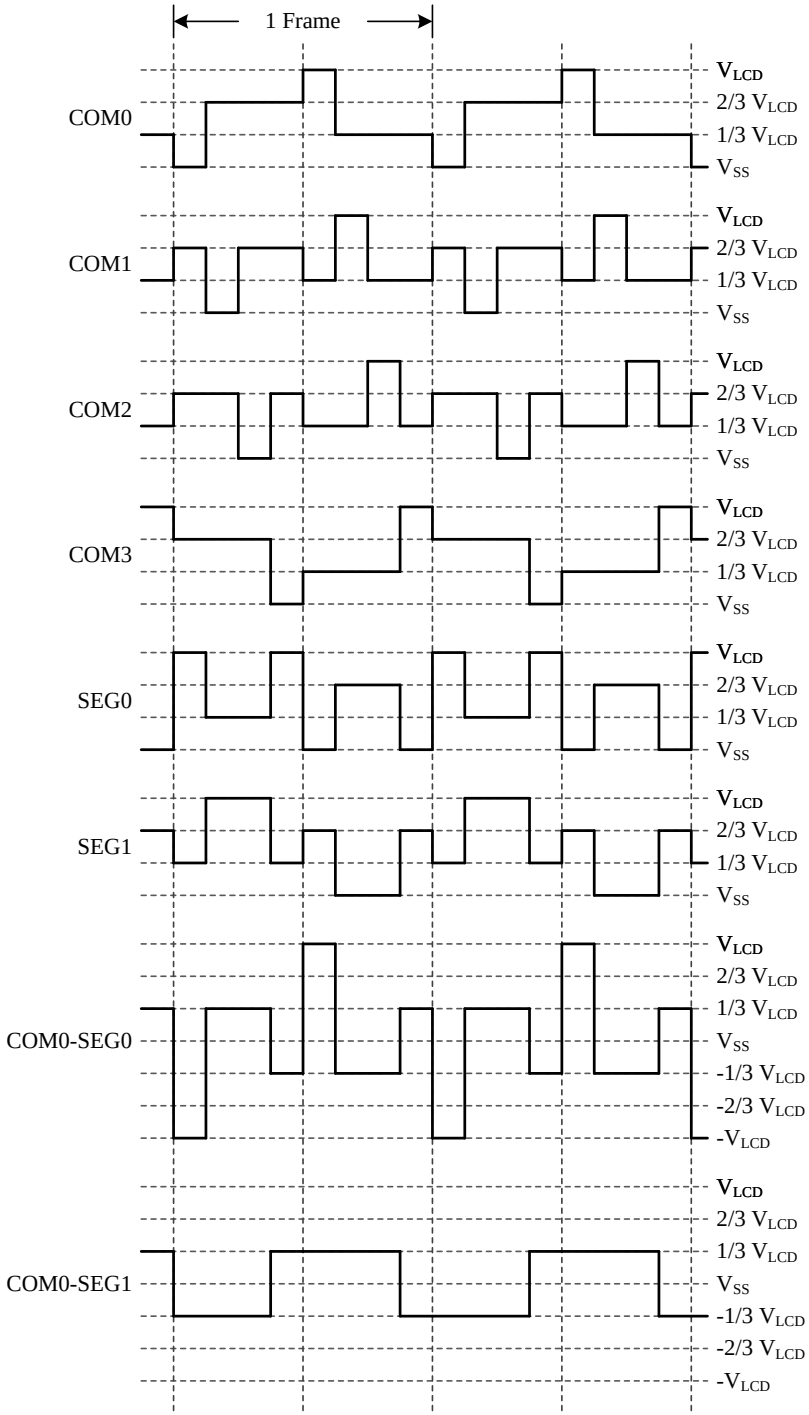


P8625/45, 1/2 Bias

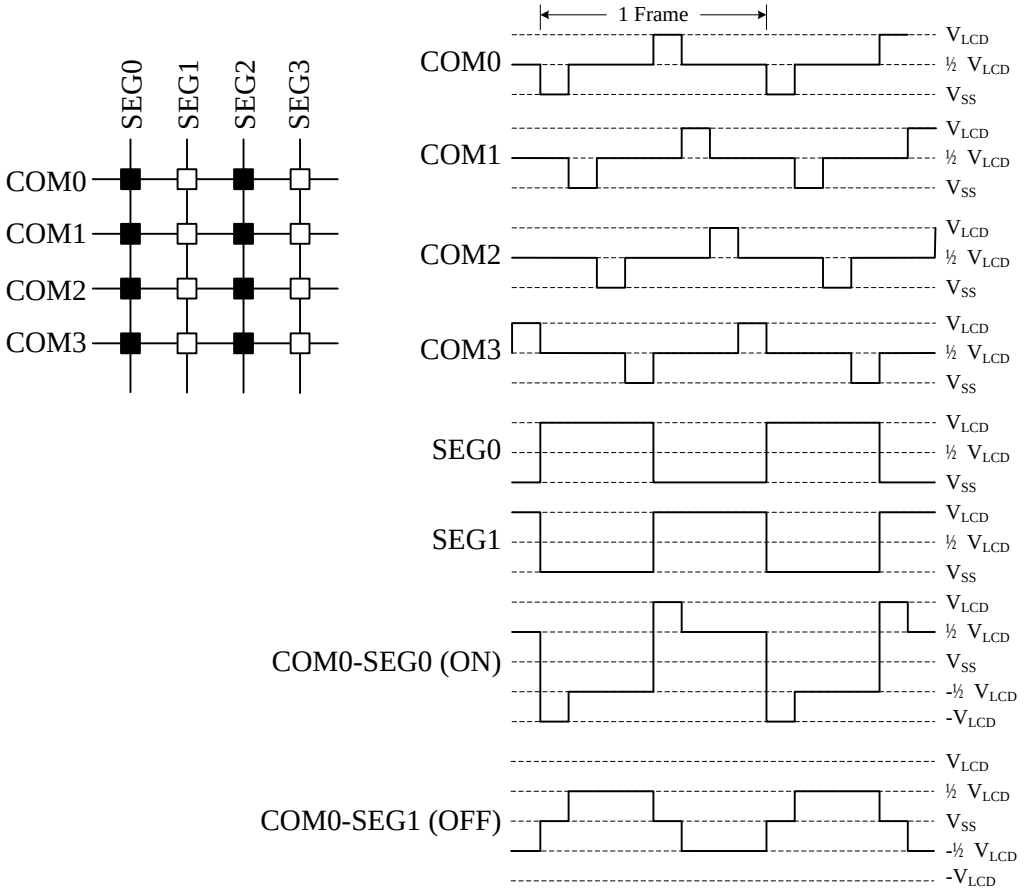
LCD Waveform Examples

1/4 Duty, 1/3 Bias Output Waveform





1/4 Duty, 1/2 Bias Output Waveform



F10	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LCDCTL	LCDON	LCDFRM		LCDUTY	LCDBIAS	–	LCDBV	
R/W	R/W	R/W	R/W	R/W	R/W	–	R/W	R/W
Reset	0	1	0	1	0	–	0	0

F10.7 **LCDON:** LCD driver enable
0: disable
1: enable

F10.6~5 **LCDFRM:** LCD frame rate, calculated by Slow-clock=32768Hz
00: 47Hz for 1/4 duty, 49Hz for 1/3 duty
01: 57Hz for 1/4 duty, 57Hz for 1/3 duty
10: 73Hz for 1/4 duty, 68Hz for 1/3 duty
11: 85Hz for 1/4 duty, 85Hz for 1/3 duty

F10.4 **LCDUTY:** LCD duty
0: 1/3 duty
1: 1/4 duty

F10.3 **LCDBIAS:** LCD Bias (P8620/40 must set 1/3 bias)
0: 1/2 Bias
1: 1/3 Bias

F10.1~0 **LCDBV:** LCD Brightness (only for 1/3 bias)
LCDON=1, V_{LCD}=
00: V_{BAT}*0.89 for P8620/40, V_{BAT}*2*0.89 for P8625/45
01: V_{BAT}*0.92 for P8620/40, V_{BAT}*2*0.92 for P8625/45
10: V_{BAT}*0.96 for P8620/40, V_{BAT}*2*0.96 for P8625/45
11: V_{BAT} for P8620/40, V_{BAT}*2 for P8625/45

R08	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PBMODL	PB3MOD		PB2MOD		PB1MOD		PB0MOD	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	1	0	1	0	1

R08.7~6 **PB3MOD:** PB3 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG25 output

R08.5~4 **PB2MOD:** PB2 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG26 output

R08.3~2 **PB1MOD:** PB1 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG27 output

R08.1~0 **PB0MOD:** PB0 pin mode
0x: Mode1, open-drain I/O without internal pull-up
10: Mode2, port data CMOS push-pull output
11: Mode3, LCD SEG28 output

F0E	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LBDCTL	CMPO	CMPVS			PWRSAV	VDDS	PUMPCKS	PORPDF
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset	–	0	0	0	0	0	0	–

F0E.1 **PUMPCKS:** LCD pump clock select (only for P8625/45)
0: Slow-clock / 4
1: Slow-clock / 8

	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0
R-Plane	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
40H	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0
41H	SEG3	SEG3	SEG3	SEG3	-	-	-	-
42H	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4
43H	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6
44H	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8
45H	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10
46H	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12
47H	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14
48H	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16
49H	SEG19	SEG19	SEG19	SEG19	SEG18	SEG18	SEG18	SEG18
4AH	SEG21	SEG21	SEG21	SEG21	SEG20	SEG20	SEG20	SEG20
4BH	SEG23	SEG23	SEG23	SEG23	SEG22	SEG22	SEG22	SEG22
4CH	SEG25	SEG25	SEG25	SEG25	SEG24	SEG24	SEG24	SEG24
4DH	SEG27	SEG27	SEG27	SEG27	SEG26	SEG26	SEG26	SEG26
4EH	SEG29	SEG29	SEG29	SEG29	SEG28	SEG28	SEG28	SEG28

*P8620/25 does not include SEG3, SEG10~SEG24

LCD RAM mapping

MEMORY MAP

F-Plane

Name	Address	R/W	Rst	Description
(F00) INDF				**Function related to: F-Plane R/W**
INDF	00.7~0	R/W	–	Not a physical register, addressing INDF actually point to the F-Plane register whose address is contained in the FSR register
(F01) TM0				**Function related to: Timer0**
TM0	01.7~0	R/W	0	Timer0 data
(F02) PCL				**Function related to: Program Counter**
PCL	02.7~0	R/W	0	Low-byte of Program Counter (PC[7~0])
(F03) STATUS				**Function related to: STATUS**
GB2	03.7	R/W	0	General purpose bit 2
GB1	03.6	R/W	0	General purpose bit 1
RAMBK	03.5	R/W	0	RAM Bank Selection
TO	03.4	R	0	WDT timeout flag, set by WDT timeout; cleared by POR, LVR, 'SLEEP' or 'CLRWDT' instruction
PD	03.3	R	0	Power down flag, set by 'SLEEP' instruction; cleared by POR, LVR or 'CLRWDT' instruction
Z	03.2	R/W	0	Zero flag
DC	03.1	R/W	0	Decimal Carry flag
C	03.0	R/W	0	Carry flag
(F04) FSR				**Function related to: F-Plane R/W**
GB3	04.7	R/W	0	General purpose bit 3
FSR	04.6~0	R/W	0	F-Plane File Select Register, indirect address mode pointer
(F05) PAD				**Function related to: Port A**
PAD	05.7~0	R	FF	Port A pin or "data register" state
		W		Port A output data register
(F06) PBD				**Function related to: Port B**
PBD	06.7~0	R	FF	Port B pin or "data register" state
		W		Port B output data register
(F08) INTIE				**Function related to: Interrupt Enable**
PWM0IE	08.7	R/W	0	PWM0 interrupt enable 0: disable 1: enable
TM1IE	08.6	R/W	0	Timer1 interrupt enable 0: disable 1: enable
RFCIE	08.5	R/W	0	RFC interrupt enable 0: disable 1: enable
TM0IE	08.4	R/W	0	Timer0 interrupt enable 0: disable 1: enable
T2IE	08.3	R/W	0	Timer2 interrupt enable 0: disable 1: enable
INT2IE	08.2	R/W	0	INT2 pin (PA7) interrupt enable 0: disable 1: enable
INT1IE	08.1	R/W	0	INT1 pin (PB4) interrupt enable 1: enable 0: disable
INT0IE	08.0	R/W	0	INT0 pin (PA0) interrupt enable 0: disable 1: enable

(F09) INTIF				Function related to: Interrupt Flag
PWM0IF	09.7	R	0	PWM0 interrupt event pending flag, Set by H/W while PWM0 period completes
		W		writing 0x7F to INTIF to clear this flag
TM1IF	09.6	R	0	Tmer1 interrupt event pending flag, Set by H/W while Timer1 overflows
		W		writing 0xBF to INTIF to clear this flag
RFCIF	09.5	R	0	RFC interrupt flag Under RFC1T=0: This flag is a counter overflow warning. When the RFC counter (RFCNT) overflows, H/W will set RFCIF to 1. Under RFC1T=1: This flag is the RFC cycle flag. Whenever the positive edge of RFCLK is triggered, H/W will set RFCIF to 1. When this flag is 1, RFCNT will suspend counting.
		W		writing 0xDF to INTIF to clear this flag
TM0IF	09.4	R	0	Timer0 interrupt event pending flag, set by H/W while Timer0 overflows
		W		writing 0xEF to INTIF to clear this flag
T2IF	09.3	R	0	Timer2 interrupt event pending flag, set by H/W while WKT time out
		W		writing 0xF7 to INTIF to clear this flag
INT2IF	09.2	R	0	INT2 (PA7) interrupt event pending flag, set by H/W at INT2 pin's rising/falling edge
		W		writing 0xFB to INTIF to clear this flag
INT1IF	09.1	R	0	INT1 (PB4) interrupt event pending flag, set by H/W at INT1 pin's rising/falling edge
		W		writing 0xFD to INTIF to clear this flag
INT0IF	09.0	R	0	INT0 (PA0) interrupt event pending flag, set by H/W at INT0 pin's rising/falling edge
		W		writing 0xFE to INTIF to clear this flag
(F0A) PCH				**Function related to: PROGRAM COUNT**
PCH	0A.3~0	R	0	4 MSBs of Program Counter (PC[11:8])
(F0B) CLKCTL				**Function related to: System Clock (Fsys)**
SCKTYPE	0B.7	R/W	0	Slow-clock Type 0: SIRC 1: SXT
SXTGAIN	0B.6~5	R/W	11	32768 SXT oscillator gain 0: lowest gain ... 3: highest gain
SLOWSTP	0B.4	R/W	0	Slow-clock Stop control 0: Slow-clock run 1: Slow-clock stop
FASTSTP	0B.3	R/W	1	Fast-clock Stop control 0: Fast-clock run 1: Fast-clock stop
CPUCKS	0B.2	R/W	0	System clock (Fsys) source selection 0: Slow-clock 1: Fast-clock
CPUPSC	0B.1~0	R/W	11	System clock source prescaler. Clock source is divided by 00: /8 01: /4 10: /2 11: /1
(F0C) MF0C				**Function related to: TM0/TM1/T2/Interrupt**
T2CLR	0C.7	R/W	0	T2 counter clear 0: T2 is counting 1: T2 is cleared, this bit is auto cleared by H/W
T2CKS	0C.6	R/W	0	T2 clock source selection 0: Slow-clock 1: Fsys/128

TM0STP	0C.5	R/W	0	Timer0 counter stop 0: Timer0 running 1: Timer0 stop
TM1STP	0C.4	R/W	0	Timer1 counter stop 0: Timer1 running 1: Timer1 stop
TM1CLR	0C.3	R/W	0	Timer1 clear and stop 0: Timer1 run 1: Timer1 clear and stop
INT2EDG	0C.2	R/W	0	INT2 pin (PA7) interrupt trigger edge select 0: falling edge 1: rising edge
INT1EDG	0C.1	R/W	0	INT1 pin (PB4) interrupt trigger edge select 0: falling edge 1: rising edge
INT0EDG	0C.0	R/W	0	INT0 pin (PA0) interrupt trigger edge select 0: falling edge 1: rising edge
(F0D) PWM0D				**Function related to: PWM0**
PWM0D	0D.7~0	R/W	80h	PWM0 duty, 0=0 PWM0CLK, 80h=128 PWM0CLK, FFh=255 PWM0CLK
(F0E) LBDCTL				**Function related to: Low battary detector(LBD), PWRSAV, LCD**
CMPO	0E.7	R	–	Low battery detect (LBD) result Compare result of bandgap voltage and VBAT voltage divider. CMPO=0 means the VBAT divided voltage is lower than bandgap voltage.
CMPVS	0E.6~4	R/W	0	LBD threshold voltage options. Select V_{BAT}/V_{LCD} resistor divider for Comparator input to compare with the 1.2V Bandgap reference voltage. P8620/40: 000: Comparator and Bandgap Disable 001: detect if V_{BAT}>2.4V 010: detect if V_{BAT}>2.5V; 011: detect if V_{BAT}>2.6V; 100: detect if V_{BAT}>2.7V; 101: detect if V_{BAT}>2.8V; 110: detect if V_{BAT}>2.9V; 111: detect if V_{BAT}>3.0V; P8625/45: 000: Comparator and Bandgap Disable 001: detect if V_{BAT}>1.20V 010:; detect if V_{BAT}>1.25V 011: detect if V_{BAT}>1.30V 100: detect if V_{BAT}>1.35V 101: detect if V_{BAT}>1.40V 110: detect if V_{BAT}>1.45V 111: detect if V_{BAT}>1.50V
PWRSAV	0E.3	R/W	0	Power saving control. (only for P8620/40) 0: Disable, $V_{DD}=V_{BAT}$ 1: Enable, $V_{DD}=V_{LCD}$*0.54 or V_{LCD}*0.625
VDDVS	0E.2	R/W	0	V_{DD} voltage selection (only for P8620/40) 0: V_{LCD}*0.54 1: V_{LCD}*0.625
PUMPCKS	0E.1	R/W	0	LCD pump clock select (only for P8625/45) 0: Slow-clock / 4 1: Slow-clock / 8
PORPDF	0E.0	R	–	POR Power Down Flag

(F0F) RFCTL				Function related to: RFC
RFCLR	0F.7	R/W	1	Clear RFC counter 0: RFC run 1: RFC clear
T1STPRFC	0F.6	R/W	0	(This option is only available under RFC1T=0) Timer1 overflow toggle signal (TM1TGL) to stop RFC counter 0: disable 1: enable
T0STPRFC	0F.5	R/W	0	(This option is only available under RFC1T=0) Timer0 overflow toggle signal (TM0TGL) to stop RFC counter 0: disable 1: enable
RFCSTP	0F.4	R/W	1	S/W stop RFC counter and oscillator 0: RFC run 1: RFC stop
SLOWPSC	0F.3~2	R/W	11	Slow clock divider for Timer0 00: /64 01: /16 10: /4 11: /1
RFCHS	0F.1~0	R/W	0	Select RFC oscillator channel 00: RFC0R (PA2) 01: RFC1R (PA0) 10: RFC2R (PA1) 11: RFC3R (PB7)
(F10) LCDCTL				**Function related to: LCD**
LCDON	10.7	R/W	0	LCD driver enable 0: disable 1: enable
LCDFRM	10.6~5	R/W	10	LCD frame rate, calculated by Slow-clock=32768Hz 00: 47Hz for 1/4 duty, 49Hz for 1/3 duty 01: 57Hz for 1/4 duty, 57Hz for 1/3 duty 10: 73Hz for 1/4 duty, 68Hz for 1/3 duty 11: 85Hz for 1/4 duty, 85Hz for 1/3 duty
LCDUTY	10.4	R/W	1	LCD duty 0: 1/3 duty 1: 1/4 duty
LCDBIAS	10.3	R/W	0	LCD bias (P8620/40 must set 1/3 bias) 0: 1/2 bias 1: 1/3 bias
LCDBV	10.1~0	R/W	0	LCD Brightness, V_{LCD} voltage level control. (only for 1/3 bias) LCDON=1, V_{LCD}= 00: V_{BAT}*0.89 for P8620/40, V_{BAT}*2*0.89 for P8625/45 01: V_{BAT}*0.92 for P8620/40, V_{BAT}*2*0.92 for P8625/45 10: V_{BAT}*0.96 for P8620/40, V_{BAT}*2*0.96 for P8625/45 11: V_{BAT} for P8620/40, V_{BAT}*2 for P8625/45
(F11) RFCNTH				**Function related to: RFC**
RFCNTH	11.7~0	R	0	RFC counter high byte, RFCNT[15:8]
(F12) RFCNTL				**Function related to: RFC**
RFCNTL	12.7~0	R	0	RFC counter low byte, RFCNT[7:0]
(F13) PWM1D				**Function related to: PWM1**
PWM1D	13.7~0	R/W	80	PWM1 duty
(F14) TM1				**Function related to: Timer1**
TM1	14.7~0	R/W	0	Timer1 data
(F15) PWMCLR				**Function related to: PWM0/PWM1**
PWM1CLR	15.1	R/W	0	PWM1 clear and hold 0: PWM1 running 1: PWM1 clear and hold
PWM0CLR	15.0	R/W	0	PWM0 clear and hold 0: PWM0 running 1: PWM0 clear and hold
(F16) LBDIE				**Function related to: Low battary detector(LBD)**
LBDIE	16.0	R/W	0	LBD interrupt enable
(F17) LBDIF				**Function related to: Low battary detector(LBD)**
LBDIF	17.0	R/W	0	LBD interrupt flag. Write 0 to clear this flag.

(F1C) RSR				**Function related to: R-Plane R/W**
RSR	1C.7~0	R/W	0	R-Plane file select register, indirect address mode pointer
(F1D) DPL				**Function related to: Table Read**
DPL	1D.7~0	R/W	0	Table read low address, data ROM pointer (DPTR[7:0])
(F1E) DPH				**Function related to: Table Read**
DPH	1E.3~0	R/W	0	Table read high address, data ROM pointer (DPTR[11:8])
(F1F) SRC_TRIM				**Function related to: SIRC**
SRC_TRIM	1F.4~0	R/W	1F	5-bit SIRC TRIM
User Data RAM				
FRAM	20~2F	R/W	–	F-Plane RAM Common area (16 Bytes)
	30~7F	R/W	–	F-Plane RAM Bank0 area (RAMBK=0, 80 Bytes)
	30~7F	R/W	–	F-Plane RAM Bank1 area (RAMBK=1, 80 Bytes)

R-Plane

Name	Address	R/W	Rst	Description
(R00) INDR				**Function related to: R-Plane R/W**
INDR	00.7~0	R/W	–	Not a physical register, addressing INDR actually point to the R-Plane register whose address is contained in the RSR register
(R01) TM0RLD				**Function related to: TM0**
TM0RLD	01.7~0	R/W	0	Timer0 reload Data
(R02) TM0CTL				**Function related to: TM0**
TM0CM	02.7	R/W	0	Timer0 Capture mode 0: Timer mode or Counter mode 1: Capture mode
T0ISRC	02.6	R/W	1	Timer0 Counter mode source 0: TM0CKI pin (PB4) 1: Slow-clock div 1/4/16/64 sets by SLOWPSC(F0F.3~2)
TM0EDGE	02.5	R/W	0	if TM0EDG=1, TM0CKI/CAPT input data will be reversed Timer0 prescaler counting edge for Counter mode 0: Rising edge 1: Falling edge Timer0 capture level for Capture mode 0: High level capture 1: Low level capture Timer1 capture edge for Capture mode 0: Falling edge capture 1: Rising edge capture
TM0CKS	02.4	R/W	0	Timer0 mode select 0 : Timer mode (Fsys) 1 : Counter mode (SCLK divided 1/4/16/64 or T0CKI(PB4))
TM0PSC	02.3~0	R/W	0	Timer0 clock source prescaler. Clock source is divided by 0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R03) PWRDN				**Function related to: Power Down**
PWRDN	03	W	–	Write this register (=SLEEP instruction) to enter IDLE or STOP Mode
(R04) WDTCLR				**Function related to: WDT**
WDTCLR	04	W	–	Write this register to clear WDT (=CLRWDT instruction)
(R05) PAMODH				**Function related to: Port A**
PA7MOD	05.6	R/W	0	0: Mode0, PA7 is open-drain I/O with internal pull-up 1: Mode1, PA7 is open-drain I/O without internal pull-up
PA6MOD	05.5~4	R/W	01	00: Mode0, PA6 is open-drain I/O with internal pull-up 01: Mode1, PA6 is open-drain I/O without internal pull-up 10: Mode2, PA6 is CMOS push-pull output 11: Mode3, PA6 is PWM0P CMOS push pull output
PA5MOD	05.3~2	R/W	01	00: Mode0, PA5 is open-drain I/O with internal pull-up 01: Mode1, PA5 is open-drain I/O without internal pull-up 10: Mode2, PA5 is CMOS push-pull output 11: Mode3, PA5 is RFCX input
PA4MOD	05.1~0	R/W	01	00: Mode0, PA4 is open-drain I/O with internal pull-up 01: Mode1, PA4 is open-drain I/O without internal pull-up 10: Mode2, PA4 is CMOS push-pull output

(R06) PAMODL				Function related to: Port A
PA3MOD	06.7~6	R/W	01	00: Mode0, PA3 is open-drain I/O with internal pull-up 01: Mode1, PA3 is open-drain I/O without internal pull-up 10: Mode2, PA3 is CMOS push-pull output
PA2MOD	06.5~4	R/W	01	00: Mode0, PA2 is open-drain I/O with internal pull-up 01: Mode1, PA2 is open-drain I/O without internal pull-up 10: Mode2, PA2 is CMOS push-pull output 11: Mode3, PA2 is RFC0R output
PA1MOD	06.3~2	R/W	01	00: Mode0, PA1 is open-drain I/O with internal pull-up 01: Mode1, PA1 is open-drain I/O without internal pull-up 10: Mode2, PA1 is CMOS push-pull output 11: Mode3, PA1 is RFC2R output
PA0MOD	06.1~0	R/W	01	00: Mode0, PA0 is open-drain I/O with internal pull-up 01: Mode1, PA0 is open-drain I/O without internal pull-up 10: Mode2, PA0 is CMOS push-pull output 11: Mode3, PA0 is RFC1R output
(R07) PBMODH				**Function related to: Port B**
PB7MOD	07.7~6	R/W	01	00: Mode0, PB7 is open-drain I/O with internal pull-up 01: Mode1, PB7 is open-drain I/O without internal pull-up 10: Mode2, PB7 is CMOS push-pull output 11: Mode3, PB7 is RFC3R output
PB6MOD	07.5~4	R/W	01	00: Mode0, PB6 is open-drain I/O with internal pull-up 01: Mode1, PB6 is open-drain I/O without internal pull-up 10: Mode2, PB6 is CMOS push-pull output 11: Mode3, PB6 is TCOUT output
PB5MOD	07.3~2	R/W	01	00: Mode0, PB5 is open-drain I/O with internal pull-up 01: Mode1, PB5 is open-drain I/O without internal pull-up 10: Mode2, PB5 is CMOS push-pull output 11: Mode3, PB5 is PWM1O output
PB4MOD	07.1~0	R/W	01	00: Mode0, PB4 is open-drain I/O with internal pull-up 01: Mode1, PB4 is open-drain I/O without internal pull-up 10: Mode2, PB4 is CMOS push-pull output
(R08) PBMODL				**Function related to: Port B**
PB3MOD	08.7~6	R/W	01	0x: Mode1, PB3 is open-drain I/O without internal pull-up 10: Mode2, PB3 is CMOS push-pull output 11: Mode3, PB3 is LCD SEG25 output
PB2MOD	08.5~4	R/W	01	0x: Mode1, PB2 is open-drain I/O without internal pull-up 10: Mode2, PB2 is CMOS push-pull output 11: Mode3, PB2 is LCD SEG26 output
PB1MOD	08.3~2	R/W	01	0x: Mode1, PB1 is open-drain I/O without internal pull-up 10: Mode2, PB1 is CMOS push-pull output 11: Mode3, PB1 is LCD SEG27 output
PB0MOD	08.1~0	R/W	01	0x: Mode1, PB0 is open-drain I/O without internal pull-up 10: Mode2, PB0 is CMOS push-pull output 11: Mode3, PB0 is LCD SEG28 output
(R0A) PWM0CTL				**Function related to: PWM0/T2/WDT**
PWM0CKS	0A.7	R/W	1	PWM0 clock source select 0: Slow-clock 1: Fast-clock
T2PSC	0A.6~5	R/W	0	T2 prescaler. T2 interrupt is T2 clock divided by 00: (32768*60) 01: 32768 10: 16384 11: 4096
PWM0PSC	0A.4~2	R/W	0	PWM0 clock prescaler 000: PWM0 clock is Slow/Fast clock divided by 128

				001: PWM0 clock is Slow/Fast clock divided by 64 010: PWM0 clock is Slow/Fast clock divided by 32 011: PWM0 clock is Slow/Fast clock divided by 16 100: PWM0 clock is Slow/Fast clock divided by 8 101: PWM0 clock is Slow/Fast clock divided by 4 110: PWM0 clock is Slow/Fast clock divided by 2 111: PWM0 clock is Slow/Fast clock divided by 1
PWM0NOE	0A.1	R/W	0	PWM0N output to PA1 pin 0: disable 1: enable
WDTPSC	0A.0	R/W	0	WDT Prescaler, 0: fsys/65536 1:fsys/32768 1.8sec/0.9sec @VDD=3V (Fsys = SIRC) 2.0sec/1.0sec @VDD=1.5V (Fsys = SIRC)
(R0B) PWM0PRD				**Function related to: PWM0**
PWM0PRD	0B.7~0	R/W	FF	PWM0 period, FFh=256 PWM0CLK, 7Fh=128 PWM0CLK
(R0C) PWM1CTL				**Function related to: PWM1**
PWM1CKS	0C.7	R/W	1	PWM1 clock source select 0: Slow-clock 1: Fast-clock
PWM1PSC	0C.4~2	R/W	0	PWM1 clock prescaler 000: PWM1 clock is Slow/Fast clock divided by 128 001: PWM1 clock is Slow/Fast clock divided by 64 010: PWM1 clock is Slow/Fast clock divided by 32 011: PWM1 clock is Slow/Fast clock divided by 16 100: PWM1 clock is Slow/Fast clock divided by 8 101: PWM1 clock is Slow/Fast clock divided by 4 110: PWM1 clock is Slow/Fast clock divided by 2 111: PWM1 clock is Slow/Fast clock divided by 1
(R0D) PWM1PRD				**Function related to: PWM1**
PWM1PRD	0D.7~0	R/W	FF	PWM1 period, FFh=256 PWM1CLK, 7Fh=128 PWM1CLK
(R10) TM1RLD				**Function related to: TM1**
TM1RLD	10.7~0	R/W	0	Timer1 reload Data
(R11) TM1CTL				**Function related to: TM1**
TM1CM	11.4	R/W	0	Timer1 Capture mode 0: Timer mode 1: Capture mode
TM1PSC	11.3~0	R/W	0	Timer1 clock source prescaler. Clock source is divided by 0000: Fsys/2 0101: Fsys/64 0001: Fsys/4 0110: Fsys/128 0010: Fsys/8 0111: Fsys/256 0011: Fsys/16 1xxx: Fsys/512 0100: Fsys/32
(R12) PBWKEN				**Function related to: Port B/Wake Up**
PBWKEN	12.7~0	R/W	0	PB7~PB0 low level wakeup 0: disable 1: enable

(R13) IAPCTL				Function related to: IAP
SV	13.6~4	R/W	3	VPP pump voltage select for IAP @ VBAT=3V (VPP recommended voltage: 6.75V) 0: VPP= 1.83*VBAT 4: VPP= 2.07*VBAT 1: VPP= 1.88*VBAT 5: VPP= 2.15*VBAT 2: VPP= 1.94*VBAT 6: VPP= 2.25*VBAT 3: VPP= 2.00*VBAT 7: VPP= 2.36*VBAT
IAPCKS	13.1~0	R/W	1	Select VPP pump clock source for IAP (IAPCKS recommended value is 0) 0: VPP pump clock source is FIRC/16 1: VPP pump clock source is FIRC/32 2: VPP pump clock source is FIRC/64 3: VPP pump clock source is FIRC/128
(R14) IAPCTL2				**Function related to: IAP**
WR_PULSE	14.2~0	R/W	3	(When VCC=3V, the recommended value of WR_PULSE is 3) (When VCC=3.2V, the recommended value of WR_PULSE is 4) Adjust the pulse width of the ROM IAP write signal. 0: The pulse width of the write signal is the shortest …… 7: The pulse width of the write signal is the longest
(R15) IAPEN				**Function related to: IAP**
IAPEN	15.7~0	W	-	Write 47h to enable main ROM IAP write
	15.0	R	-	IAPEN flag
(R16) IAPDATA				**Function related to: IAP**
IAPDATA	16.7~0	R/W	0	IAP write main ROM by moving data to IAPDATA (IAP address=DPTR)
(R17) RFC1T				**Function related to: RFC**
RFC1T	17.0	R/W	0	When RFC1T=1, the RFC counter clock source is FIRC, and the calculation time is one RFCLK cycle
(R18) HIX2				**Function related to: PWM0**
HIX2	18.0	R/W	0	(For P8625 and P8645 only) (need LCDON(F10.7) = 1) Used for PWM0 pin. When HIX2 = 1, the CMOS output high voltage of PWM0 (PA1 and PA6) will be boosted to 2*VCC.
(R1F) POROFF				**Function related to: POR**
POROFF	1F.7~0	W	–	Write this register with 0x37 to force POR disable
	1F.0	R	0	Flag indicates POR is forced to disable or not 1: POR is forced to disable
User Data RAM				
LCDRAM	40~4E	R/W	–	LCD RAM area (15 Bytes)
RRAM	60~FF	R/W	–	R-Plane RAM (160 Bytes) (only for P8640/45)

INSTRUCTION SET

Each instruction is a 14-bit word divided into an Op Code, which specifies the instruction type, and one or more operands, which further specify the operation of the instruction. The instructions can be categorized as byte-oriented, bit-oriented and literal operations list in the following table.

For byte-oriented instructions, “f” or “r” represents the address designator and “d” represents the destination designator. The address designator is used to specify which address in Program memory is to be used by the instruction. The destination designator specifies where the result of the operation is to be placed. If “d” is “0”, the result is placed in the W register. If “d” is “1”, the result is placed in the address specified in the instruction.

For bit-oriented instructions, “b” represents a bit field designator, which selects the number of the bit affected by the operation, while “f” represents the address designator. For literal operations, “k” represents the literal or constant value.

Field/Legend	Description
f	F-Plane Register File Address
r	R-Plane Register File Address
b	Bit address
k	Literal. Constant data or label
d	Destination selection field, 0: Working register, 1: Register file
W	Working Register
Z	Zero Flag
C	Carry Flag or/Borrow Flag
DC	Decimal Carry Flag or Decimal/Borrow Flag
PC	Program Counter
TOS	Top Of Stack
GIE	Global Interrupt Enable Flag (i-Flag)
[]	Option Field
( )	Contents
.	Bit Field
B	Before
A	After
←	Assign direction

Mnemonic		Op Code	Cycle	Flag Affect	Description
Byte-Oriented File Register Instruction					
ADDWF	f, d	00 0111 dfff ffff	1	C, DC, Z	Add W and "f"
ANDWF	f, d	00 0101 dfff ffff	1	Z	AND W with "f"
CLRF	F	00 0001 1fff ffff	1	Z	Clear "f"
CLRW		00 0001 0100 0000	1	Z	Clear W
COMF	f, d	00 1001 dfff ffff	1	Z	Complement "f"
DECF	f, d	00 0011 dfff ffff	1	Z	Decrement "f"
DECFSZ	f, d	00 1011 dfff ffff	1 or 2	-	Decrement "f", skip if zero
INCF	f, d	00 1010 dfff ffff	1	Z	Increment "f"
INCFSZ	f, d	00 1111 dfff ffff	1 or 2	-	Increment "f", skip if zero
IORWF	f, d	00 0100 dfff ffff	1	Z	OR W with "f"
MOVFW	f	00 1000 0fff ffff	1	-	Move "f" to W
MOVWF	f	00 0000 1fff ffff	1	-	Move W to "f"
MOVWR	r	01 1110 00rr rrrr	1	-	Move W to "r"
MOVRW	r	01 1111 00rr rrrr	1	-	Move "r" to W
RLF	f, d	00 1101 dfff ffff	1	C	Rotate left "f" through carry
RRF	f, d	00 1100 dfff ffff	1	C	Rotate right "f" through carry
SUBWF	f, d	00 0010 dfff ffff	1	C, DC, Z	Subtract W from "f"
SWAPF	f, d	00 1110 dfff ffff	1	-	Swap nibbles in "f"
TESTZ	f	00 1000 1fff ffff	1	Z	Test if "f" is zero
XORWF	f, d	00 0110 dfff ffff	1	Z	XOR W with "f"
Bit-Oriented File Register Instruction					
BCF	f, b	01 000b bbff ffff	1	-	Clear "b" bit of "f"
BSF	f, b	01 001b bbff ffff	1	-	Set "b" bit of "f"
BTFSC	f, b	01 010b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if clear
BTFSS	f, b	01 011b bbff ffff	1 or 2	-	Test "b" bit of "f", skip if set
Literal and Control Instruction					
ADDLW	k	01 1100 kkkk kkkk	1	C, DC, Z	Add Literal "k" and W
ANDLW	k	01 1011 kkkk kkkk	1	Z	AND Literal "k" with W
CALL	k	10 kkkk kkkk kkkk	2	-	Call subroutine "k"
CLRWDT		01 1110 0000 0100	1	TO, PD	Clear Watch Dog Timer
GOTO	k	11 kkkk kkkk kkkk	2	-	Jump to branch "k"
IORLW	k	01 1010 kkkk kkkk	1	Z	OR Literal "k" with W
MOVLW	k	01 1001 kkkk kkkK	1	-	Move Literal "k" to W
NOP		00 0000 0000 0000	1	-	No operation
RET		00 0000 0100 0000	2	-	Return from subroutine
RETI		00 0000 0110 0000	2	-	Return from interrupt
RETLW	k	01 1000 kkkk kkkK	2	-	Return with Literal in W
SLEEP		01 1110 0000 0011	1	TO, PD	Go into Power-down mode, Clock oscillation stops
TABRH		00 0000 0101 1000	2	-	Lookup ROM high data to W
TABRL		00 0000 0101 0000	2	-	Lookup ROM low data to W
XORLW	k	01 1101 kkkk kkkk	1	Z	XOR Literal "k" with W

ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings (T_A =25℃)

Parameter	Rating	Unit
Supply voltage	Vss-0.3 ~ Vss+3.6	V
Operating voltage (P8620/40)	POR ~ Vss+3.6	
Operating voltage (P8625/45)	LVCR ~ Vss+1.8	
Input voltage	V_{SS} -0.3 ~ V_{BAT} +0.3	V
Output voltage	V_{SS} -0.3 ~ V_{BAT} +0.3	
Output current high per all pins	–50	mA
Output current low per all pins	+100	
Operating temperature	-40 ~ +85	℃
Storage temperature	-65 ~ +150	

2. DC Characteristics (T_A =25℃)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	P8620/40: V_{BAT}=3V P8625/45: V_{BAT}=1.5V		0.6V_{BAT}	–	–	V
Input Low Voltage	V_{IL}			–	–	0.3V_{BAT}	
I/O Source/Sink Current (except PA7)	I_{OH}	V_{OH}=2.7V	P8620/40 V_{BAT}=3V	–	6.5	–	mA
	I_{OL}	V_{OL}=0.3V		–	15	–	
I/O Source/Sink Current (except PA7)	I_{OH}	V_{OH}=1.35V	P8625/45 V_{BAT}=1.5V	–	1.5	–	
	I_{OL}	V_{OL}=0.15V		–	5	–	
I/O Source/Sink Current (PA7)	I_{OH}	V_{OH}=2.7V	P8620/40 V_{BAT}=3V	–	N/A	–	
	I_{OL}	V_{OL}=0.3V		–	15	–	
I/O Source/Sink Current (PA7)	I_{OH}	V_{OH}=1.35V	P8625/45 V_{BAT}=1.5V	–	N/A	–	
	I_{OL}	V_{OL}=0.15V		–	5	–	
Input leakage current (pin high)	I_{ILH}	all Input	V_{IN}=V_{BAT}	–	–	1	uA
Input leakage current (pin low)	I_{ILL}		Vin=0V	–	–	–1	
Power Supply Current	I_{BAT}	FIRC, 2.7MHz	P8620/40 V_{BAT}=3V V_{DD}=3V	–	550	–	uA
		SIRC, 36KHz		–	15	–	
		SXT, 32KHz			15		
		FIRC, 0.9MHz	P8620/40 V_{BAT}=3V V_{DD}=1.5V	–	100	–	
		SIRC, 32KHz		–	8	–	
		SXT, 32KHz		–	8	–	
		FIRC, 0.9MHz	P8625/45 V_{BAT}=1.5V	–	90	–	
		SIRC, 32KHz		–	5	–	
		SXT, 32KHz		–	5	–	
Timepiece Current CPU Off, LCD On, 32K Crystal oscillating	I_{BAT}	P8620/40, V_{BAT}=3V, V_{DD}=3V			7		uA
		P8620/40, V_{BAT}=3V, V_{DD}=1.5V		–	3	–	
		P8625/45, V_{BAT}=1.5V, 1/3 LCD bias		–	4	–	
		P8625/45, V_{BAT}=1.5V, 1/2 LCD bias		–	2	–	
Stop Mode Current	I_{BAT}	P8620/40, V_{BAT}=3V		–	1.2	–	uA

		P8625/45, V_{BAT}=1.5V, 1/3 LCD bias	–	1.0	–	
		P8625/45, V_{BAT}=1.5V, 1/2 LCD bias	–	0.1	–	
Pull-Up Resistor	PA7	P8625/45, V_{BAT}=1.5V, LVDON=1	–	2	–	MΩ
		P8620/40, V_{BAT}=3V	–	60	–	KΩ
		P8625/45, V_{BAT}=1.5V, LVDON=0	–	250	–	
	PA0~PA6, PB4~PB7	P8620/40, V_{BAT}=3V	–	60	–	
		P8625/45, V_{BAT}=1.5V	–	250	–	
	PB0~PB3	–	–	N/A	–	
Power On Reset	V_{POR}	P8620/40	1.45	1.65	1.85	V
		P8625/45	0.75	0.95	1.15	

3. Clock Timing

Parameter	Sym	Conditions	Min	Typ	Max	Unit
FIRC Clock Frequency	F_{FIRC}	V_{DD}=3V	–	2.7	–	MHz
		V_{DD}=1.5V	–	0.9	–	
SIRC Clock Frequency	F_{SIRC}	V_{DD}=3V	-10%	37	+10%	KHz
		V_{DD}=1.5V	-5%	32	+5%	

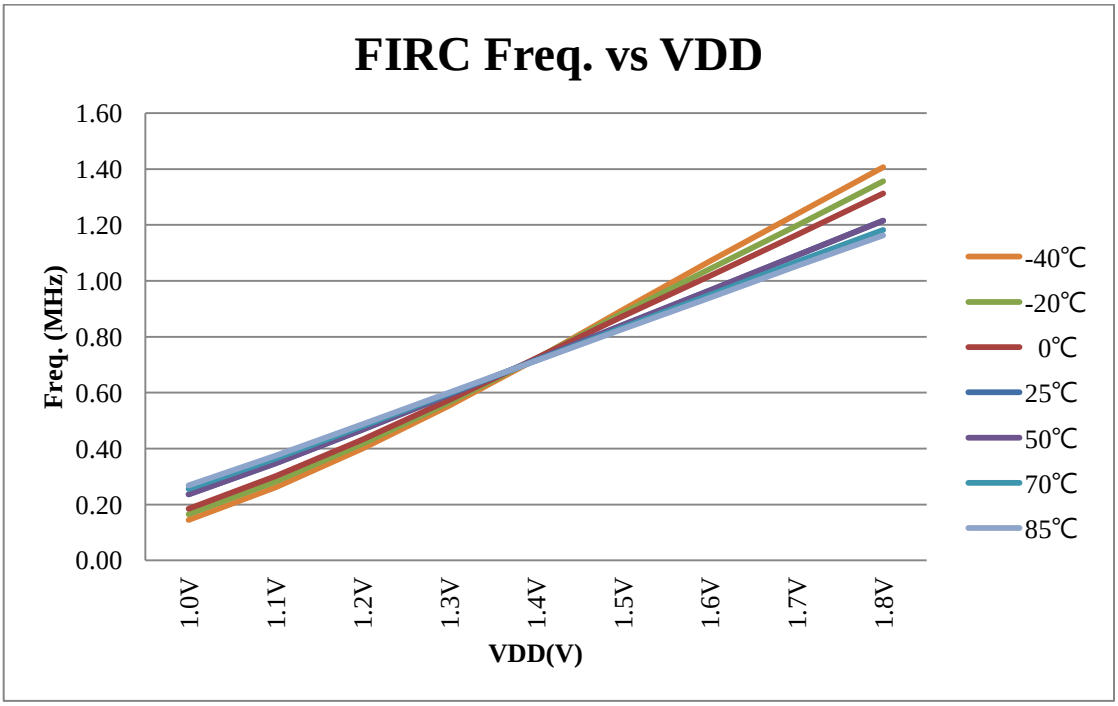
4. Low Battery Voltage Detection (LBD)

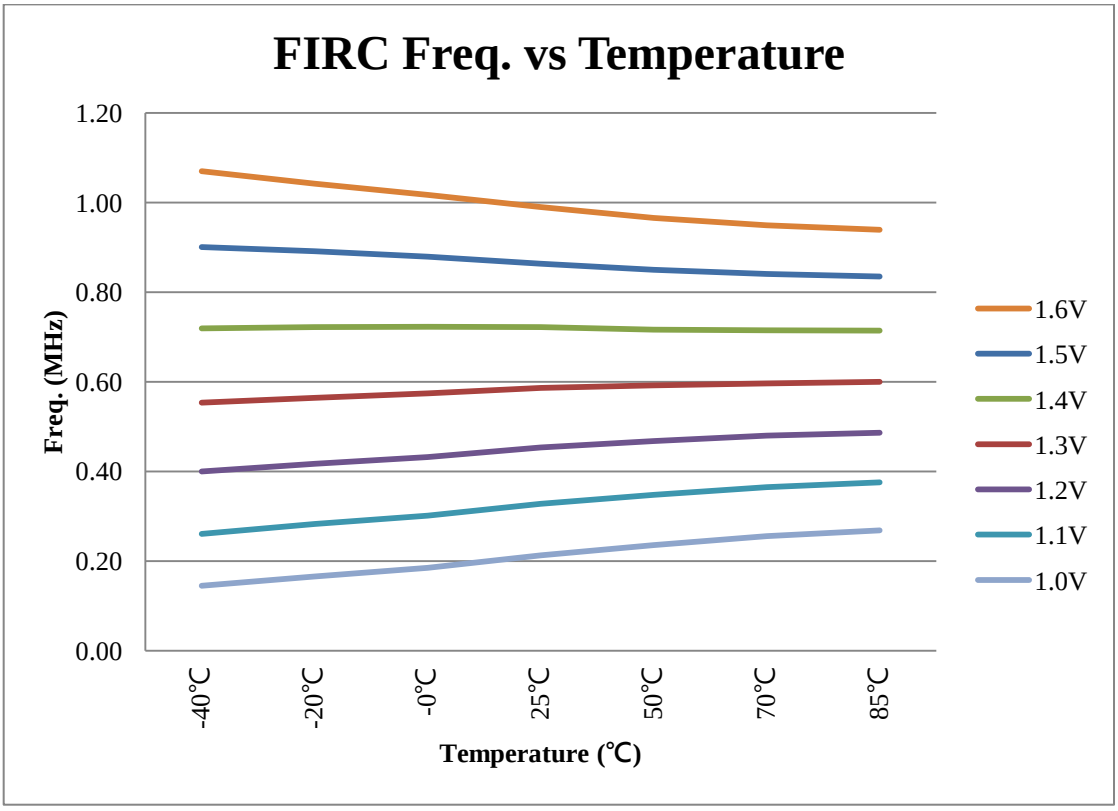
Parameter	Sym	Conditions	Min	Typ	Max	Unit
BandGap Reference Voltage	V_{BG}	V_{BAT}=3V, 25℃	1.14	1.2	1.26	V
		V_{BAT}=3V, –40℃~85℃	1.12	1.2	1.28	
LBD Delay Time	T_{LBD}	-	-	20	-	us

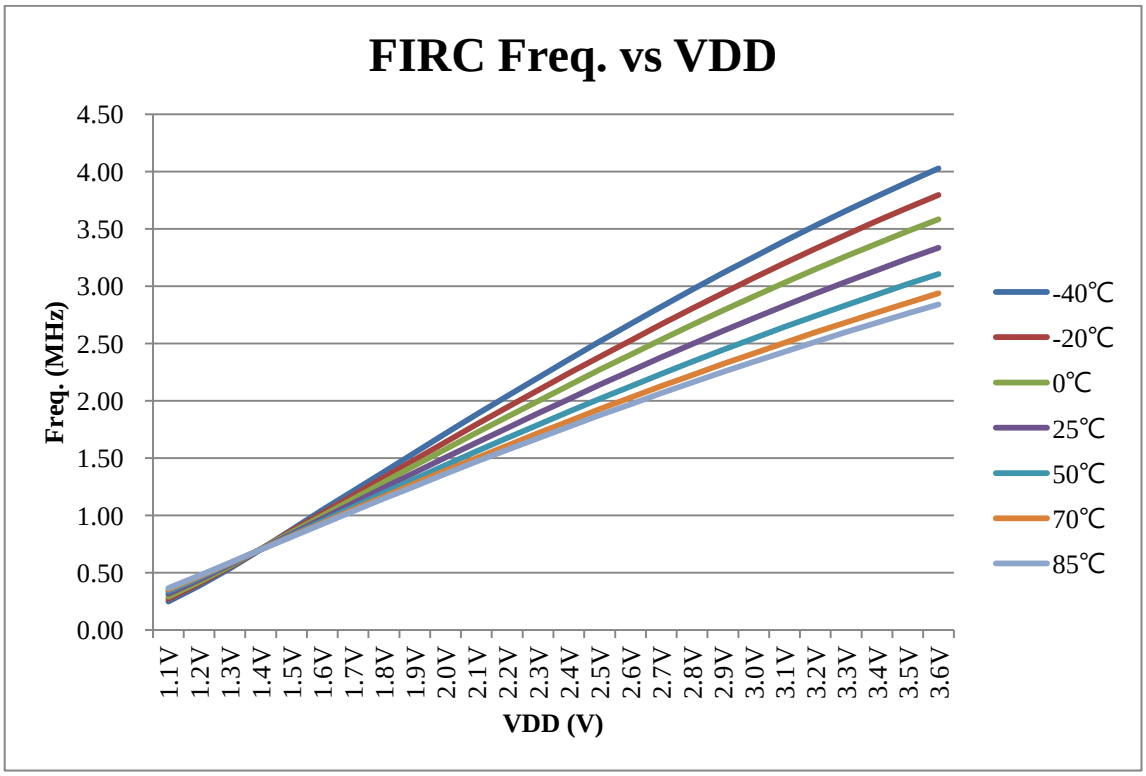
5. Slow Crystal Oscillator (SXT) (Xin=15pF, Xout=15pF)

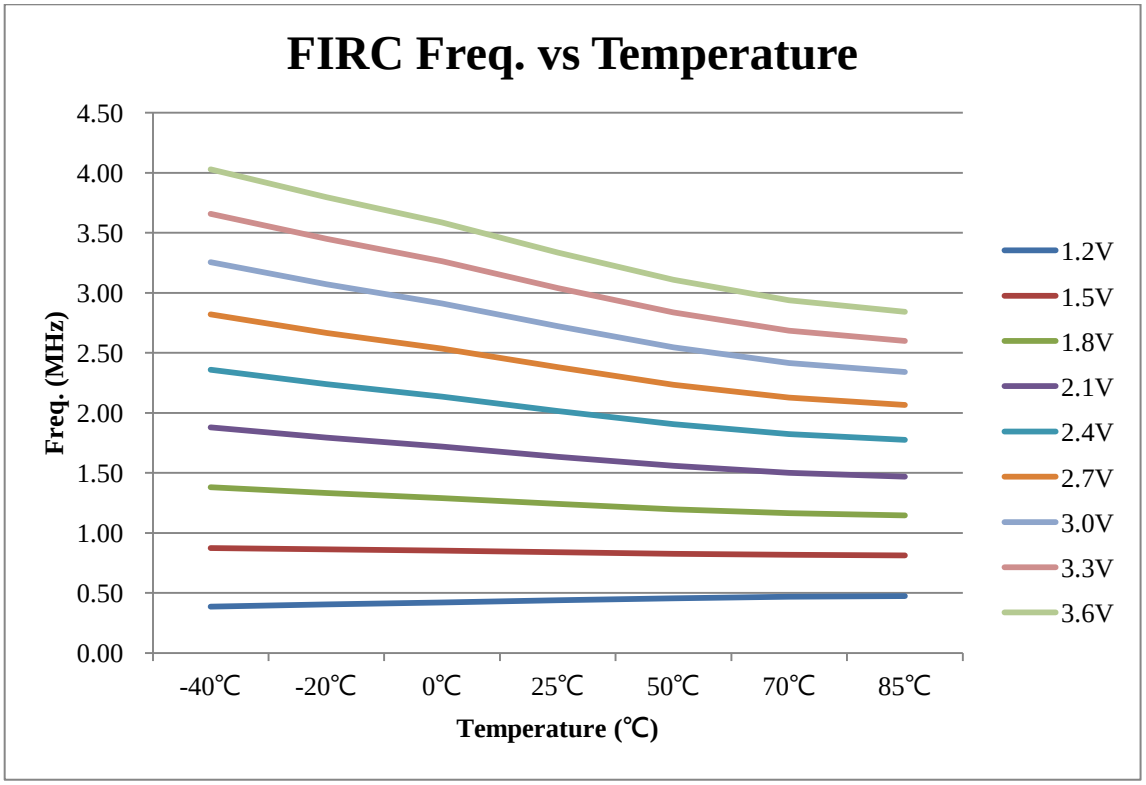
Parameter	Sym	Conditions	Min	Typ	Max	Unit
Oscillator start-up voltage	VDD	gain=3, 25℃~70℃	1.25	-	-	V
Oscillator start-up voltage	VDD	gain=3, 0℃~70℃	1.30	-	-	V
Oscillator start-up voltage	VDD	gain=3, –20℃~70℃	1.35	-	-	V
Oscillator Hold Voltage	VDD	gain=3, –20℃~70℃	1.20	-	-	V

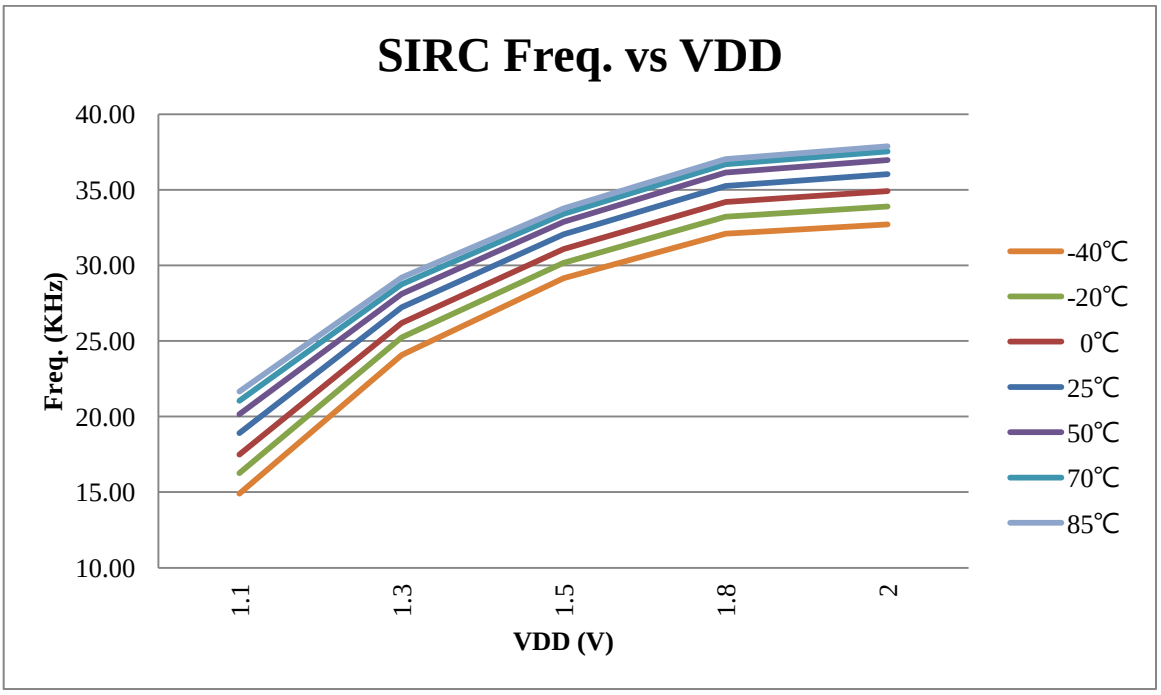
6. Characteristic Graph

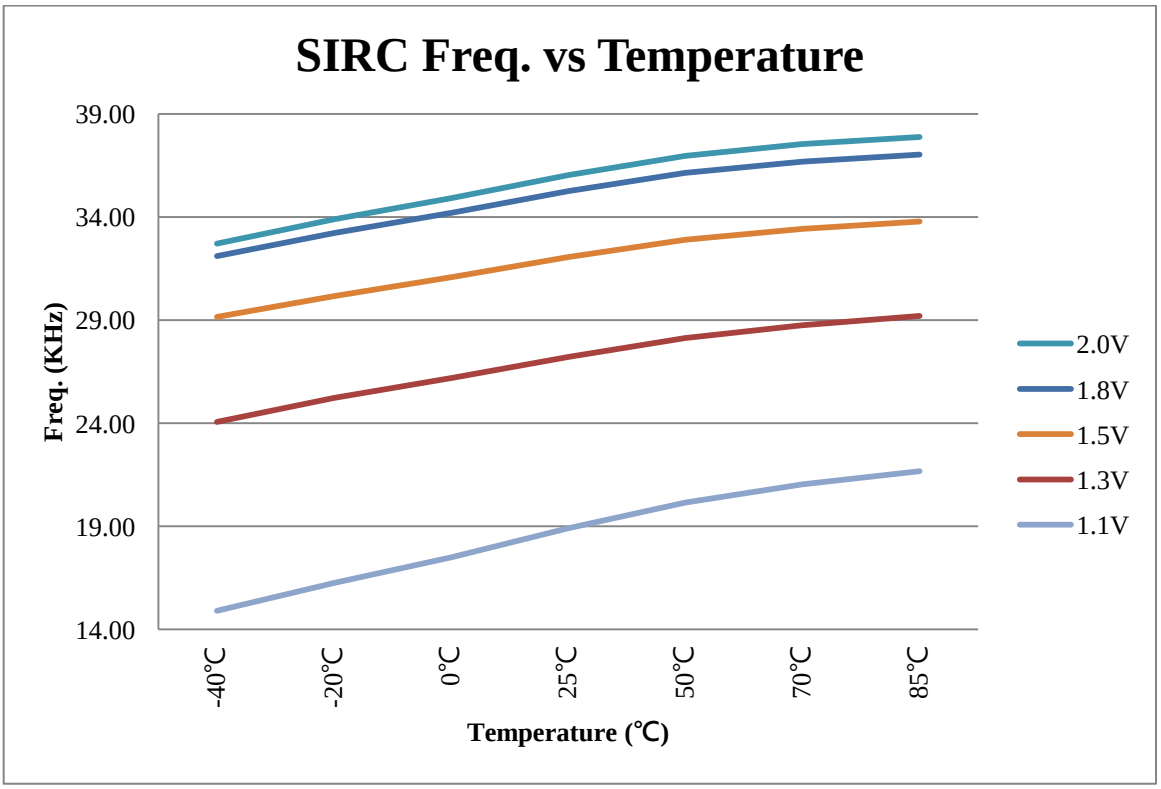


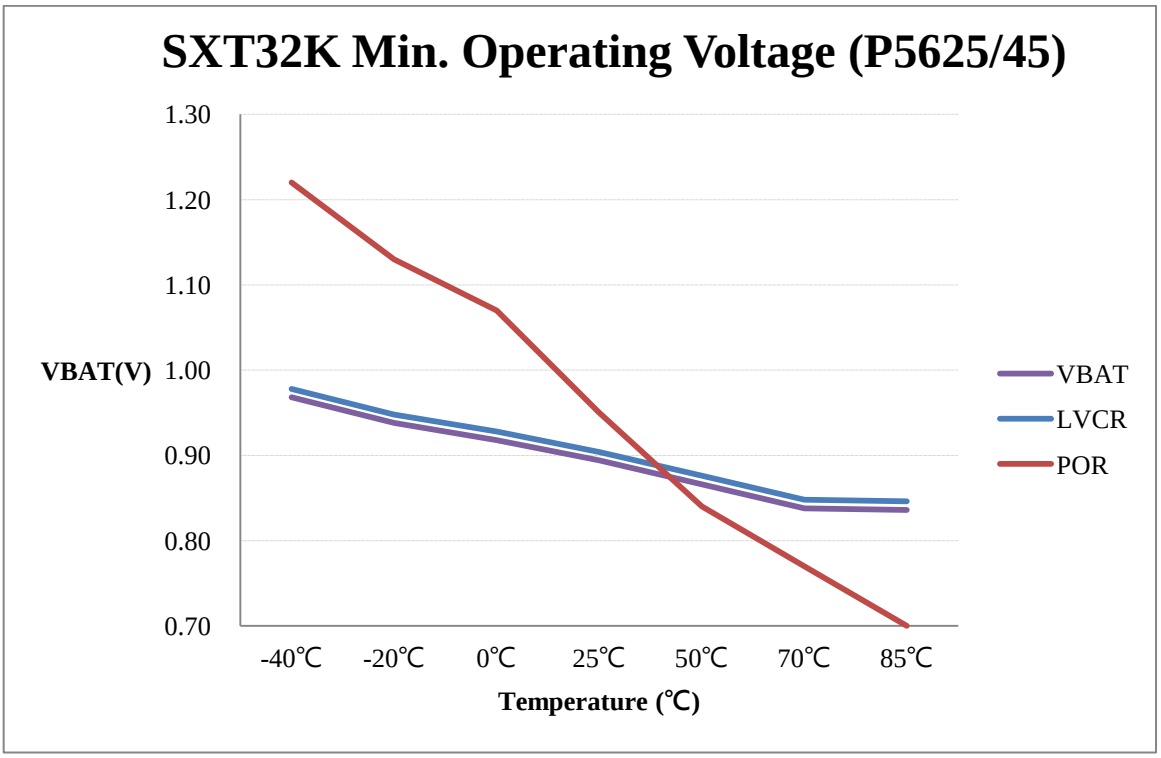



FIRC Freq. vs VDD
Freq. (MHz)
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
1.1V 1.2V 1.3V 1.4V 1.5V 1.6V 1.7V 1.8V 1.9V 2.0V 2.1V 2.2V 2.3V 2.4V 2.5V 2.6V 2.7V 2.8V 2.9V 3.0V 3.1V 3.2V 3.3V 3.4V 3.5V 3.6V
VDD (V)
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃


FIRC Freq. vs Temperature
Freq. (MHz)
4.50
4.00
3.50
3.00
2.50
2.00
1.50
1.00
0.50
0.00
-40℃ -20℃ 0℃ 25℃ 50℃ 70℃ 85℃
Temperature (℃)
1.2V
1.5V
1.8V
2.1V
2.4V
2.7V
3.0V
3.3V
3.6V

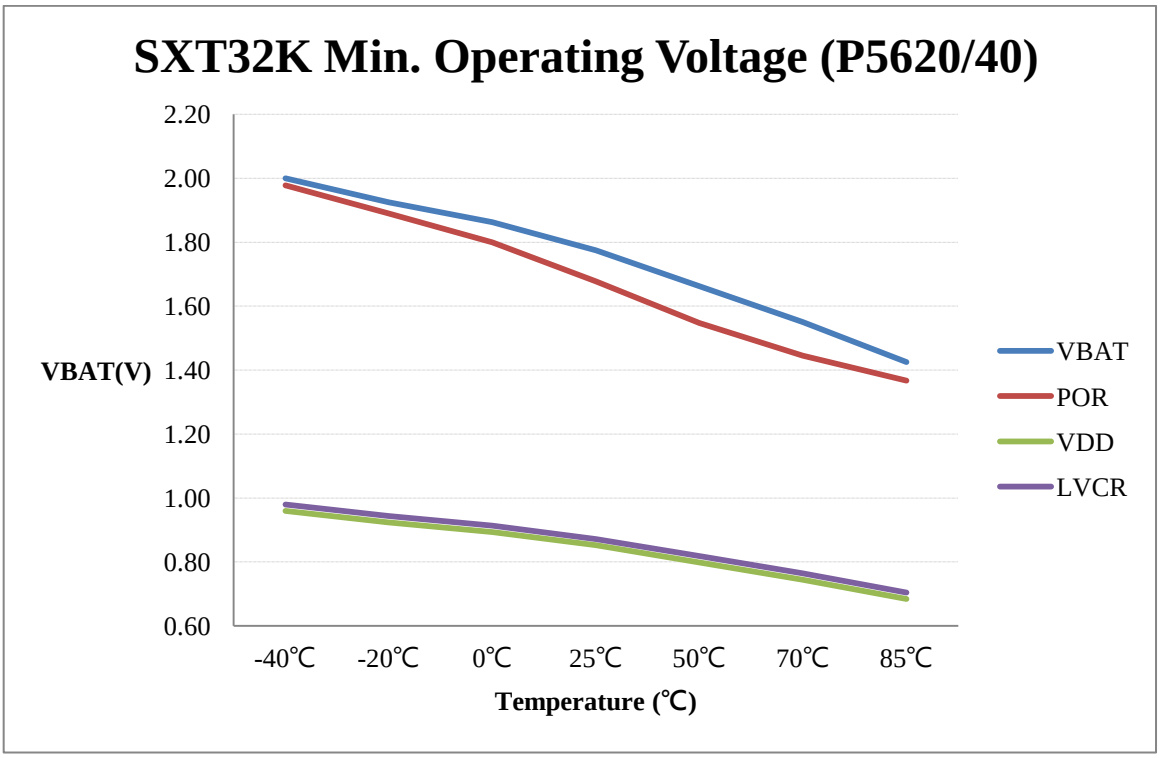

SIRC Freq. vs VDD
40.00
35.00
30.00
25.00
20.00
15.00
10.00
Freq. (KHz)
1.1
1.3
1.5
1.8
2
VDD (V)
-40℃
-20℃
0℃
25℃
50℃
70℃
85℃


SIRC Freq. vs Temperature
39.00
34.00
29.00
24.00
19.00
14.00
Freq. (KHz)
-40°C
-20°C
0°C
25°C
50°C
70°C
85°C
Temperature (℃)
2.0V
1.8V
1.5V
1.3V
1.1V



SXT32K Min. Operating Voltage (P8625/45)

Note:
1. LVCR (ROM error reset, follow the minimum operating voltage) is always enabled.
2. POR (power-on reset or low-voltage reset) can be disabled by the POROFF register.
3. Power on VBAT must exceed POR (1.1V@25C). Set POROFF = 0x37 (POR disabled) to obtain the lowest VBAT operation.



SXT32K Min. Operating Voltage (P8620/40)
under LCDBV=00,VDDVS=0 & PWRSAV=1

Note:

1. LVCR (ROM error reset, follow the minimum operating voltage) is always enabled.
2. POR (power-on reset or low-voltage reset) can be disabled by the POROFF register.
3. Power on VBAT must exceed POR (1.6V@25C). Set POROFF = 0x37 (disable POR) to obtain the lowest VBAT operation.
4. Under the condition of LCDBV=00, VDDVS=0 and PWRSAV=1, VDD (chip internal voltage) = VLCD * 0.54 = VBAT*0.89*0.54

7. The main difference in DC characteristics with M5620/25/40/45

(1) FIRC has a slower frequency (2.7MHz@3V, 0.9MHz@1.5V)

(2) The frequency of SIRC under 3V is slower (36KHz@3V)

(3) The SIRC characteristic is that the frequency increases with temperature

(4) Provide SIRC frequency calibration under 1.5V (±5%@1.5V)

(5) If 3V is used under the condition of PWRSAV=0, it will consume more power (~7uA), it is recommended to use PWRSAV=1

(6) In STOP mode, LCD uses 1/3 bias conditions, it consumes more power (1.2uA@3V, 1uA@1.5V)

(7) The GPIO pull-up resistor value under 1.5V is reduced

(8) Increase PA7 sink current

(9) Improve the minimum working voltage at low temperature (-40℃)

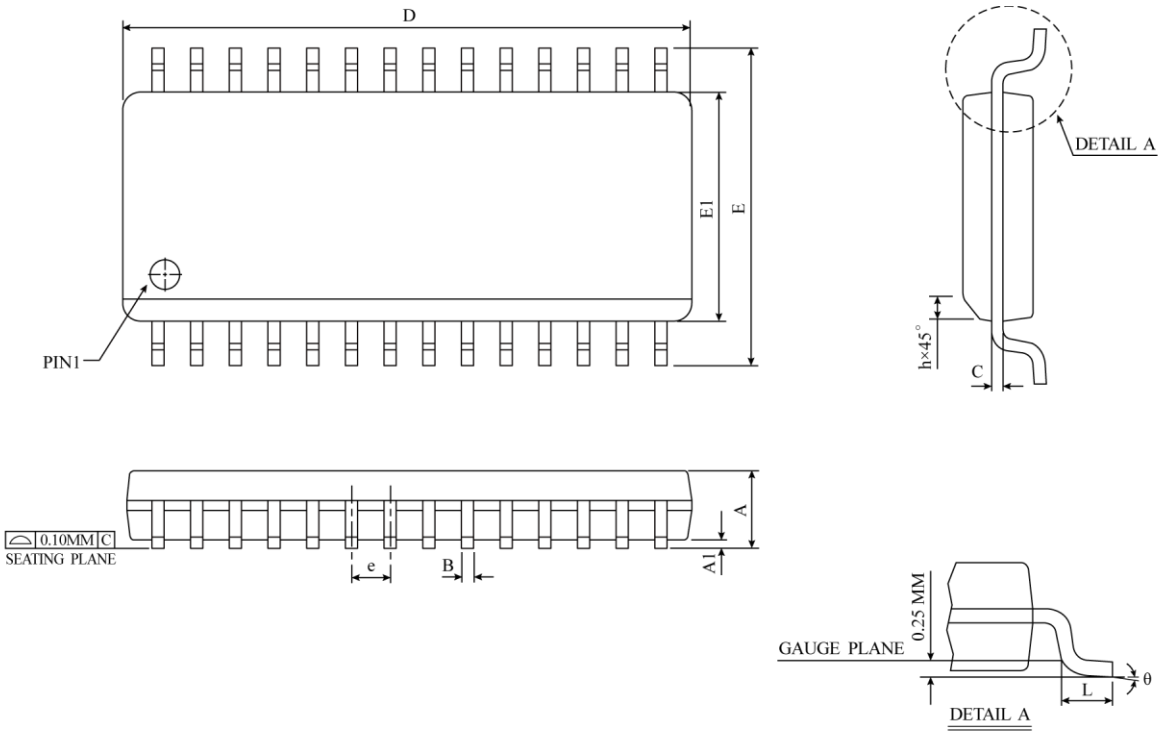
PACKAGING INFORMATION

Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

The ordering information:

Ordering number	Package
TM57P8620-OTP	Wafer / Dice blank chip
TM57P8620-COD	Wafer / Dice with code
TM57P8620-OTP-23	SOP 28 pin (300mil)
TM57P8625-OTP	Wafer / Dice blank chip
TM57P8625-COD	Wafer / Dice with code
TM57P8625-OTP-23	SOP 28 pin (300mil)
TM57P8640-OTP	Wafer / Dice blank chip
TM57P8640-COD	Wafer / Dice with code
TM57P8640-OTP-37	SSOP 48 pin (300mil)
TM57P8640-OTP-72	LQFP 48 pin (7*7*1.4mm)
TM57P8645-OTP	Wafer / Dice blank chip
TM57P8645-COD	Wafer / Dice with code
TM57P8645-OTP-37	SSOP 48 pin (300mil)
TM57P8645-OTP-72	LQFP 48 pin (7*7*1.4mm)

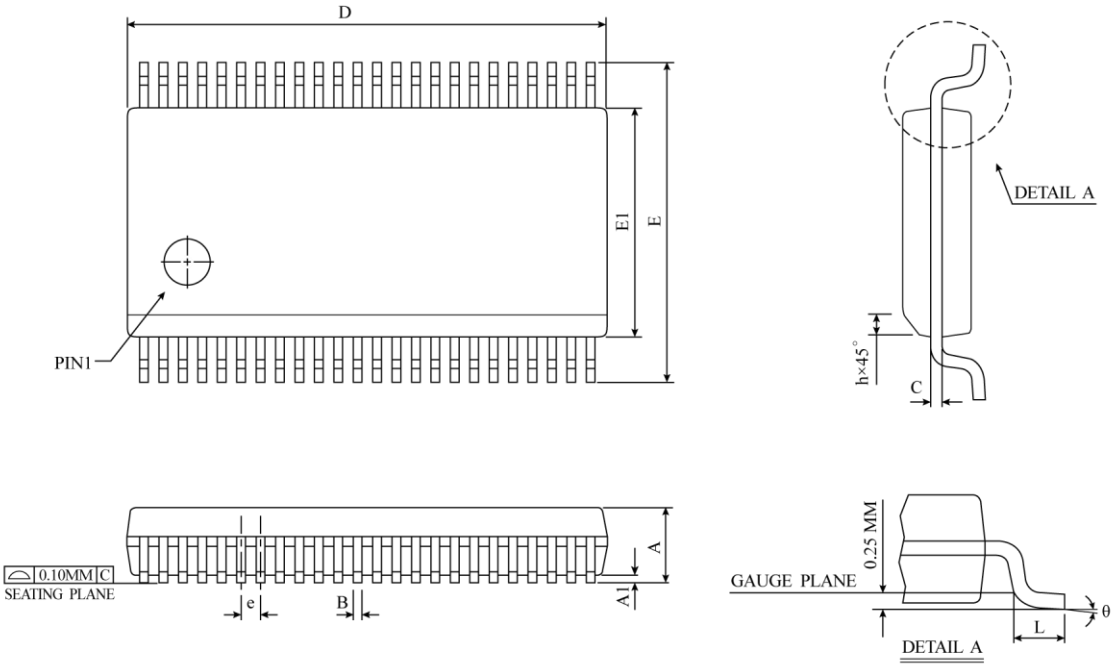
SOP-28 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.35	2.50	2.65	0.0926	0.0985	0.1043
A1	0.10	0.20	0.30	0.0040	0.0079	0.0118
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.23	0.28	0.32	0.0091	0.0108	0.0125
D	17.70	17.90	18.10	0.6969	0.7047	0.7125
E	10.00	10.33	10.65	0.3940	0.4425	0.4910
E1	7.40	7.50	7.60	0.2914	0.2953	0.2992
e	1.27 BSC			0.050 BSC		
h	0.25	0.50	0.75	0.0100	0.0195	0.0290
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-013 (AE)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

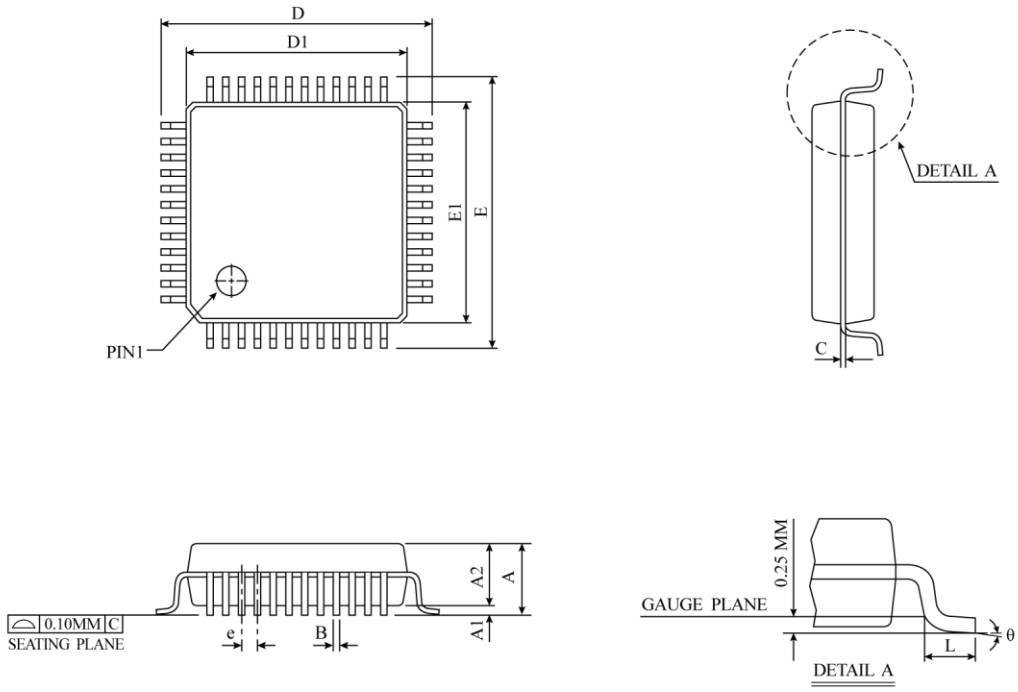
SSOP-48 (300mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.413	2.604	2.794	0.095	0.103	0.110
A1	0.203	0.305	0.406	0.008	0.012	0.016
B	0.203	0.273	0.343	0.008	0.011	0.014
C	0.127	0.191	0.254	0.005	0.008	0.010
D	15.748	15.875	16.002	0.620	0.625	0.630
E	10.033	10.351	10.668	0.395	0.408	0.420
E1	7.391	7.493	7.595	0.291	0.295	0.299
e	0.635 BSC			0.025 BSC		
L	0.508	0.762	1.016	0.020	0.030	0.040
θ	0°	4°	8°	0°	4°	8°
JEDEC	M0-118 (AA)					

△ * NOTES : DIMENSION " D " DOES NOT INCLUDE MOLD FLASH,
PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED
0.1524 MM (0.006 INCH) PER SIDE.

LQFP-48 (7×7mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	1.60	-	-	0.063
A1	0.05	0.10	0.15	0.001	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09	0.15	0.20	0.004	0.006	0.008
D	9.00 BSC			0.354 BSC		
D1	7.00 BSC			0.276 BSC		
E	9.00 BSC			0.354 BSC		
E1	7.00 BSC			0.276 BSC		
e	0.50 BSC			0.020 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
θ	0°	3.5°	7°	0°	3.5°	7°
JEDEC	MS-026 (BBC)					

△ * NOTES : DIMENSION " D1 " AND " E1 " DO NOT INCLUDE MOLD PROTRUSIONS. ALLOWABLE PROTRUSIONS IS 0.25 mm PER SIDE. " D1 " AND " E1 " ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMACH.