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TK8813E

Three Key Touch Detector for TWS

DATA SHEET Rev 0.91

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AMENDMENT HISTORY

Version	Date	Description
V0.90	May,2020	New release.
V0.91	Aug,2020	Modify package Information Modify Device List

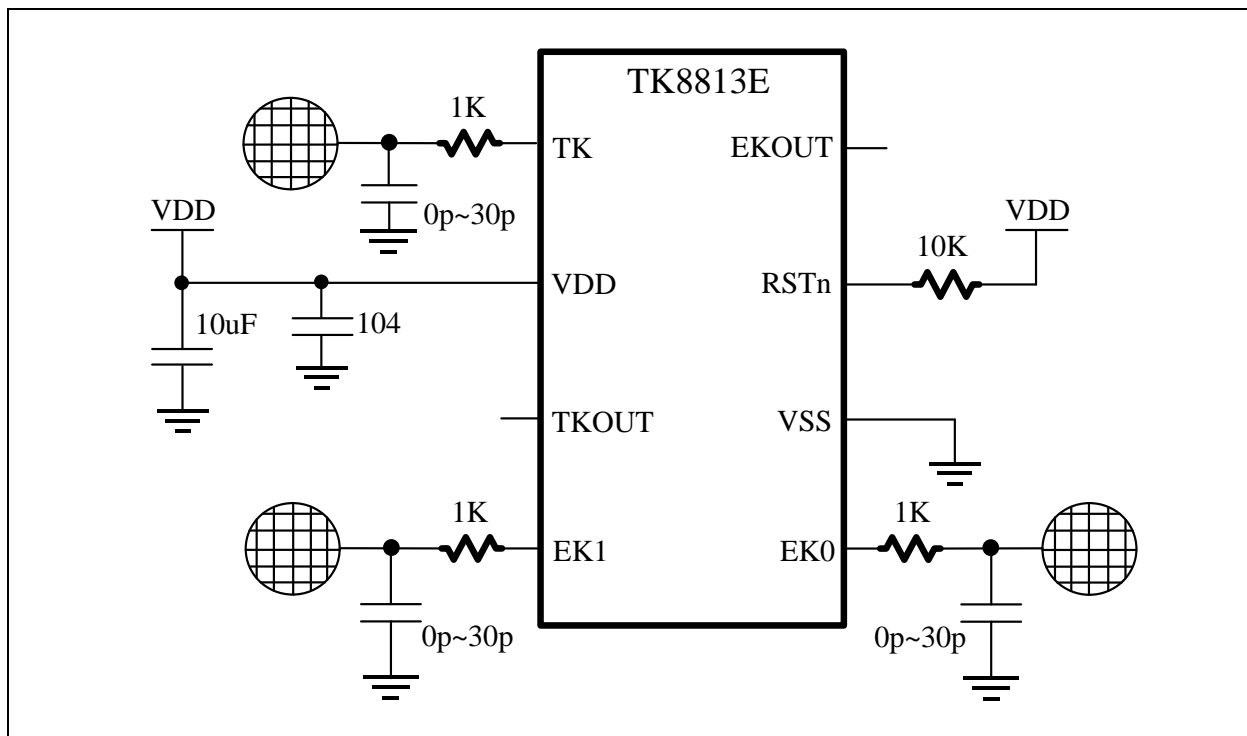
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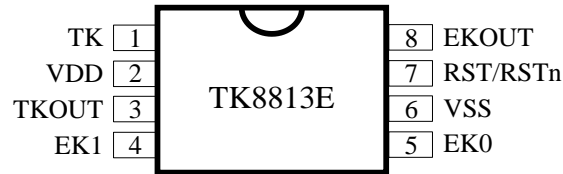
FEATURES

1. Three Key Touch Detector (2 EK + 1 TK), tailor to TWS earphone
2. Operation Voltage: 2.2V~5.5V
3. Operation Current(TK8813E1): Normal mode =5.5uA, Low Power mode=1.9uA @V_{DD}=3V
4. Enter Low Power mode after no activity for 10 second
5. Response Time: Normal mode < 60mS; Low Power mode < 120mS
6. Sensitivity adjusted by TK/EK pin capacitor (0pF~30pF)
7. Open-Drain Active Low output
8. TK pin activated after either EK pins touched
9. TK pin 8 second timeout reset, EK pins no timeout limit
10. Pin change Reset available
11. Built-in 2.3V LDO
12. LVR=2.0V
13. DFN-8, SOP8 package

APPLICATION CIRCUIT



PIN ASSIGNMENT



PIN DESCRIPTION

Name	In/Out	Pin Description
EK0, EK1	I	Ear touch detection input, these pins do not support press timeout
EKOUT	O	Ear touch detection open drain output, goes low when either EK0 or EK1 pressed
TK	I	Functional touch key detection input, activated after EK0 or EK1 pressed This pin generates chip reset after 8S pressed timeout
TKOUT	O	Function key open drain output, goes low when TK pressed
RST, RSTn	I	Pin change reset, this pin's state is recorded at power on stage, once the pin's state changes, the chip will reset
VDD, VSS	P	Power input pin and ground

DEVICE LIST

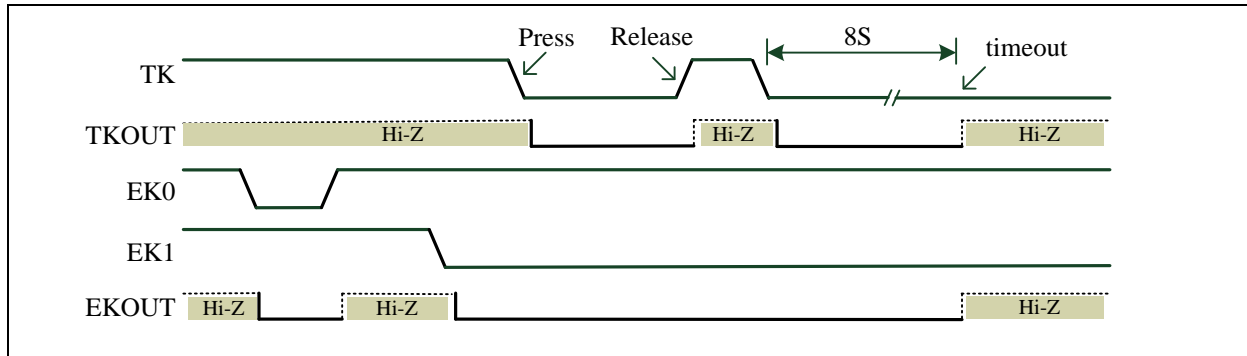
	Max. time for key press timeout	OUT pin output level	Sensitivity	2.3V LDO
TK8813E1	TK 8S, EK unlimited	Open-Drain Active Low	High	Enable

Note: The standard parts TK8813E1 is recommended.

FUNCTIONAL DESCRIPTION

1. Output Pin Function

EKOUT and TKOUT are active low open drain output. EKOUT goes low when either EK0 or EK1 pressed. If neither EK0 nor EK1 is pressed, TK pin stops detection and TKOUT reset to Hi-Z state.



2. Touch Sensitivity Adjustment

The sensitivity of touch key can be adjusted by the capacitance of TK/EK pin. The adjustment range is from 0pF to 30pF. Smaller capacitance can make higher sensitivity.

3. Key Press Timeout Reset

If EK pressed, Long press (8S) on the TK pin will generate a timeout chip reset.

4. Pin Change Reset

RST/RSTn pin's state is recorded at power on stage, once the pin's state changes, the chip will reset.

5. Normal mode and Low Power mode

The chip starts at Normal mode after reset. If no event occurred for 10 second, it switches to Low Power mode. It switches to Normal mode after sampling TK/EK pin's capacitance variation event.

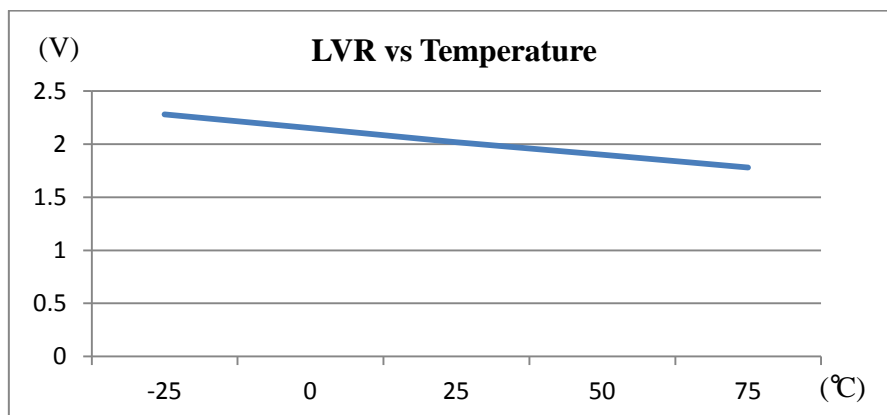
ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply voltage	$V_{SS}-0.3 \sim V_{SS}+5.5$	V
Input voltage	$V_{SS}-0.3 \sim V_{DD}+0.3$	
Operating temperature	-20 ~ +70	°C
Storage temperature	-65 ~ +150	

DC Characteristics (TA=25°C)

Parameter	Sym	Conditions		Min	Typ	Max	Unit
Input High Voltage	V_{IH}	all Input	-	$0.8V_{DD}$			V
Input Low Voltage	V_{IL}			-	-	$0.2V_{DD}$	
I/O Port Source Current	I_{OH}	all Output	$V_{DD}=3.0V$ $V_{OH}=2.7V$	-	5	-	mA
			$V_{DD}=5.0V$ $V_{OH}=4.5V$	-	10	-	
I/O Port Sink Current	I_{OL}	all Output	$V_{DD}=3.0V$ $V_{OL}=0.3V$	-	15	-	
			$V_{DD}=5.0V$ $V_{OL}=0.5V$	-	30	-	
Power Supply Current (TK8813E1)	I_{DD}	Normal mode	$V_{DD}=4.2V$	-	6.7	-	uA
			$V_{DD}=3.0V$	-	5.5	-	
		Low Power mode	$V_{DD}=4.2V$	-	2.2	-	
Power Supply Current (TK8813E0)	I_{DD}	Normal mode	$V_{DD}=4.2V$	-	15.4	-	uA
			$V_{DD}=3.0V$	-	7.7	-	
		Low Power mode	$V_{DD}=4.2V$	-	4.6	-	
			$V_{DD}=3.0V$	-	2.1	-	
Timeout Lead Time	T_{LT}		$V_{DD}=3.0V$	-	8	-	S
LVR Voltage	V_{LVR}	TA=25°C		1.8	2.0	2.2	V



PACKAGE INFORMATION

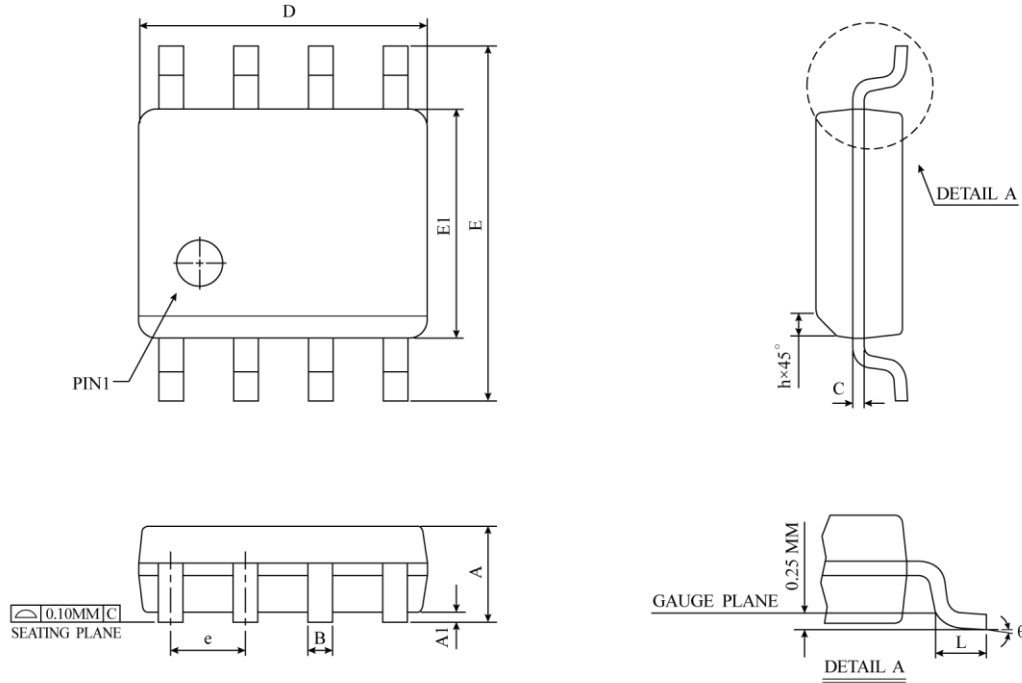
Please note that the package information provided is for reference only. Since this information is frequently updated, users can contact Sales to consult the latest package information and stocks.

Ordering Information

Ordering number	Package
TK8813E1-011-14	SOP8 (150mil)
TK8813E1-011-C9	DFN8 (2*2*0.5-0.5mm)

Package Information

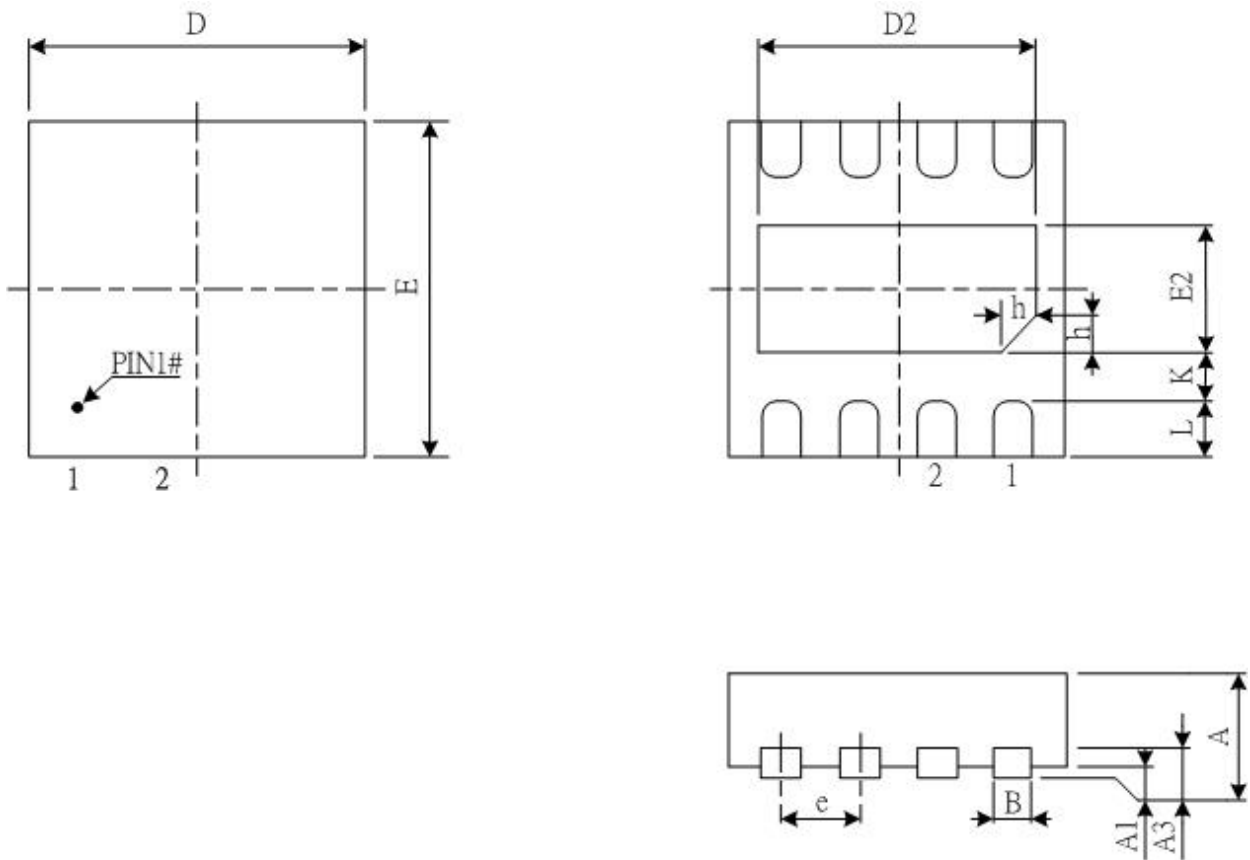
●SOP-8 (150mil) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	1.55	1.75	0.0532	0.0610	0.0688
A1	0.10	0.18	0.25	0.0040	0.0069	0.0098
B	0.33	0.42	0.51	0.0130	0.0165	0.0200
C	0.19	0.22	0.25	0.0075	0.0087	0.0098
D	4.80	4.90	5.00	0.1890	0.1939	0.1988
E	5.80	6.00	6.20	0.2284	0.2362	0.2440
E1	3.80	3.90	4.00	0.1497	0.1536	0.1574
e	1.27 BSC			0.050 BSC		
h	0.25	0.38	0.50	0.0099	0.0148	0.0196
L	0.40	0.84	1.27	0.0160	0.0330	0.0500
θ	0°	4°	8°	0°	4°	8°
JEDEC	MS-012 (AA)					

△ * NOTES : DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15 MM (0.006 INCH) PER SIDE.

• DFN 8pin (2x2x0.5-0.5mm) Package Dimension



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	-	0.02	0.05	-	0.001	0.002
A3	0.203 REF			0.008 REF		
B	0.15	0.20	0.25	0.006	0.008	0.010
D	1.90	2.00	2.10	0.075	0.079	0.083
E	1.90	2.00	2.10	0.075	0.079	0.083
D2	1.60	1.70	1.80	0.063	0.067	0.071
E2	0.80	0.90	1.00	0.031	0.035	0.039
e	0.50 BSC			0.020 BSC		
L	0.25	0.30	0.35	0.010	0.012	0.014
K	0.20	0.25	0.30	0.008	0.010	0.012
h	0.25	0.30	0.35	0.010	0.012	0.014
JEDEC	-					