PROUCT NAME
TM58PE10

TITLE
Applications of TIMER Interrupt on TM58PE10

APPLICATION NOTE
1. Types of interrupt methods
2. Substantial descriptions of interrupt methods
3. Application circuits

There are three TIMER Interrupt methods in TM58PE10: TMR0 IRQ, TMR1 IRQ and TMR2 IRQ. In addition, TMR1 and TMR2 can be combined to form a 16-bit timer. To use the timer IRQ function, users must select the ADVANCED mode of the TM58 series IC since IRQ function is only available in the advanced mode. In the advanced mode, the interrupt vector is at 3FFH.

Descriptions of interrupt methods:

1. TMR0 Interrupt
There are two special function registers associated with its operation, namely the interrupt mask register IRQM (address 21H) and the interrupt flag register IRQF (address 22H). Their definitions are tabulated as follow:

IRQM:

Control register IRQM (21H)		
Address	Symbol	Description
7	INTM	Bit for enabling use: The priority of this bit is higher than other interrupt enabling signals. 1: Enable 0: Disable **Note:** When the “RETI” command is executed, it sets the address of “INTM” to 1.
6	----	Unused
5	TMR2M	TMR2 interrupt enable: 1: enable interrupted 0: disable interrupted
4	TMR1M	TMR1 interrupt enable: 1: enable interrupted 0: disable interrupted

3	----	Unused
2	EXINTM1	External interrupt enable PA5/RESETB1/INT1: 1: enable interrupted 0: disable interrupted
1	EXINTM0	External interrupt enable PA0/RESETB0/INT0: 1: enable interrupted 0: disable interrupted
0	TMR0M	TMR0 interrupt enable: 1: enable interrupted 0: disable interrupted

FIG. 6-10 Interrupt Mask Register (IRQM Register)

IRQM:

Control register IRQF (22H)		
Address	Symbol	Description
7~6	----	Unused
5	TMR2F	TMR2 interrupt flag: 1: The overflow of TMR2 timer generates an interrupt request.
4	TMR1F	TMR1 interrupt flag: 1: The overflow of TMR1 timer generates an interrupt request.
3	----	Unused
2	EXINTF1	External interrupt flag 1: 1: PA5/RESETB1/INT1 The change in the falling edge of the pin generates an interrupt request (NOTE<4>)
1	EXINTF0	External interrupt flag 0: 1: PA0/RESETB0/INT0 The change in the falling edge of the pin generates an interrupt request (NOTE<4>)
0	TMR0F	TMR0 interrupt flag: 1: The overflow of TMR0 timer generates an interrupt request.

FIG. 1-2 Interrupt Flag Register (IRQF Register)

NOTE:

<1> TMR0 counts upwards and overflows when the value reaches 256.
The hardware will set TMR0F to 1 to enter interrupt.

<2> One should pay attention, when programming, to the saving of variables when entering interrupt and the resuming of variables when exiting interrupt.

<3> Primary interrupt generation time= 1/4M*4*tmr0 rate* (256-tmr0 value) second.

<4> The value of TMR0 should be reloaded when entering interrupt.

2. TMR1 interrupt

There are four special function registers (SFR) associated with its operation, namely the IRQM (Interrupt Mask Register, its address is 21H), the IRQF (Interrupt Flag Register, its address is 22H), TRM1Control, which is the control register of TMR1 (with the address of 24H), and TMR1Preload, which is the data register of TMR1 (with the address of 26H); SFRs are defined as follows:

TMR1Control:

<table>
<tr><td colspan="6">Control register TMR1 Control (24H)</td></tr>
<tr><td>Address</td><td>Symbol</td><td colspan="4">Description</td></tr>
<tr><td>7</td><td>TMR1EN</td><td colspan="4">TMR1 enable input:
1: TMR1 enable
0: TMR1 disable</td></tr>
<tr><td>6</td><td>LOAD</td><td colspan="4">Timer1 data loading mode:
1: When data is being written into TMR1 Preload register (TMR1_PRELOAD, 26H), the content of TMR1 is loaded immediately (default).
0: When data is being written into TMR1 Preload register (TMR1_PRELOAD, 26H), its value is not loaded until there is a count overflow in TMR1.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SUR1</td><td>SUR1 SUR0</td><td colspan="3">TMR1 clock source</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">SUR0</td><td>0 0
0 1
1 0
1 1</td><td colspan="3">Sourced from system time (only applicable to internal RC or external RC)(NOTE<5>)
Sourced from EXT_CLK
Sourced from TMR2 (Connected to form a 16bit timer)
Not executed</td></tr>
<tr><td>3</td><td>EDGE1</td><td colspan="4">EDGE1: Sourced from the edge control bit in the source signal of system time.
1: When EXT_CLK signal changes from high → low, TMR1 plus 1
0: When EXT_CLK signal changes from low → high, TMR1 plus 1</td></tr>
<tr><td>2~0</td><td>PS2~PS0</td><td>PS2</td><td>PS1</td><td>PS0</td><td>TMR1 prescaling ratio</td></tr>
<tr><td></td><td></td><td>0
0
0
0
1
1
1
1</td><td>0
0
1
1
0
0
1
1</td><td>0
1
0
1
0
1
0
1</td><td>1: 1
1: 2
1: 4
1: 8
1: 16
1: 32
1: 64
1: 128</td></tr>
</table>

FIG. 1-3 TMR1 Control register

TMR1、TMR2 Preload:

Control register TMR1, TMR2 Preload register (26H, 27H)		
Address	Symbol	Description
7~0	D7~D0	TMR1 and TMR2 Preload data register. Default data value: D7~ D0 = FFH

NOTE:

<1> TMR1 counts down, and data overflow occurs after the value becomes 00, then the hardware sets TMR1F to 1 in order to enter an interrupt.

<2> During programming, special attention should be directed to the storage of variables when entering an interrupt; as well as the restoration of variables when exiting an interrupt.

<3> The time for generating an interrupt =1/4＊tmr1 prescaler rate＊tmr1 preload seconds

<4> When entering an interrupt, the value of TMR1Preload does not need to be reloaded, the already defined value in the preload register will be automatically reloaded into the timer register.

<5> The setting of Tmr1 data load mode for entering the TMR1Control register: when it is 1 (default) and there is data to be written into the register, the count value of TMR1 changes immediately. When it is 0 and there is data to be written into the register, the data can only be written into the register after a count overflow of TMR1 has occurred. As shown in the following diagram:

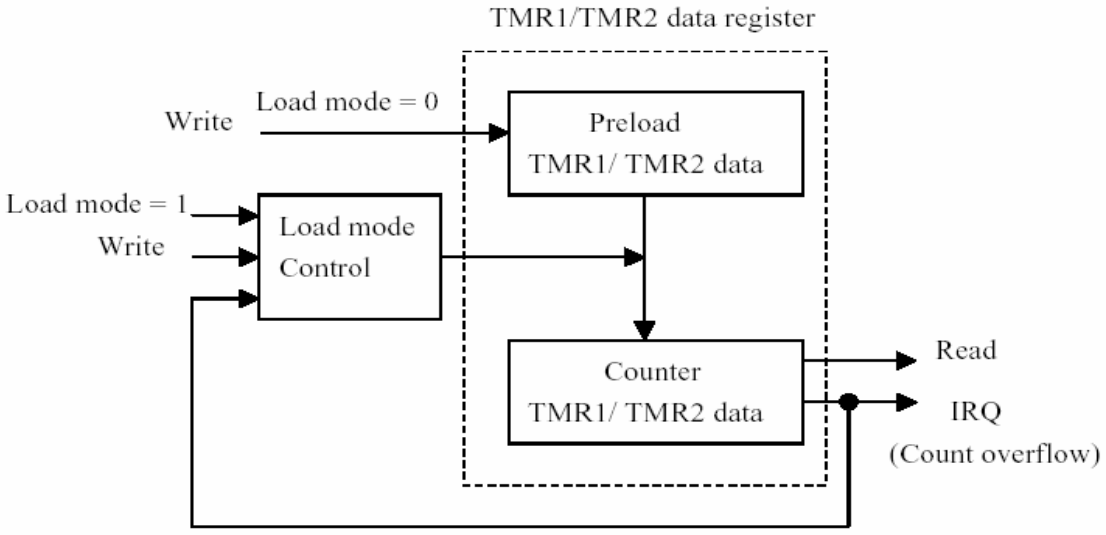

FIG. 1-5 TMR1/TMR2 Data register (timer/preloader)

3. TMR2 interrupt

There are four special function registers (SFR) associated with its operation, namely the IRQM (Interrupt Mask Register, its address is 21H), the IRQF (Interrupt Flag Register, its address is 22H), TRM2Control, which is the control register of TMR2 (with the address of 25H), and TMR2Preload, which is the data register of TMR2 (with the address of 27H); the four SFRs are defined as follows:

<table>
<tr><td colspan="5">Control register TMR2 Control (25H)</td></tr>
<tr><td>Address</td><td>Symbol</td><td colspan="3">Description</td></tr>
<tr><td>7</td><td>TMR2EN</td><td colspan="3">TMR2 enable input:
1: TMR2 enable
0: TMR2 disable</td></tr>
<tr><td>6</td><td>LOAD</td><td colspan="3">TMR2 data loading mode:
1: When data is being written into TMR2 Preload register (TMR2_PRELOAD, 27H), the content of TMR2 is loaded immediately (default).
0: When data is being written into TMR2 Preload register (TMR1_PRELOAD, 26H), its value is not loaded until there is a count overflow in TMR2.</td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">SUR1</td><td>SUR1
SUR0</td><td colspan="2">TMR2 clock source</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">SUR0</td><td>0 0
0 1
1 0
1 1</td><td colspan="2">Sourced from system time (only applicable in CRYSTAL mode)(NOTE<5>)
Sourced from EXT_CLK
Sourced from TMR1 (Connected to form a 16bit timer)
Not executed</td></tr>
<tr><td>3</td><td>EDGE2</td><td colspan="3">EDG2: Sourced from the edge control bit in the TMR2 clock signal of EXT_CLK.
1: When EXT_CLK signal changes from high → low, TMR2 plus 1
0: When EXT_CLK signal changes from low → high, TMR2 plus 1</td></tr>
<tr><td>2~0</td><td>PS2~PS0</td><td colspan="3"><table><tr><td>PS2</td><td>PS1</td><td>PS0</td><td>TMR2 Prescaler</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1: 1</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1: 2</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1: 4</td></tr><tr><td>0</td><td>1</td><td>1</td><td>1: 8</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1: 16</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1: 32</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1: 64</td></tr><tr><td>1</td><td>1</td><td>1</td><td>1: 128</td></tr></table></td></tr>
</table>

FIG. 1-6 TMR2 Control register

Control register TMR1, TMR2 Preload register (26H, 27H)		
Address	Symbol	Description
7~0	D7~D0	TMR1 and TMR2 Preload data register Default data value: D7~ D0 = FFH

FIG. 1-7 TMR1 and TMR2 Preload data register

NOTE:

<1> TMR2 counts down, and data overflow occurs after the value becomes 00, then the hardware sets TMR2F to 1 in order to enter an interrupt.

<2> During programming, special attention should be directed to the storage of variables when entering an interrupt; as well as the restoration of variables when exiting an interrupt.

<3> The time for generating an interrupt =1/4∗tmr2 prescaler rate∗tmr1 preload seconds.

<4> When entering an interrupt, the value of TMR2Preload does not need to be reloaded.
the already defined value in the preload register will be automatically reloaded into the timer register.

<5> The setting of Tmr2 data mode for the TMR2Control register:
when it is 1 (default) and there is data to be written into the register, the count value of TMR2 changes immediately. When it is 0 and there is data to be written into the register, the data can only be written into the register after a count overflow of TMR2 has occurred. As shown in the following diagram:

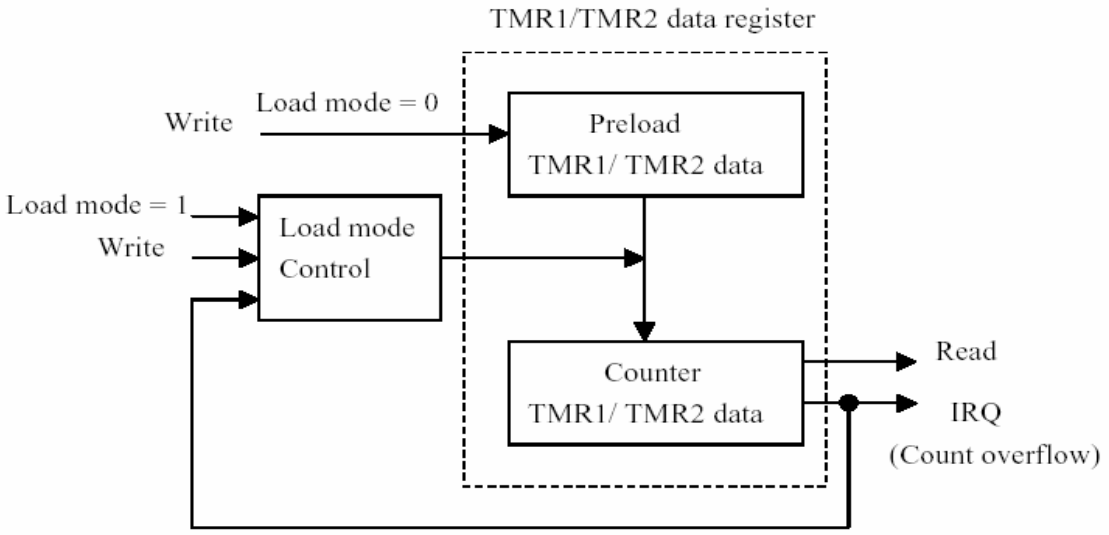

FIG. 1-5 TMR1/TMR2 Data register (timer/preloader)

4. Combining TMR1 and TMR2 interrupts (TMR1 Source from TMR2):

There are six types of SFR that are related to this mode of interrupt: they are the IRQM (Interrupt Mask Register, its address is 21H), the IRQF (Interrupt Flag Register, its address is 22H), TRM1Control, which is the control register of TMR1 (with the address of 24H), TMR1Preload, which is the data register of TMR1 (with the address of 26H), TRM2Control, which is the control register of TMR2 (with the address of 25H), and TMR2Preload, which is the data register of TMR2 (with the address of 27H).

NOTE:

<1> Under this mode, TMR2Control[5：4] should be fixed at 0 0, which means TMR2 Source originates from System CLK (Only Crystal mode), whereas [5:4] should be fixed at 1 0, which means TMR1 Source originates from TMR2.

<2> Under this mode, the prescale frequency of tmr2 can be selected by setting the tmr2 control register, but the prescale frequency of tmr1 can only be fixed at 1:1.

<3> The time for generating an interrupt =1/4M＊（（tmr1preload －1）＊256＋tmr2preload）＊tmr2prescaler rate seconds.

<4> When entering an interrupt, the values of TMR1Preload and TMR2Perload do not need to be re-loaded.

5. Combining TMR2 and TMR1 interrupts (TMR2 Source from TMR1):

There are six types of SFR associated with its operation, namely the IRQM (Interrupt Mask Register, its address is 21H), the IRQF (Interrupt Flag Register, its address is 22H), TRM1Control, which is the control register of TMR1 (with the address of 24H), TMR1Preload, which is the data register of TMR1 (with the address of 26H), TRM2Control, which is the control register of TMR2 (with the address of 25H), and TMR2Preload, which is the data register of TMR2 (with the address of 27H).

NOTE:

<1> Under this mode, TMR1Control[5：4] should be fixed at 0 0, which means TMR1 Source originates from System CLK (Only Internal RC or External RC), whereas TMR2Control[5:4] should be fixed at 1 0, which means TMR2 Source originates from TMR1.

<2> Under this mode, the prescale frequency of TMR1 can be selected by setting theTMR1 control register, but the prescale frequency of TMR2 can only be fixed at 1:1.

<3> The time for generating an interrupt =1/4M＊（（tmr2preload －1）＊256＋tmr1preload）＊tmr1prescaler rate seconds.

<4> When entering an interrupt, the values of TMR1Preload and TMR2Perload do not need to be re-loaded.

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Examples will be used to explain the different types of interrupts in the following sections:

Ex. 1: Using the TMR0 interrupt

Program function: By using PORTB, 0 PIN to control LED to flash at the speed of approximately 1Hz (bright 500mS, dark 500mS).

(Diagram of the applicable circuit Y_2)

Firstly, it is necessary to select simulation and set up the configuration for the hardware of WDT within CONFIG WORD.

```
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,configuration word,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
;TYPE=Advanced ,CLOCK=SINGLE,NT
;WDTE=Disable ,CPT=ON,LV=Don't use
;RESETB0=PA0 be normal I/O pin
;RESETB1=RESETB(PA5)be input pin
;IOC=OSC1,2 be clock pin
;AUP=Enable auto update page in advance mode
;INRC_FREQ=4M
;WORK_VOLTAGE=5V
;--------------------------------------------------------------------------------
;;;;;;;;;;;;;;;;;;;;;;;;;;;;Register Definitions;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;--------------------special register---------------------------------------
IAR                 EQU   00H
TMR0                EQU   01H
PC                  EQU   02H
STATUS              EQU   03H
BSR                 EQU   04H
PORTA               EQU   05H
PORTB               EQU   06H
PULL_HI             EQU   20H
IRQM                EQU   21H
IRQF                EQU   22H
WDTSEL              EQU   23H
TMR1CONTROL         EQU   24H
TMR2CONTROL         EQU   25H
TMR1PRELOAD         EQU   26H
TMR2PRELOAD         EQU   27H
WAKE_UP             EQU   40H
;--------------STATUS REGISTER BIT-----------------------------------
C                   EQU   0
DC                  EQU   1
Z                   EQU   2
PDB                 EQU   3
TOB                 EQU   4
SA0                 EQU   5
A8                  EQU   6
;----------------IRQM REGISTER BIT-------------------------------------
TIMR0M              EQU   0
EXINTM0             EQU   1
EXINTM1             EQU   2
TMR1M               EQU   4
TMR2M               EQU   5
INTM                EQU   7
;----------------IRQF REGISTER BIT-------------------------------------
TMR0F               EQU   0
EXINTF0             EQU   1
EXINTF1             EQU   2
TMR1F               EQU   4
```

```
TMR2F           EQU  5
;--------------INSTRUCTION FLAG----------------------------
A               EQU  0
M               EQU  1
;--------------GENEPORTA1 REGISTER --------------------
ACC_BUF         EQU  07H
STATUS_BUF      EQU  08H
COUNT           EQU  09H
```

```
;****************** PROGRAM STARTS ************************************************************
        ORG             3FEH
        LGOTO           INTERRUPT
        ORG             3FFH
        LGOTO           MAIN
-------------------------------------------------------------------------------------------------
        ORG             00H
MAIN
        CLRM            ACC_BUF
        CLRM            STATUS_BUF
        CLRM            COUNT

        MOVLA           B'00000000'
        IODIR           PORTB
        CLRM            PORTB

        MOVLA           B'00000111'     ; TMR0 PRESCALE FREQUENCY 1：256
        MOVAM           IRQM

        MOVLA           .191
        MOVAM           TMR0
        MOVLA           B'10000001'     ; TMR0 INTERRUPT ENABLE
        MOVAM           IRQM
LOOP:
        LGOTO           LOOP
-------------------------------------------------------------------------------------------------
THE TIME FOR GENERATING AN INTERRUPT=1/4M＊4＊256＊(256-191)=0.01664S
INTERRUPT:
        MOVAM           ACC_BUF         ; STORING ACC AND STATUS
                                          REGISTER VALUES
        SWAPM           STATUS,A
        MOVAM           STATUS_BUF
        MOVLA           .191
        MOVAM           TMR0
        INCM            COUNT,M
        MOVLA           .30
        XORAM           COUNT,A         ; 0.016664*30=0.4992S(CLOSE TO
                                          500mS)
        BTMSS           STATUS,Z
```

```
        LGOTO           INTERRUPT_END
        CLRM            COUNT
        MOVLA           B'00000001'
        XORAM           PORTB,M          ; 500mS IS UP, CHANGES THE STATUS
                                           OF PORTB TO 0
INTERRUPT_END:
        BCM             IRQF,TMR0F
        SWAPM           STATUS_BUF,A
        MOVAM           STATUS           ; RESTORING ACC AND STATUS
                                           REGISTER VALUES BEFORE THE
                                           INTERRUPT
        MOVM            ACC_BUF,A
        RETI
------------------------------------------------------------
        END
;==========================================================================
```

Ex. 2: Using the TMR1 interrupt

Program function: By using PORTB, 0 PIN to control LED to flash at the speed of approximately 1Hz (bright 500mS, dark 500mS).

(Diagram of the applicable circuit Y_1)

Firstly, it is necessary to select simulation and set up the configuration for the hardware of WDT within CONFIG WORD.

```
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,configuration word,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
;TYPE=Advanced ,CLOCK=SINGLE ,external RC
;WDTE=Disable, CPT=ON,LV=Don't use
;RESETB0=PA0 be normal I/O pin
;RESETB1=RESETB(PA5)be input pin
;IOC=OSC1,2 be clock pin
;AUP=Enable auto update page in advance mode
;INRC_FREQ=4M
;WORK_VOLTAGE=5V
;-----------------------------------------------------------------------------------------
;;;;;;;;;;;;;;;;;;;;;;;;;REGISTER DEFINITIONS;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;--------------------SPICIAL REGISTER ---------------------------------------
IAR             EQU   00H
TMR0            EQU   01H
PC              EQU   02H
STATUS          EQU   03H
BSR             EQU   04H
PORTA           EQU   05H
PORTB           EQU   06H
PULL_HI         EQU   20H
IRQM            EQU   21H
IRQF            EQU   22H
WDTSEL          EQU   23H
TMR1CONTROL     EQU   24H
TMR2CONTROL     EQU   25H
TMR1PRELOAD     EQU   26H
```

```
TMR2PRELOAD     EQU   27H
WAKE_UP         EQU   40H
;-------------STATUS REGISTER BIT----------------------
C       EQU   0
DC      EQU   1
Z       EQU   2
PDB     EQU   3
TOB     EQU   4
SA0     EQU   5
A8      EQU   6
;----------------IRQM REGISTER BIT--------------------------
TIMR0M      EQU   0
EXINTM0     EQU   1
EXINTM1     EQU   2
TMR1M       EQU   4
TMR2M       EQU   5
INTM        EQU   7
;----------------IRQF REGISTER BIT--------------------------
TMR0F           EQU       0
EXINTF0         EQU       1
EXINTF1         EQU       2
TMR1F           EQU       4
TMR2F           EQU       5
;--------------INSTRUCTION FLAG----------------------------
A       EQU   0
M       EQU   1
;--------------GENEPORTA1 REGISTER ----------------------
ACC_BUF         EQU   07H
STATUS_BUF      EQU   08H
COUNT           EQU   09H
```

```
;****************** PROGRAM STARTS ************************************************************
        ORG                 3FEH
        LGOTO               INTERRUPT
        ORG                 3FFH
        LGOTO               MAIN
-------------------------------------------------------------------------------------------------
        ORG                 00H
MAIN
        CLRM                ACC_BUF
        CLRM                STATUS_BUF
        CLRM                COUNT

        MOVLA               B'00000000'
        IODIR               PORTB
        CLRM                PORTB

        MOVLA               B'10010000'         ; TMR1 INTERRUPT ENABLE
        MOVAM               IRQM
```

```
        MOVLA           .130
        MOVAM           TMR1PRELOAD
        MOVLA           B'11000111'         ; TMR1 PRESCALE FREQUENCY
                                              1：128
        MOVAM           TMR1CONTROL         ; TMR1 FROM EXTERNAL RC
LOOP:
        LGOTO           LOOP
-------------------------------------------------------------------------------------------------
THE TIME FOR GENERATING AN INTERRUPT =1/4＊128＊130=0.00416 S
INTERRUPT:
        MOVAM           ACC_BUF             ; STORING ACC AND STATUS
                                              REGISTER VALUES
        SWAPM           STATUS,A
        MOVAM           STATUS_BUF
        INCM            COUNT,M
        MOVLA           .120
        XORAM           COUNT,A             ; 0.00416*120=0.4992S(CLOSE TO
                                              500mS)
        BTMSS           STATUS,Z
        LGOTO           INTERRUPT_END
        CLRM            COUNT
        MOVLA           B'00000001'
        XORAM           PORTB,M             ; 500mS IS UP, CHANGES THE STATUS
                                              OF PORTB TO 0
INTERRUPT_END:
        BCM             IRQF,TMR1F
        SWAPM           STATUS_BUF,A
        MOVAM           STATUS              ; RESTORING ACC AND STATUS
                                              REGISTER VALUES BEFORE THE
                                              INTERRUPT
        MOVM            ACC_BUF,A
        RETI
-----------------------------------------------------------
        END
; ==========================================================================
```

Ex. 3: Using the TMR2 interrupt

Program function: By using PORTB, 0 PIN to control LED to flash at the speed of approximately 1Hz (bright 500mS, dark 500mS).

(Diagram of the applicable circuit Y_2)

Firstly, it is necessary to select simulation and set up the configuration for the hardware of WDT within CONFIG WORD.

```
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,configuration word,,,,,,,,,,,,,,,,,,,,,
;TYPE=Advanced ,CLOCK=NT
;WDTE=Disable ,CPT=ON,LV=Don't use
;RESETB0=PA0 be normal I/O pin
;RESETB1=RESETB(PA5)be input pin
;IOC=OSC1,2 be clock pin
```

```
;AUP=Enable auto update page in advance mode
;INRC_FREQ=4M
;WORK_VOLTAGE=5V
;-------------------------------------------------------------------------------------
;;;;;;;;;;;;;;;;;;;;;;;;;;REGISTER DEFINITIONS;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;--------------------SPECIAL REGISTER ----------------------------------------
IAR                 EQU   00H
TMR0                EQU   01H
PC                  EQU   02H
STATUS              EQU   03H
BSR                 EQU   04H
PORTA               EQU   05H
PORTB               EQU   06H
PULL_HI             EQU   20H
IRQM                EQU   21H
IRQF                EQU   22H
WDTSEL              EQU   23H
TMR1CONTROL         EQU   24H
TMR2CONTROL         EQU   25H
TMR1PRELOAD         EQU   26H
TMR2PRELOAD         EQU   27H
WAKE_UP             EQU   40H
;--------------STATUS REGISTER BIT-----------------------
C                   EQU   0
DC                  EQU   1
Z                   EQU   2
PDB                 EQU   3
TOB                 EQU   4
SA0                 EQU   5
A8                  EQU   6
;----------------IRQM REGISTER BIT--------------------------
TIMR0M              EQU   0
EXINTM0             EQU   1
EXINTM1             EQU   2
TMR1M               EQU   4
TMR2M               EQU   5
INTM                EQU   7
;----------------IRQF REGISTER BIT--------------------------
TMR0F               EQU   0
EXINTF0             EQU   1
EXINTF1             EQU   2
TMR1F               EQU   4
TMR2F               EQU   5
;--------------INSTRUCTION FLAG----------------------
A                   EQU   0
M                   EQU   1
;--------------GENEPORTA1 REGISTER ---------------
ACC_BUF             EQU   07H
```

```
STATUS_BUF      EQU   08H
COUNT           EQU   09H

;****************** PROGRAM STARTS ************************************************************
        ORG             3FEH
        LGOTO           INTERRUPT
        ORG             3FFH
        LGOTO           MAIN
-----------------------------------------------------------------------------------------------
        ORG             00H
MAIN
        CLRM            ACC_BUF
        CLRM            STATUS_BUF
        CLRM            COUNT

        MOVLA           B'00000000'
        IODIR           PORTB
        CLRM            PORTB

        MOVLA           B'10100000'     ; TMR2 INTERRUPT ENABLE
        MOVAM           IRQM

        MOVLA           .130
        MOVAM           TMR2PRELOAD
        MOVLA           B'11000111'     ; TMR2 PRESCALE FREQUENCY
                                          1：128
        MOVAM           TMR2CONTROL     ; TMR2 FROM CRYSTAL OSCILLATION
                                          MODE
LOOP:
        LGOTO           LOOP
-----------------------------------------------------------------------------------------------
THE TIME FOR GENERATING AN INTERRUPT =1/4＊128＊130=0.00416 S
INTERRUPT:
        MOVAM           ACC_BUF         ; STORING ACC AND STATUS
                                          REGISTER VALUES
        SWAPM           STATUS,A
        MOVAM           STATUS_BUF
        INCM            COUNT,M
        MOVLA           .120            ; AFTER 120 TIMES OF INTERRUPTS,
                                          THESTATUS OF PORTB, 0 IS
                                          CHANGED
        XORAM           COUNT,A         ; 0.00416*120=0.4992S
                                          (CLOSE TO 500mS)
        BTMSS           STATUS,Z
        LGOTO           INTERRUPT_END
        CLRM            COUNT
        MOVLA           B'00000001'
        XORAM           PORTB,M         ; 500mS IS UP, CHANGES THE STATUS
```

```
                                                        OF PORTB TO 0
INTERRUPT_END:
        BCM             IRQF,TMR2F
        SWAPM           STATUS_BUF,A
        MOVAM           STATUS                  ; RESTORING ACC AND STATUS
                                                  REGISTER VALUES BEFORE THE
                                                  INTERRUPT
        MOVM            ACC_BUF,A
        RETI
--------------------------------------------------------------
        END
; ==================================================================
```

Ex. 4: Combining TMR1 and TMR2 interrupts (TMR1 sources from TMR2)

Program function: By using PORTB, 0 PIN to control LED to flash at the speed of approximately 1Hz (bright 500mS, dark 500mS).

(Diagram of the applicable circuit Y_2)

Firstly, it is necessary to select simulation and set up the configuration for the hardware of WDT within CONFIG WORD.

```
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,configuration word,,,,,,,,,,,,,,,,,
;TYPE=Advanced ,CLOCK=NT
;WDTE=Disable ,CPT=ON,LV=Don't use
;RESETB0=PA0 be normal I/O pin
;RESETB1=RESETB(PA5)be input pin
;IOC=OSC1,2 be clock pin
;AUP=Enable auto update page in advance mode
;INRC_FREQ=4M
;WORK_VOLTAGE=5V
;-------------------------------------------------------------------------------------------
;;;;;;;;;;;;;;;;;;;;;;;;;;REGISTER DEFINITIONS;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;--------------------SPECIAL REGISTER ----------------------------------------
IAR             EQU   00H
TMR0            EQU   01H
PC              EQU   02H
STATUS          EQU   03H
BSR             EQU   04H
PORTA           EQU   05H
PORTB           EQU   06H
PULL_HI         EQU   20H
IRQM            EQU   21H
IRQF            EQU   22H
WDTSEL          EQU   23H
TMR1CONTROL     EQU   24H
TMR2CONTROL     EQU   25H
TMR1PRELOAD     EQU   26H
TMR2PRELOAD     EQU   27H
WAKE_UP         EQU   40H
;--------------STATUS REGISTER BIT--------------------------
C               EQU   0
```

```
DC              EQU   1
Z               EQU   2
PDB             EQU   3
TOB             EQU   4
SA0             EQU   5
A8              EQU   6
;----------IRQM REGISTER BIT----------
TIMR0M          EQU   0
EXINTM0         EQU   1
EXINTM1         EQU   2
TMR1M           EQU   4
TMR2M           EQU   5
INTM            EQU   7
;----------IRQF REGISTER BIT----------
TMR0F           EQU   0
EXINTF0         EQU   1
EXINTF1         EQU   2
TMR1F           EQU   4
TMR2F           EQU   5
;----------INSTRUCTION FLAG----------
A               EQU   0
M               EQU   1
;----------GENEPORTA1 REGISTER ----------
ACC_BUF         EQU   07H
STATUS_BUF      EQU   08H
COUNT           EQU   09H
```

```
;****************** PROGRAM STARTS ************************************************************
        ORG             3FEH
        LGOTO           INTERRUPT
        ORG             3FFH
        LGOTO           MAIN
-------------------------------------------------------------------------------------------------
        ORG             00H
MAIN
        CLRM            ACC_BUF
        CLRM            STATUS_BUF
        CLRM            COUNT

        MOVLA           B'00000000'
        IODIR           PORTB
        CLRM            PORTB

        MOVLA           B'10010000'         ;TMR1 INTERRUPT ENABLE
        MOVAM           IRQM

        MOVLA           B'01100000'         ;TMR1 PRESCALE FREQUENCY
                                              1 : 1
        MOVAM           TMR1CONTROL         ;TMR1 SOURCE FROM
```

```
                                        TMR2(CONNECTED TO TMR2 TO
                                        FORM A 16BIT TIMER)

        MOVLA           B'01000111'     ;TMR2 PRESCALE FREQUENCY
                                         1：128
        MOVAM           TMR2CONTROL     ; TMR2 FROM CRYSTAL
                                         OSCILLATION
        MOVLA           09H
        MOVAM           TMR2PRELOAD

        MOVLA           03H
        MOVAM           TMR1PRELOAD

        BSM             TMR2CONTROL,7
        BSM             TMR1CONTROL,7
LOOP:
        LGOTO           LOOP
-------------------------------------------------------------------------------------------------------
THE TIME FOR GENERATING AN INTERRUPT =1/4＊((3-1)＊256+9)*128=0.016672 S
INTERRUPT:
        MOVAM           ACC_BUF         ; STORING ACC AND STATUS
                                          REGISTER VALUES
        SWAPM           STATUS,A
        MOVAM           STATUS_BUF

        INCM            COUNT,M
        MOVLA           .30
        XORAM           COUNT,A          ;  0.016672*30=0.50016 S(CLOSE TO
                                           500mS)
        BTMSS           STATUS,Z
        LGOTO           INTERRUPT_END
        CLRM            COUNT
        MOVLA           B'00000001'
        XORAM           PORTB,M         ; 500mS IS UP, CHANGES THE STATUS
                                          OF PORTB TO 0
INTERRUPT_END:
        BCM             IRQF,TMR1F      ; CLEARS TMR1INTERRUPT FLAG
        SWAPM           STATUS_BUF,A
        MOVAM           STATUS          ; RESTORING ACC AND STATUS
                                          REGISTER VALUES BEFORE THE
                                          INTERRUPT
        MOVM            ACC_BUF,A
        RETI
-----------------------------------------------------------
        END
; ===========================================================
```

Ex. 5: Combining TMR2 and TMR1 interrupts (TMR2 sources from TMR1)

Program function: By using PORTB, 0 PIN to control LED to flash at the speed of approximately 1Hz (bright 500mS, dark 500mS).

(Diagram of the applicable circuit Y_2)

Firstly, it is necessary to select simulation and set up the configuration for the hardware of WDT within CONFIG WORD.

```
,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,configuration word,,,,,,,,,,,,,,,,
;TYPE=Advanced ,CLOCK=SINGLE ,external RC
;WDTE=Disable ,CPT=ON,LV=Don't use
;RESETB0=PA0 be normal I/O pin
;RESETB1=RESETB(PA5)be input pin
;IOC=OSC1,2 be clock pin
;AUP=Enable auto update page in advance mode
;INRC_FREQ=4M
;WORK_VOLTAGE=5V
;-------------------------------------------------------------------------------------
;;;;;;;;;;;;;;;;;;;;;;;;;REGISTER DEFINITINOS;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
;--------------------SPICIAL REGISTER ----------------------------------------
IAR                 EQU   00H
TMR0                EQU   01H
PC                  EQU   02H
STATUS              EQU   03H
BSR                 EQU   04H
PORTA               EQU   05H
PORTB               EQU   06H
PULL_HI             EQU   20H
IRQM                EQU   21H
IRQF                EQU   22H
WDTSEL              EQU   23H
TMR1CONTROL         EQU   24H
TMR2CONTROL         EQU   25H
TMR1PRELOAD         EQU   26H
TMR2PRELOAD         EQU   27H
WAKE_UP             EQU   40H
;--------------STATUS REGISTER BIT-----------------------
C                   EQU   0
DC                  EQU   1
Z                   EQU   2
PDB                 EQU   3
TOB                 EQU   4
SA0                 EQU   5
A8                  EQU   6
;----------------IRQM REGISTER BIT--------------------------
TIMR0M              EQU   0
EXINTM0             EQU   1
EXINTM1             EQU   2
TMR1M               EQU   4
TMR2M               EQU   5
INTM                EQU   7
```

```
;----------------IRQF REGISTER BIT--------------------------
TMR0F           EQU  0
EXINTF0         EQU  1
EXINTF1         EQU  2
TMR1F           EQU  4
TMR2F           EQU  5
;--------------INSTRUCTION FLAG-----------------------------
A               EQU  0
M               EQU  1
;--------------GENEPORTA1 REGISTER ----------------------
ACC_BUF         EQU  07H
STATUS_BUF      EQU  08H
COUNT           EQU  09H
```

```
;****************** PROGRAM STARTS ************************************************************
        ORG             3FEH
        LGOTO           INTERRUPT
        ORG             3FFH
        LGOTO           MAIN
-------------------------------------------------------------------------------------------------
        ORG             00H
MAIN
        CLRM            ACC_BUF
        CLRM            STATUS_BUF
        CLRM            COUNT

        MOVLA           B'00000000'
        IODIR           PORTB
        CLRM            PORTB

        MOVLA           B'10100000'         ; TMR2 INTERRUPT ENABLE
        MOVAM           IRQM

        MOVLA           B'01000111'         ;TMR1 PRESCALE FREQUENCY
                                             1：128
        MOVAM           TMR1CONTROL         ;TMR1 FROM EXTERNAL RC

        MOVLA           B'01000111'         ;TMR2 PRESCALE FREQUENCY
                                             1：1
        MOVAM           TMR2CONTROL         ;TMR2 FROM TMR1(CONNECTED
                                             TO TMR2 AND FORM A 16BIT
                                             TIMER)

        MOVLA           03H
        MOVAM           TMR2PRELOAD

        MOVLA           09H
        MOVAM           TMR1PRELOAD
```

```
        BSM             TMR2CONTROL,7
        BSM             TMR1CONTROL,7
LOOP:
        LGOTO           LOOP
-------------------------------------------------------------------------------------------------------
THE TIME FOR GENERATING AN INTERRUPT =1/4＊((3-1)＊256+9)*128=0.016672 S
INTERRUPT:
        MOVAM           ACC_BUF         ; STORING ACC AND STATUS
                                          REGISTER VALUES
        SWAPM           STATUS,A
        MOVAM           STATUS_BUF

        INCM            COUNT,M
        MOVLA           .30
        XORAM           COUNT,A         ; 0.016672*30=0.50016 S(CLOSE TO
                                          500mS)
        BTMSS           STATUS,Z
        LGOTO           INTERRUPT_END
        CLRM            COUNT
        MOVLA           B'00000001'
        XORAM           PORTB,M         ; 500MS IS UP, CHANGES THE STATUS
                                          OF PORTB TO 0
INTERRUPT_END:
        BCM             IRQF,TMR2F      ;CLEARS TMR2 INTERRUPT FLAG
        SWAPM           STATUS_BUF,A
        MOVAM           STATUS          ; RESTORING ACC AND STATUS
                                          REGISTER VALUES BEFORE THE
                                          INTERRUPT
        MOVM            ACC_BUF,A
        RETI
-------------------------------------------------------------
        END
; ===========================================================
```

Diagrams of the applicable circuits